

FIG. 1

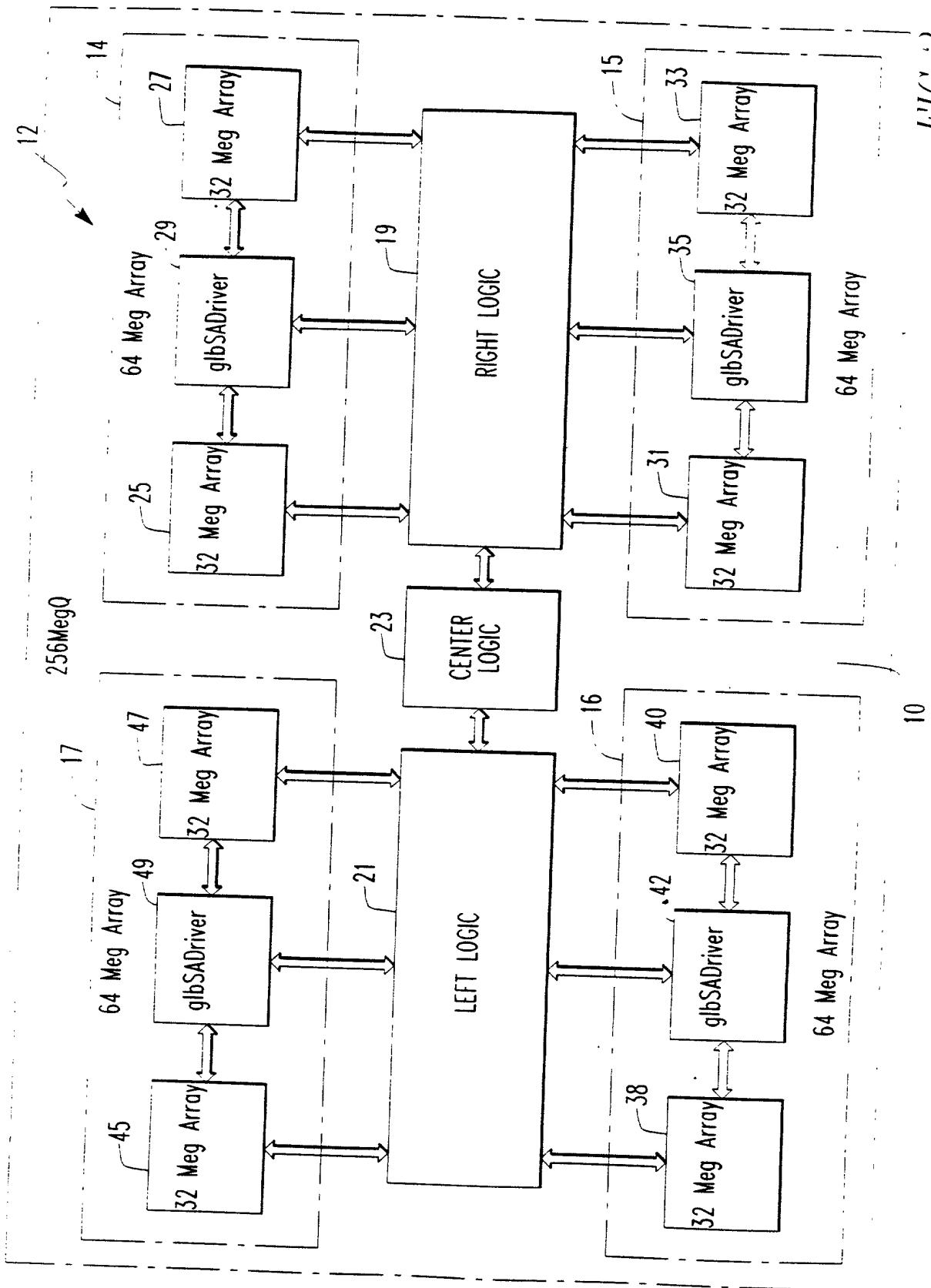
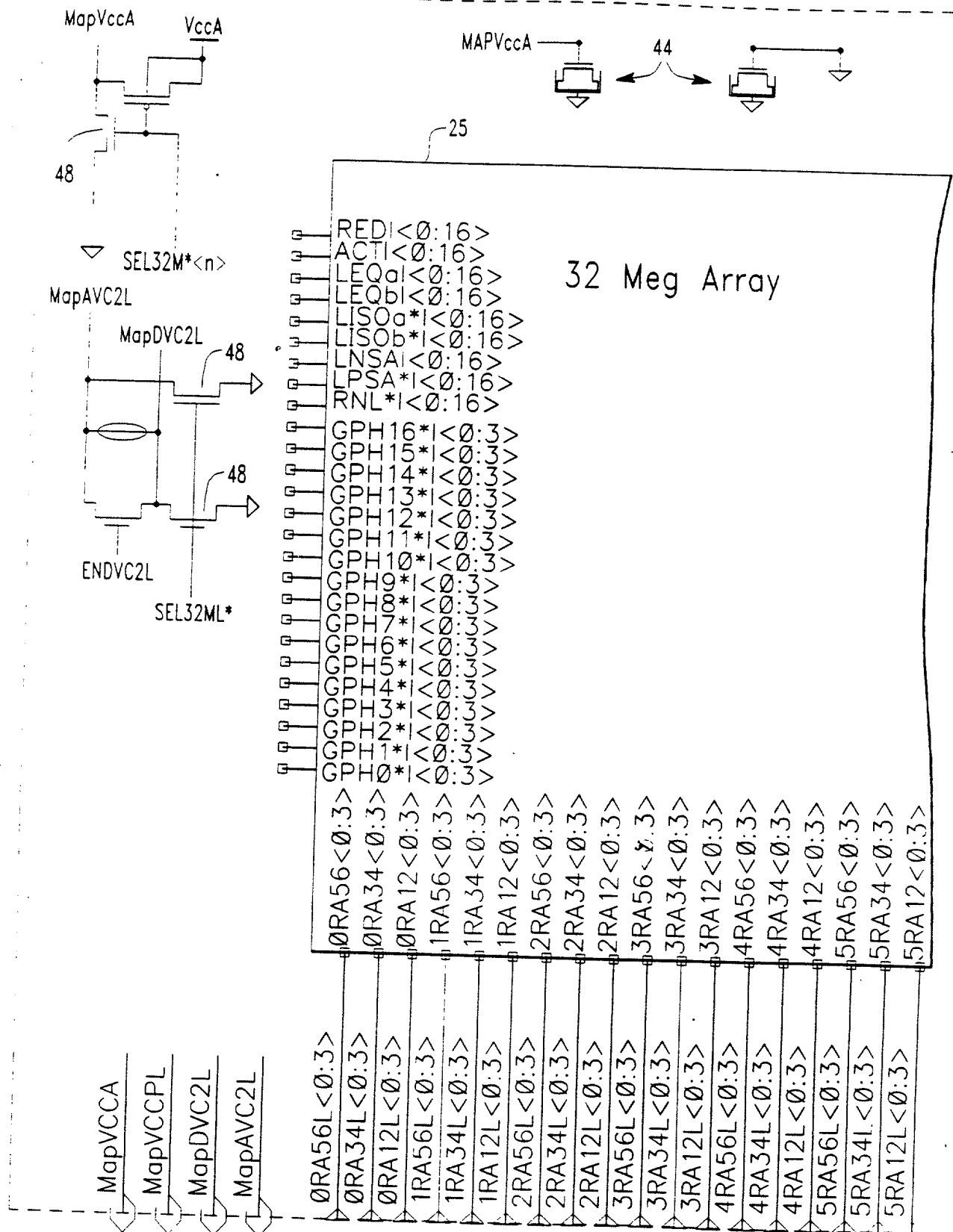


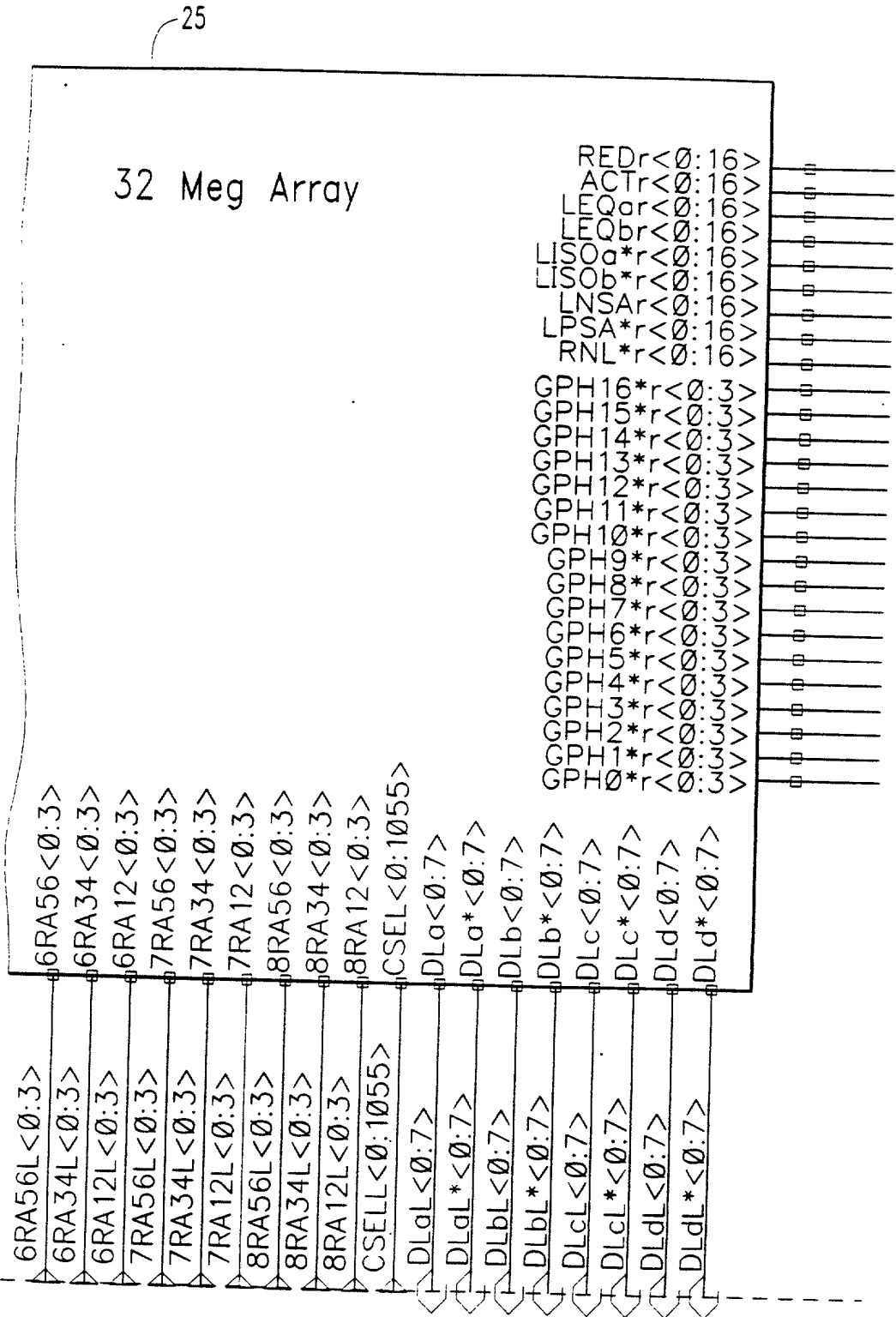
FIG. 2

FIG. 3A

3,367



.....



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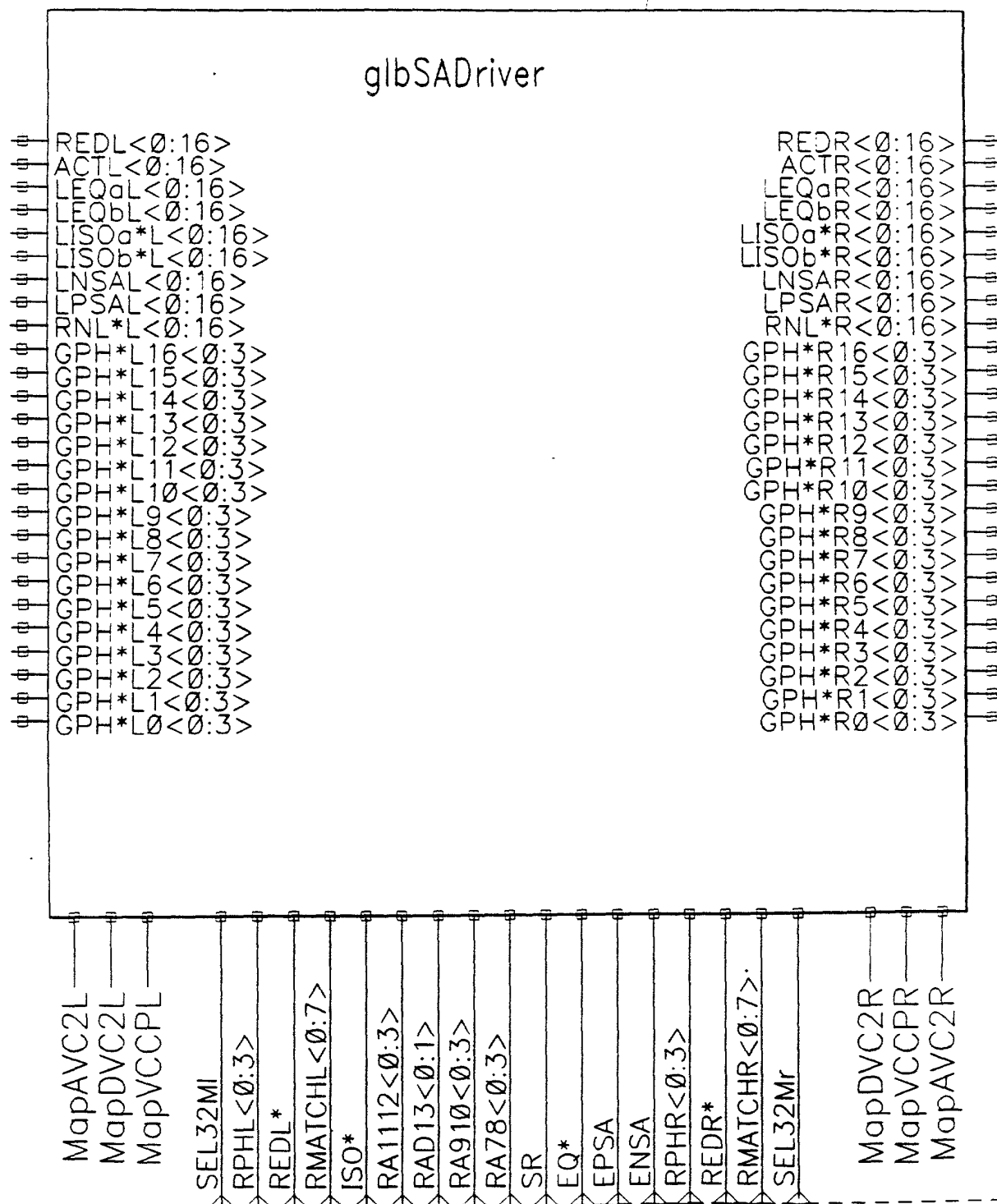


FIG. 3D

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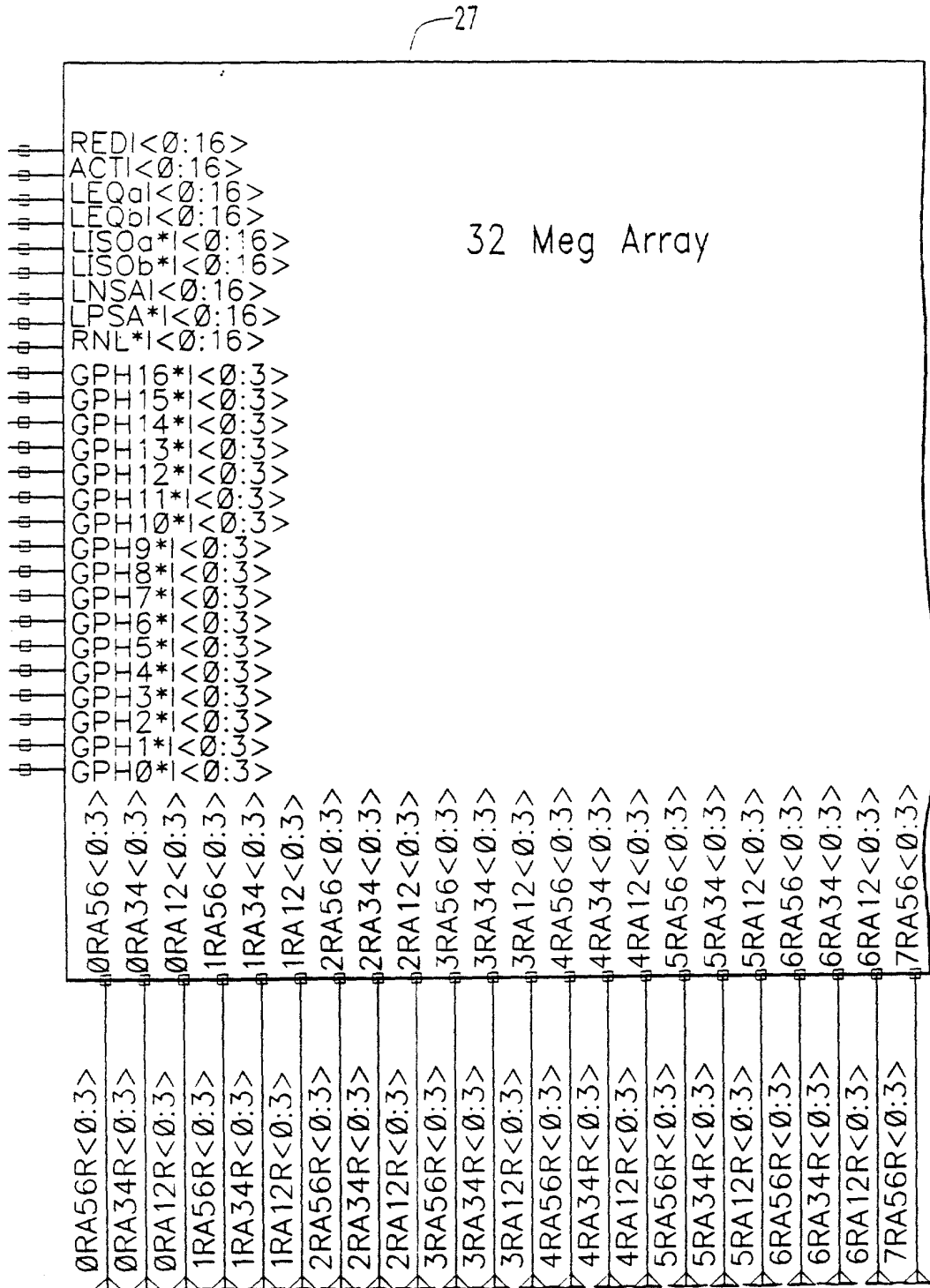
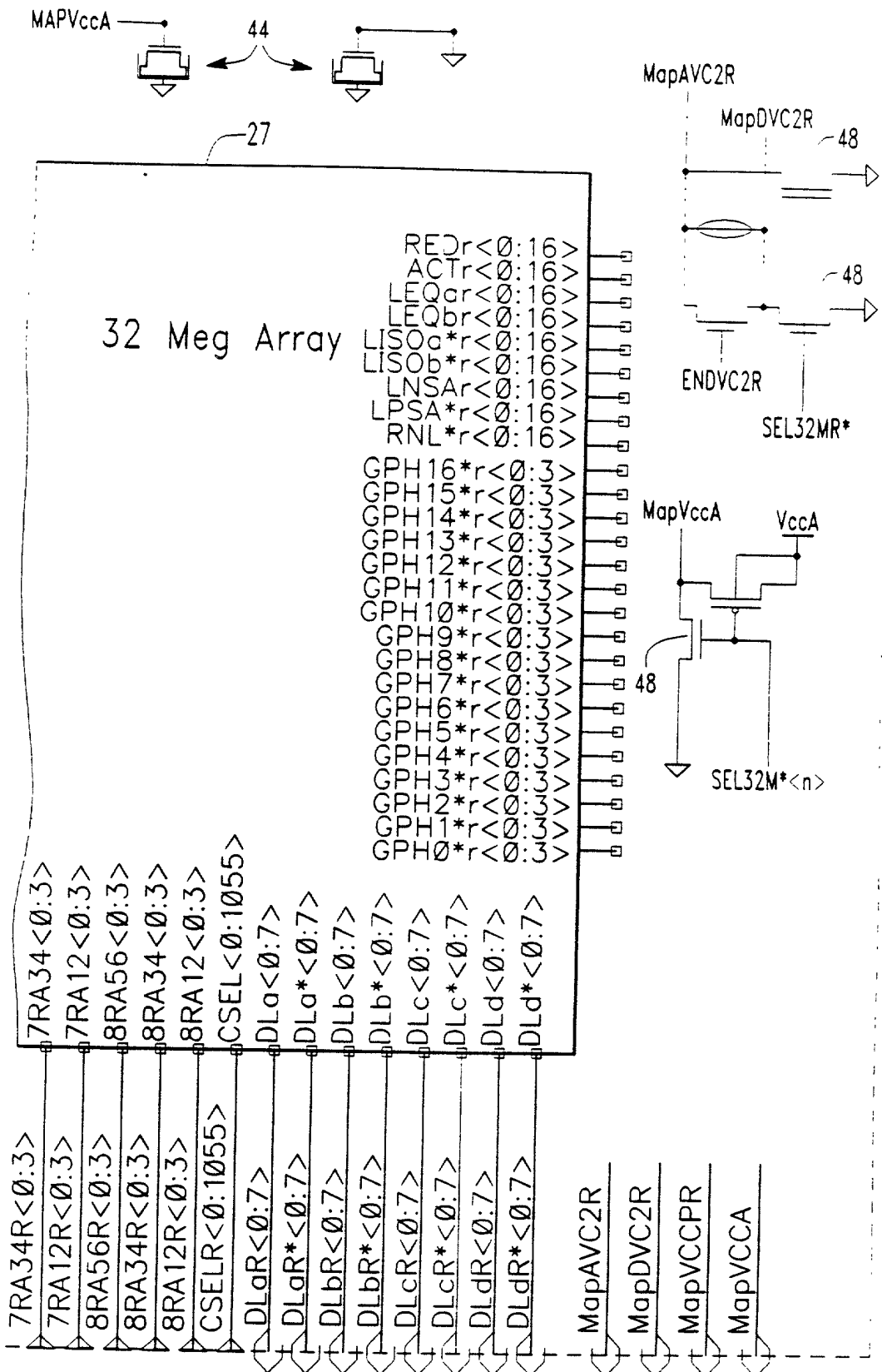


FIG. 3E

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32MEG ARRAY

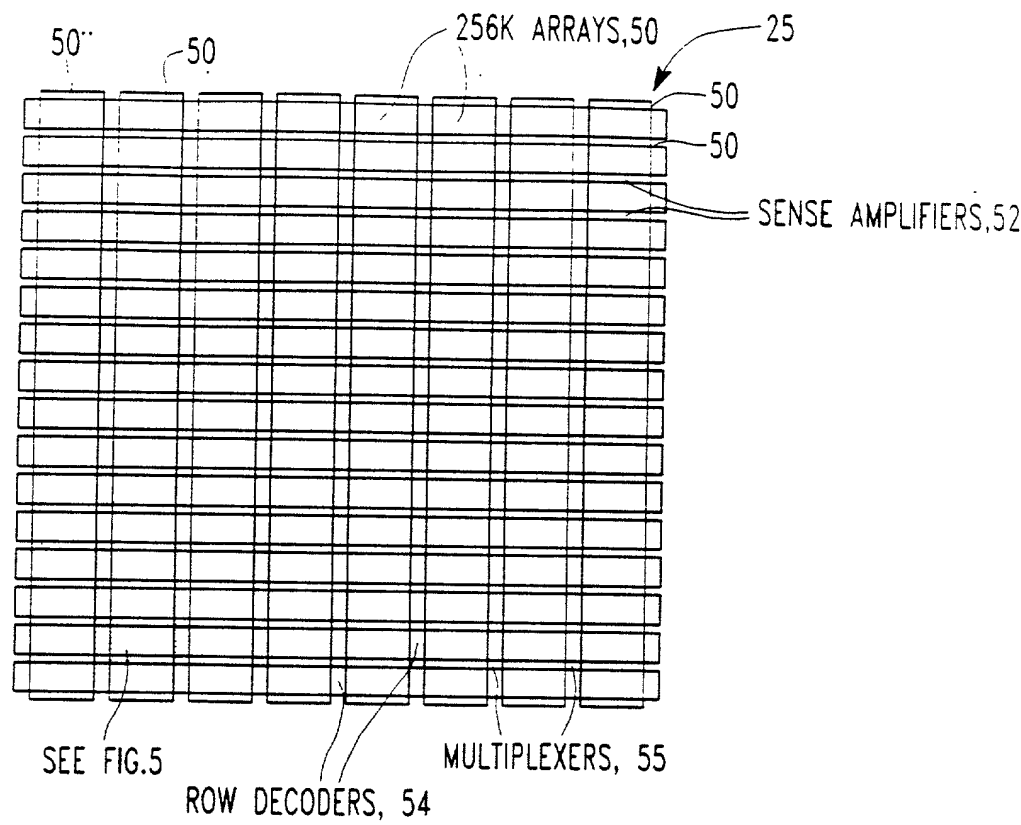


FIG. 4

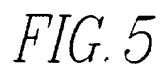


FIG. 5

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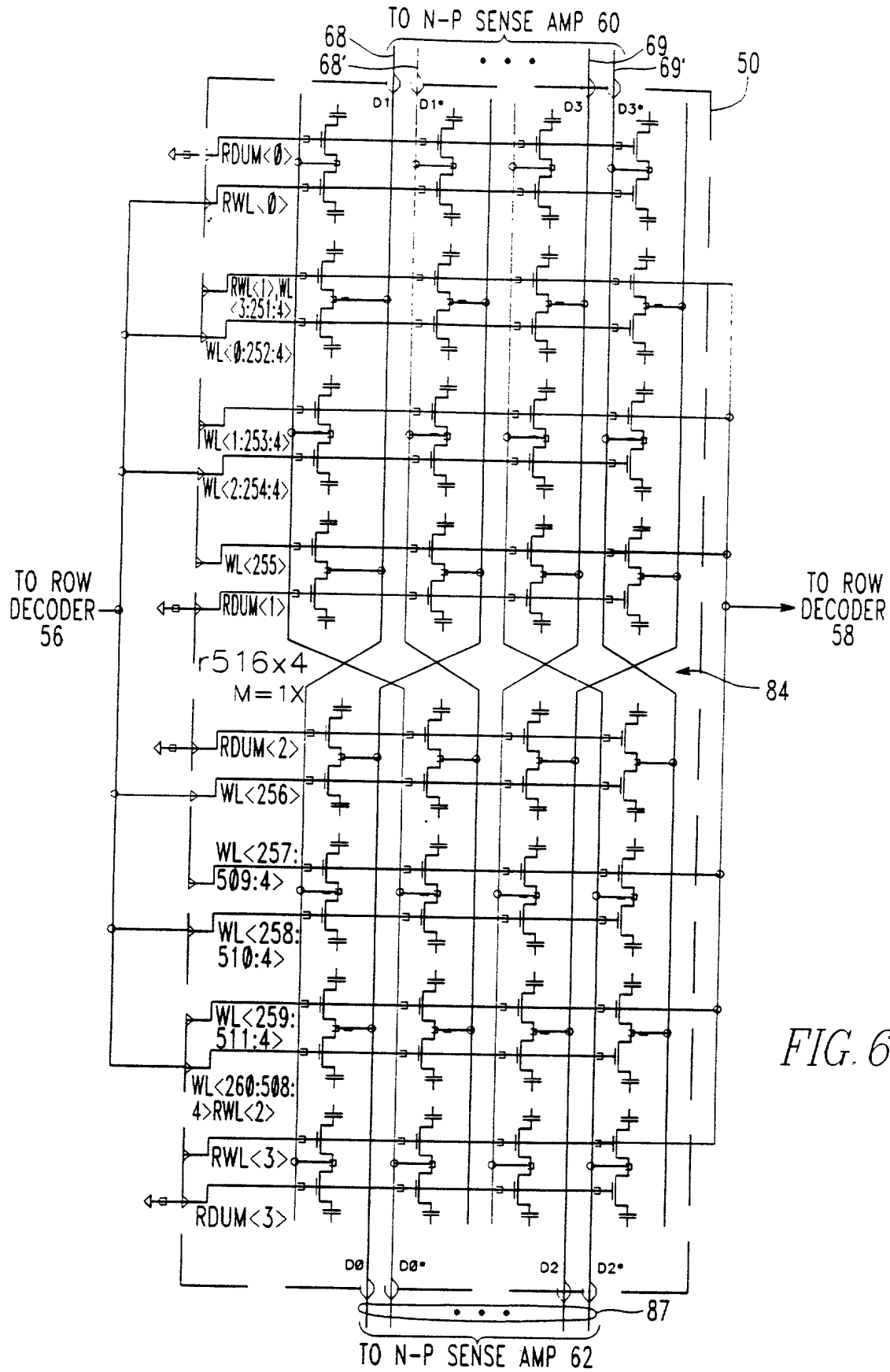


FIG. 6A

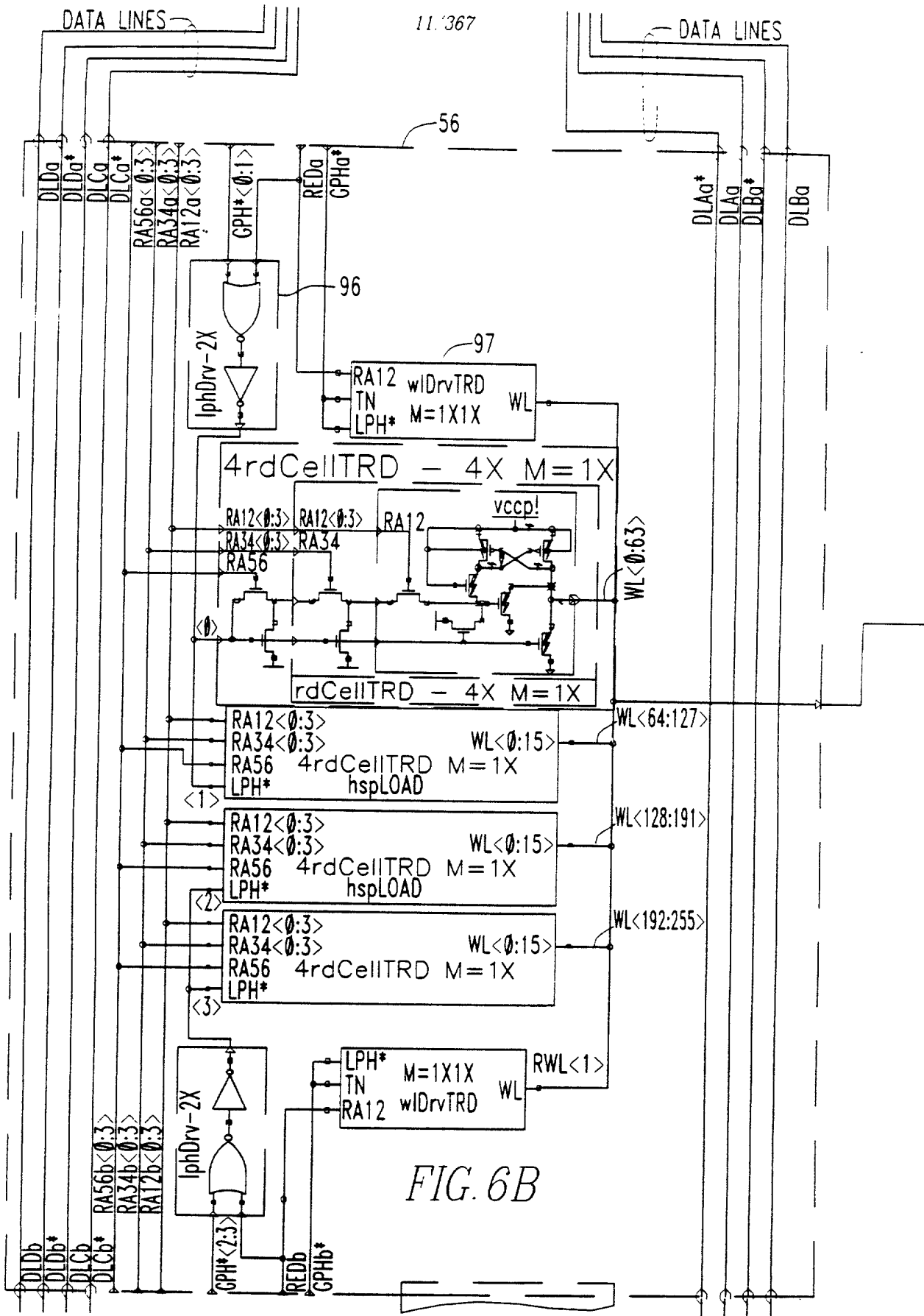
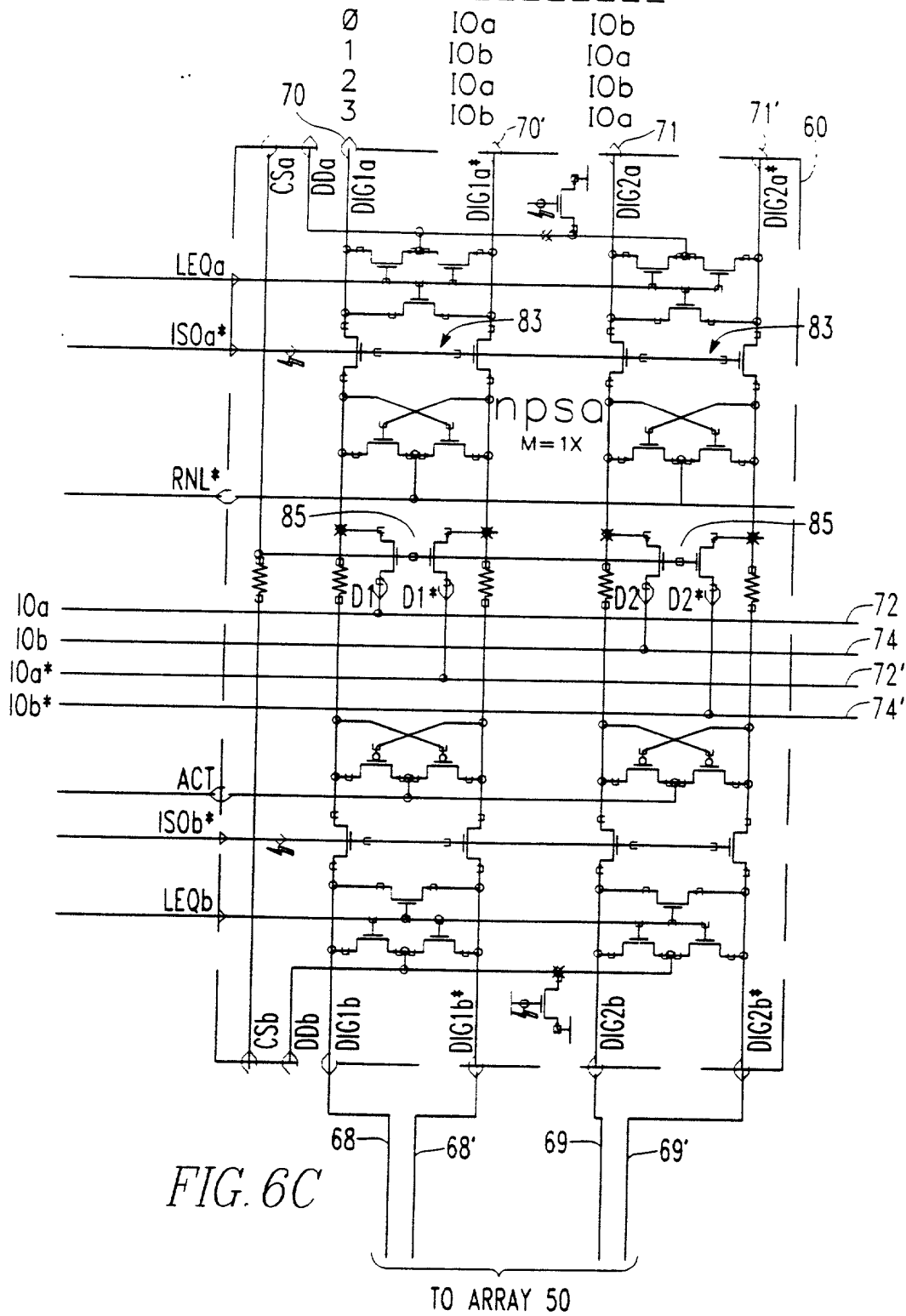


FIG. 6B

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Connections of odd/even
columns to IOa and IOb
alternates with odd/even
column select lines:
CA01* D1(even) D2(odd)



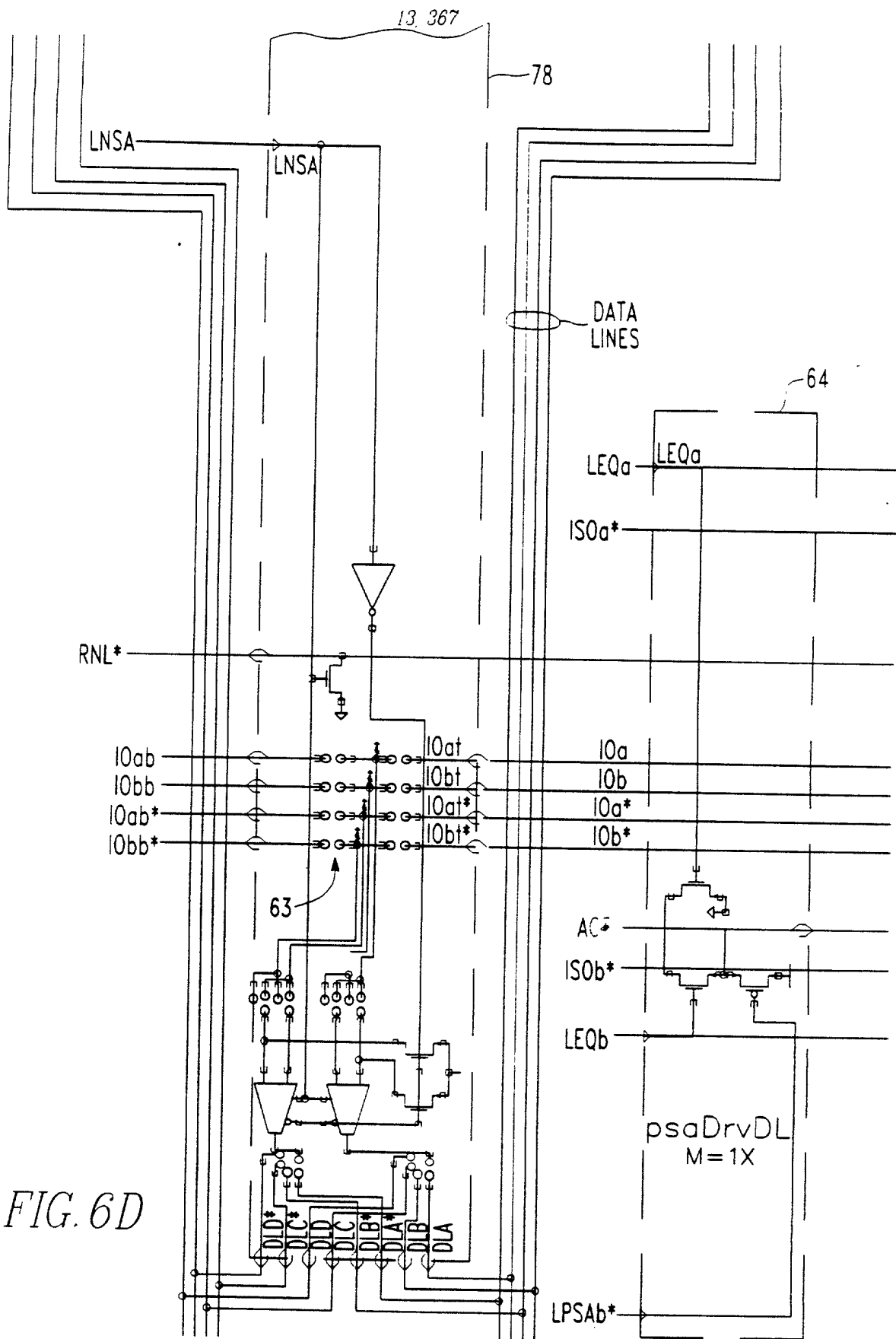


FIG. 6D



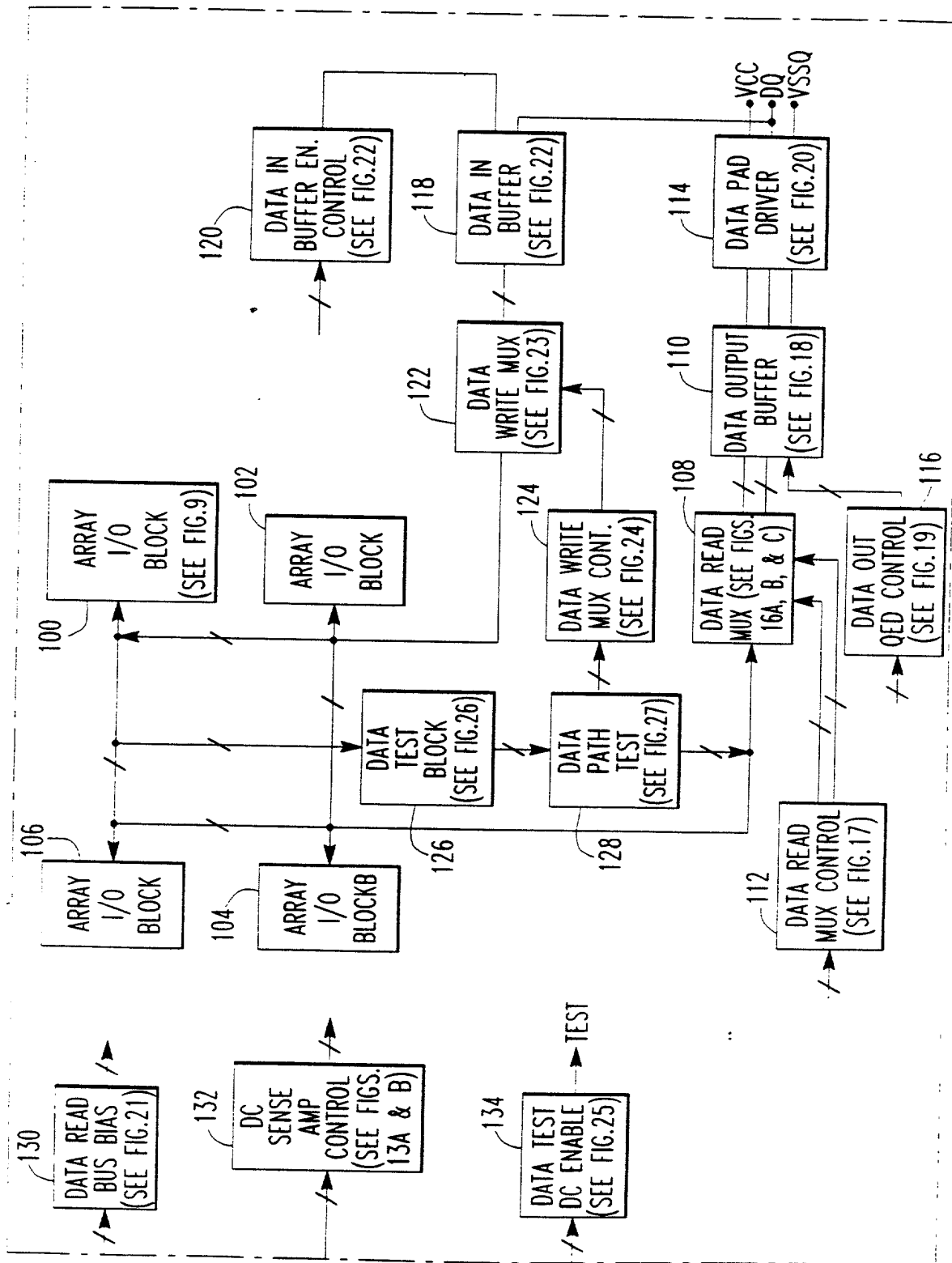


FIG. 8

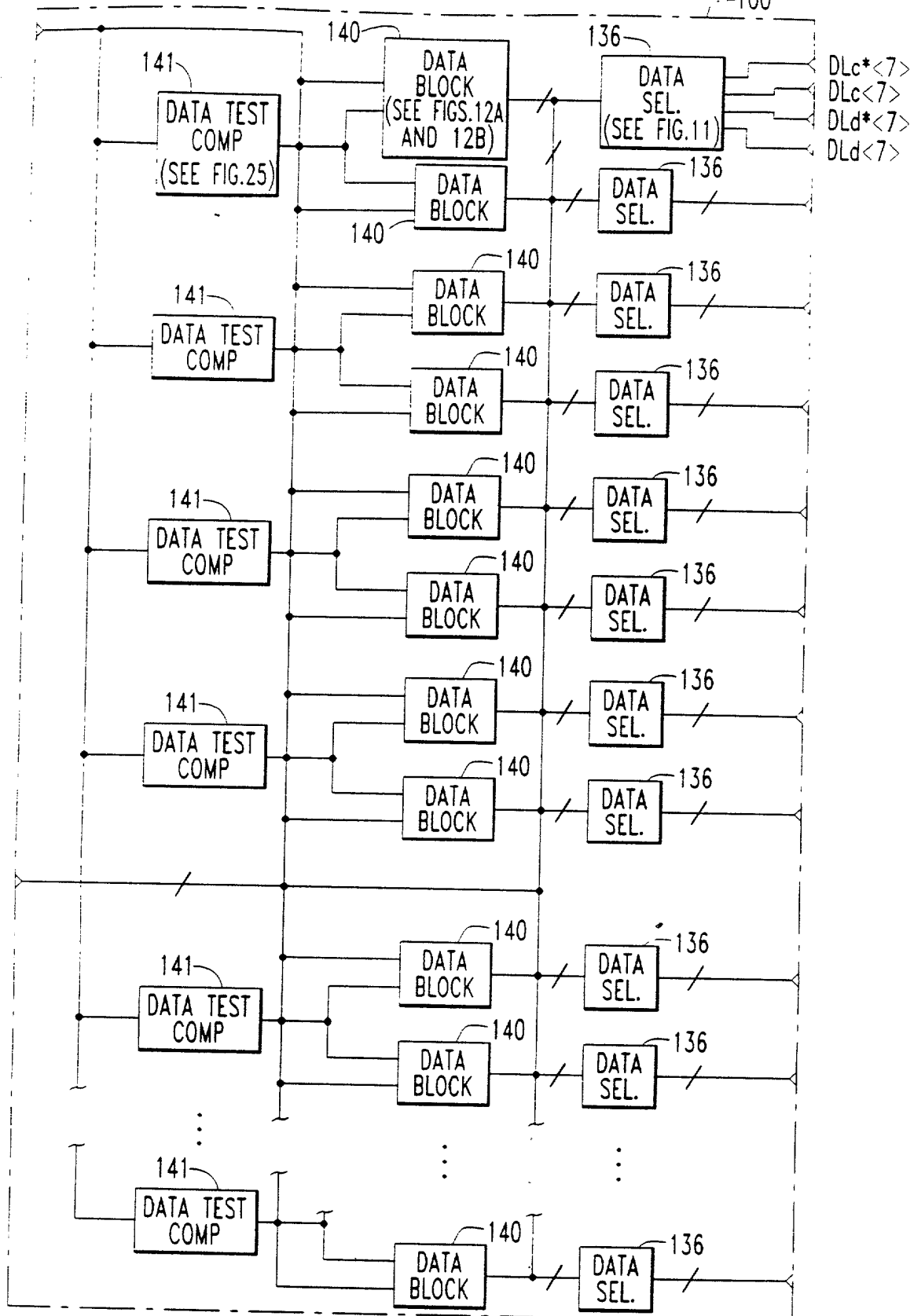
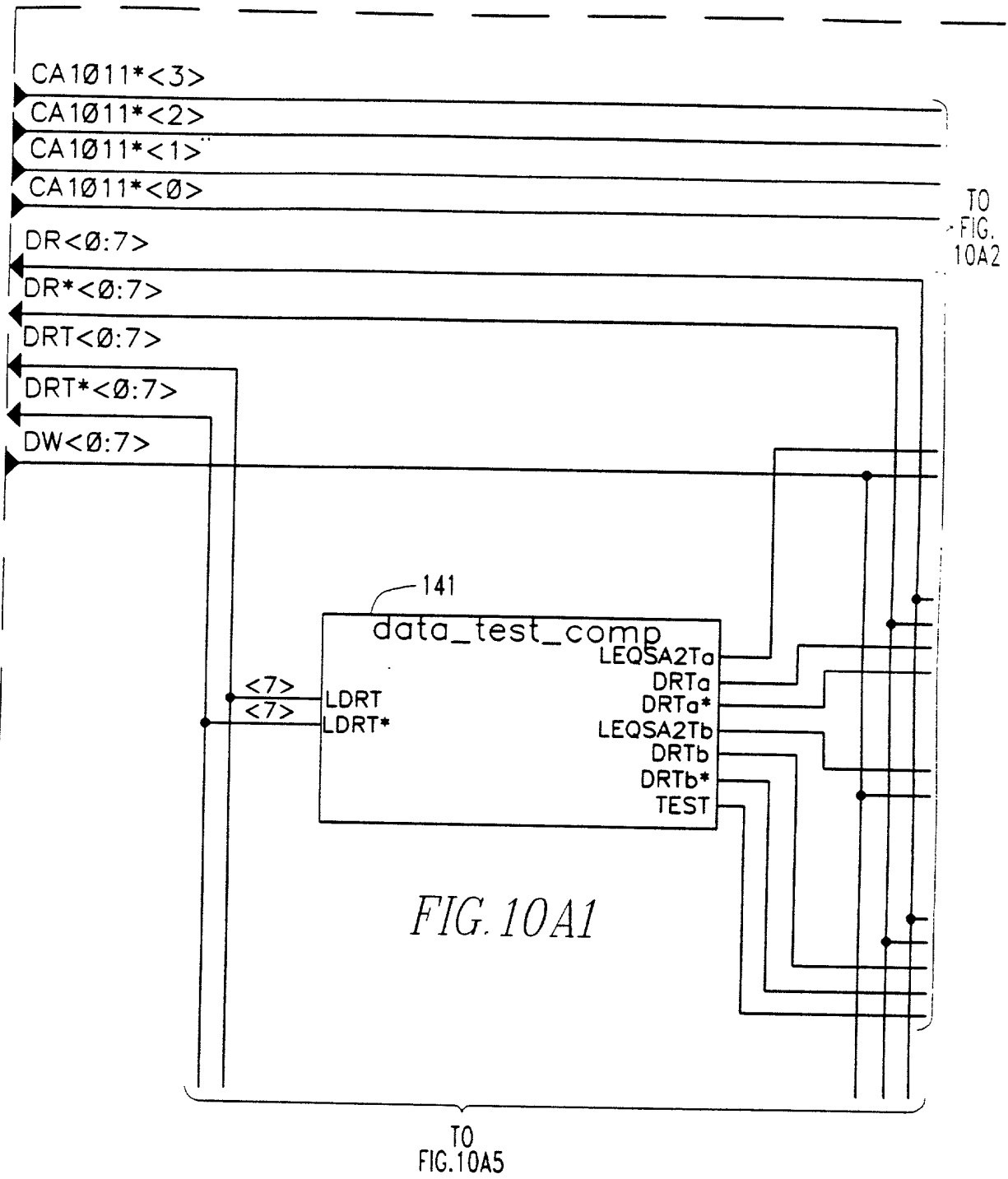


FIG. 9



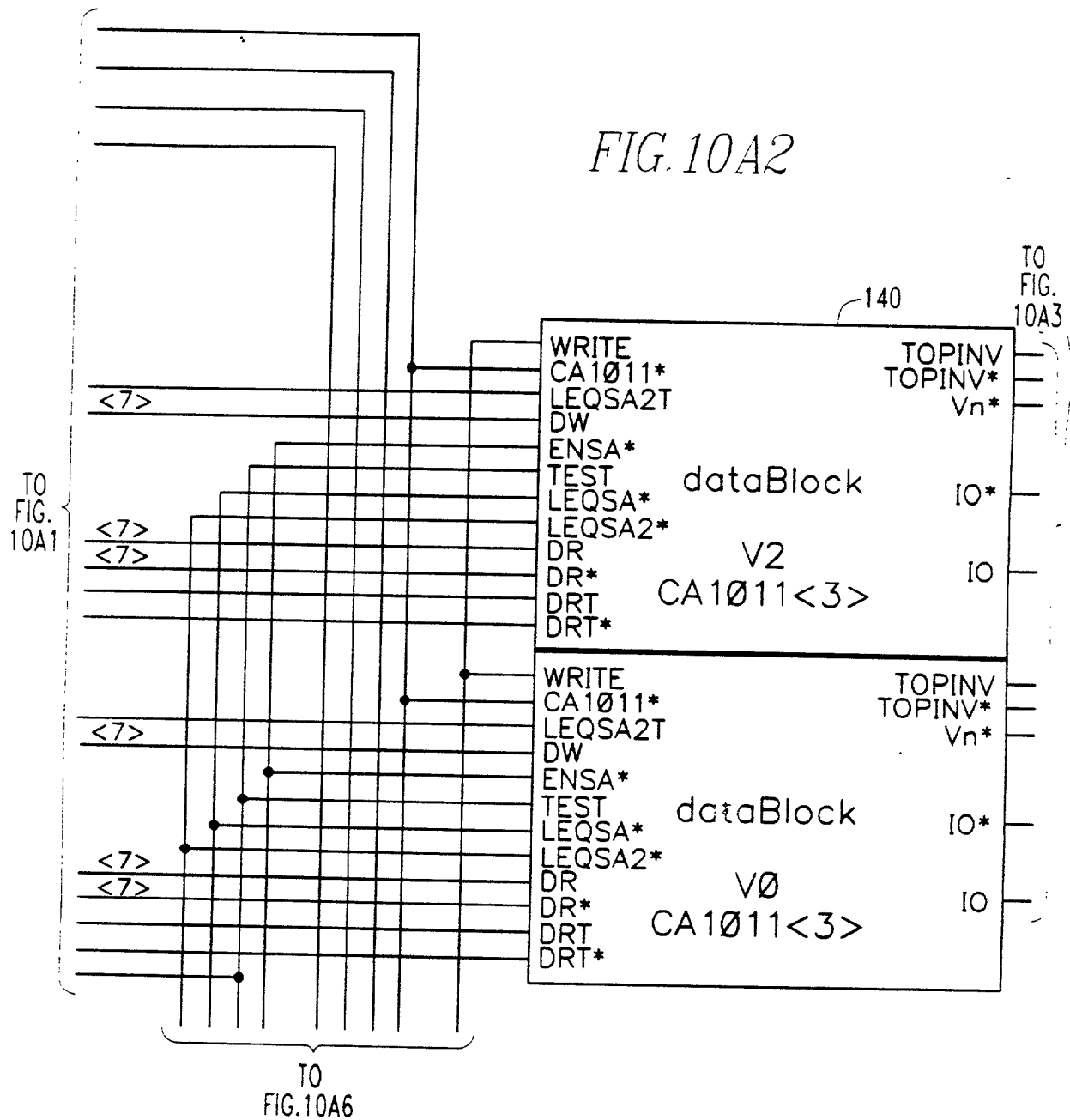
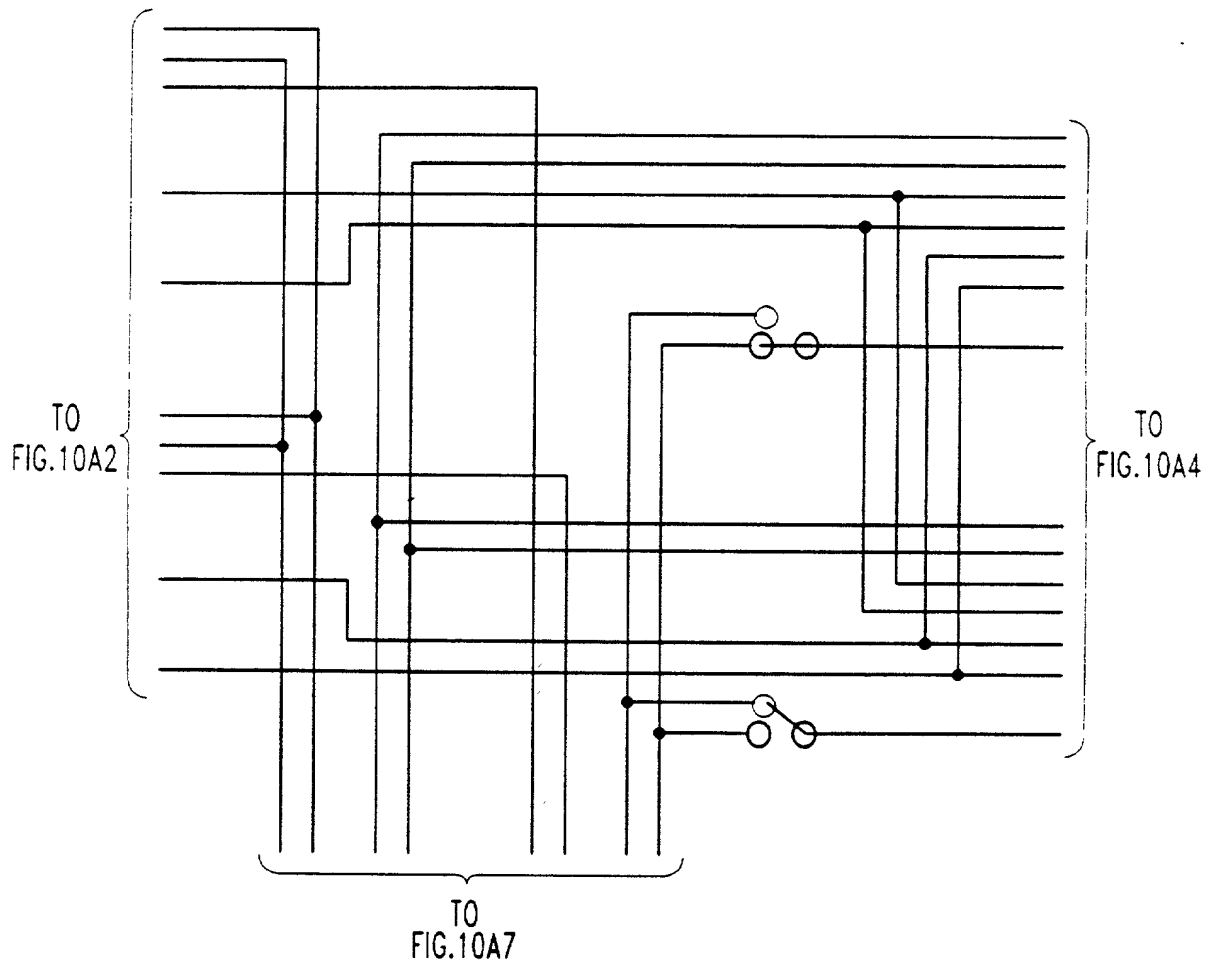


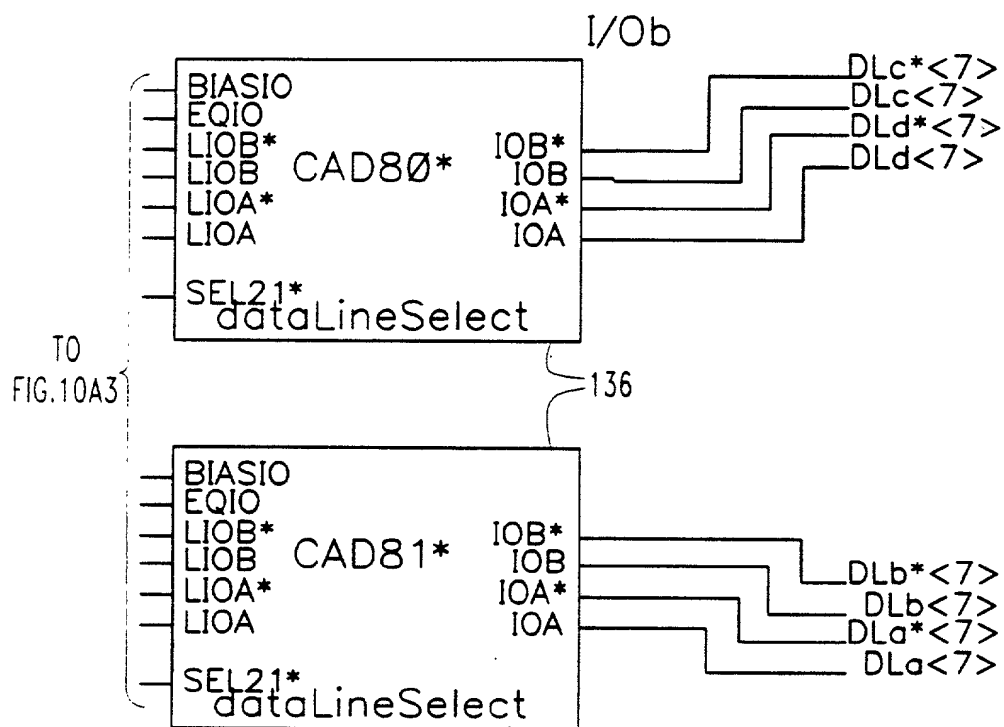
FIG. 10A3



arrayIOBlock

100

FIG. 10A4



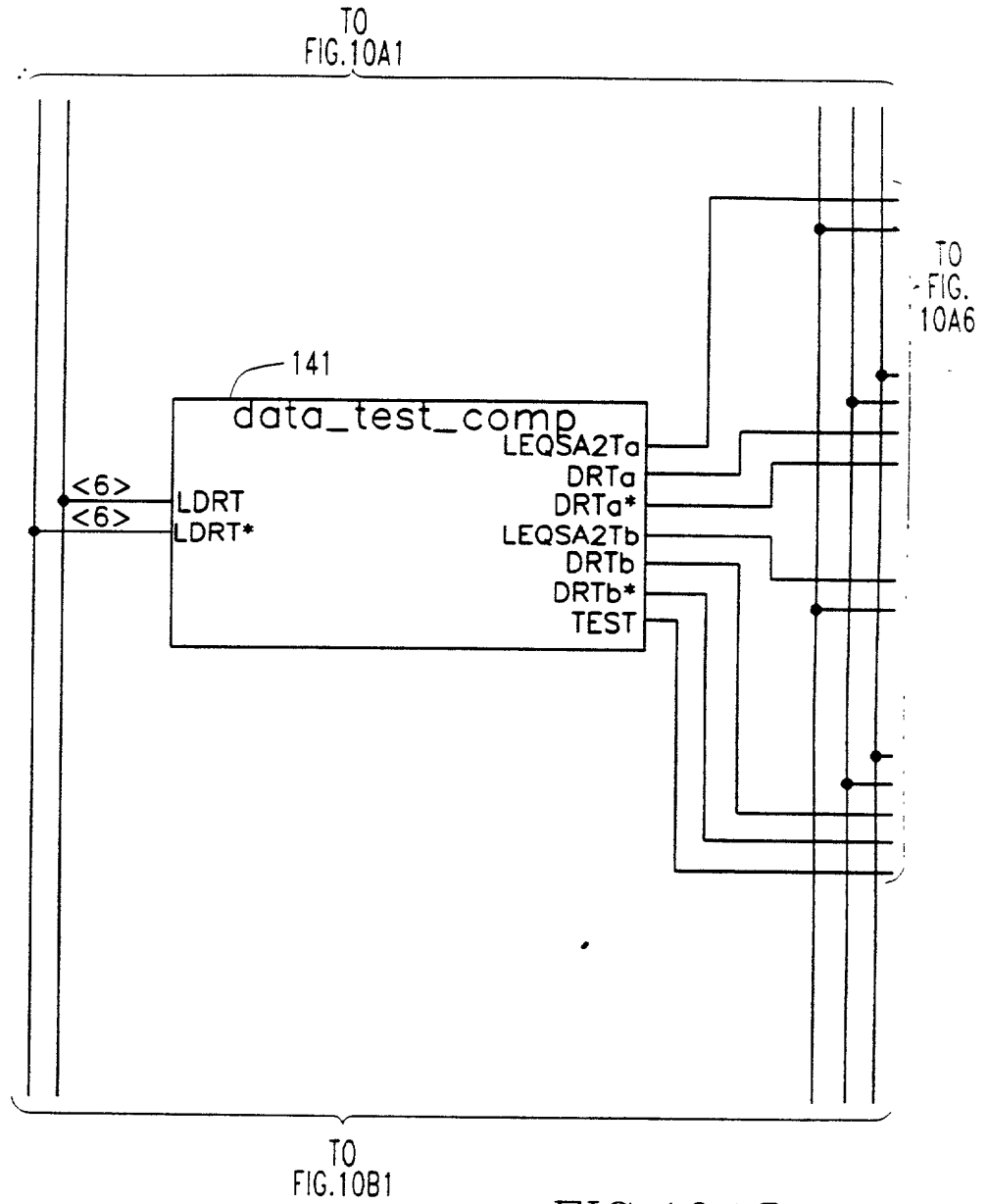


FIG. 10A5

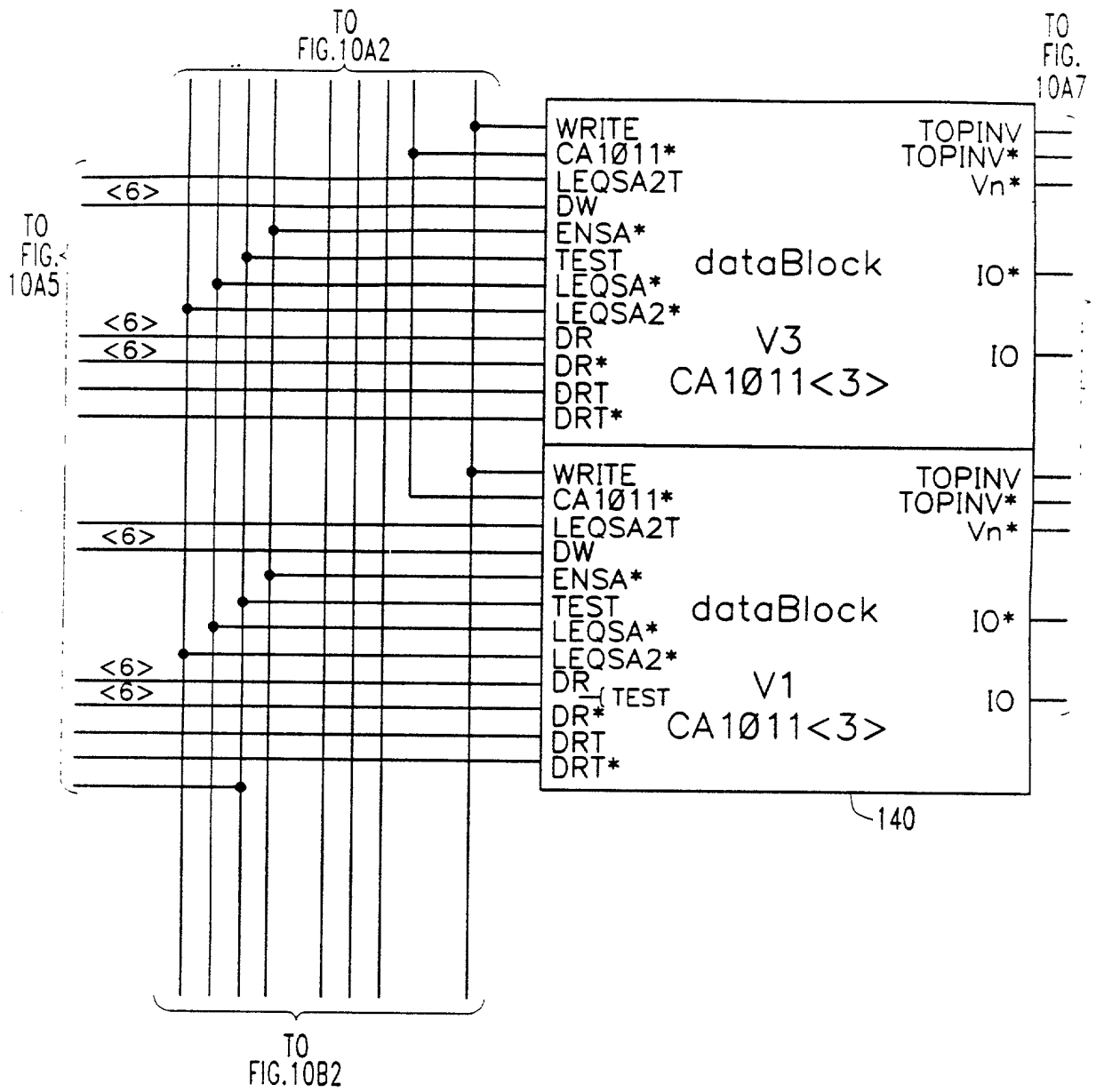


FIG. 10A6

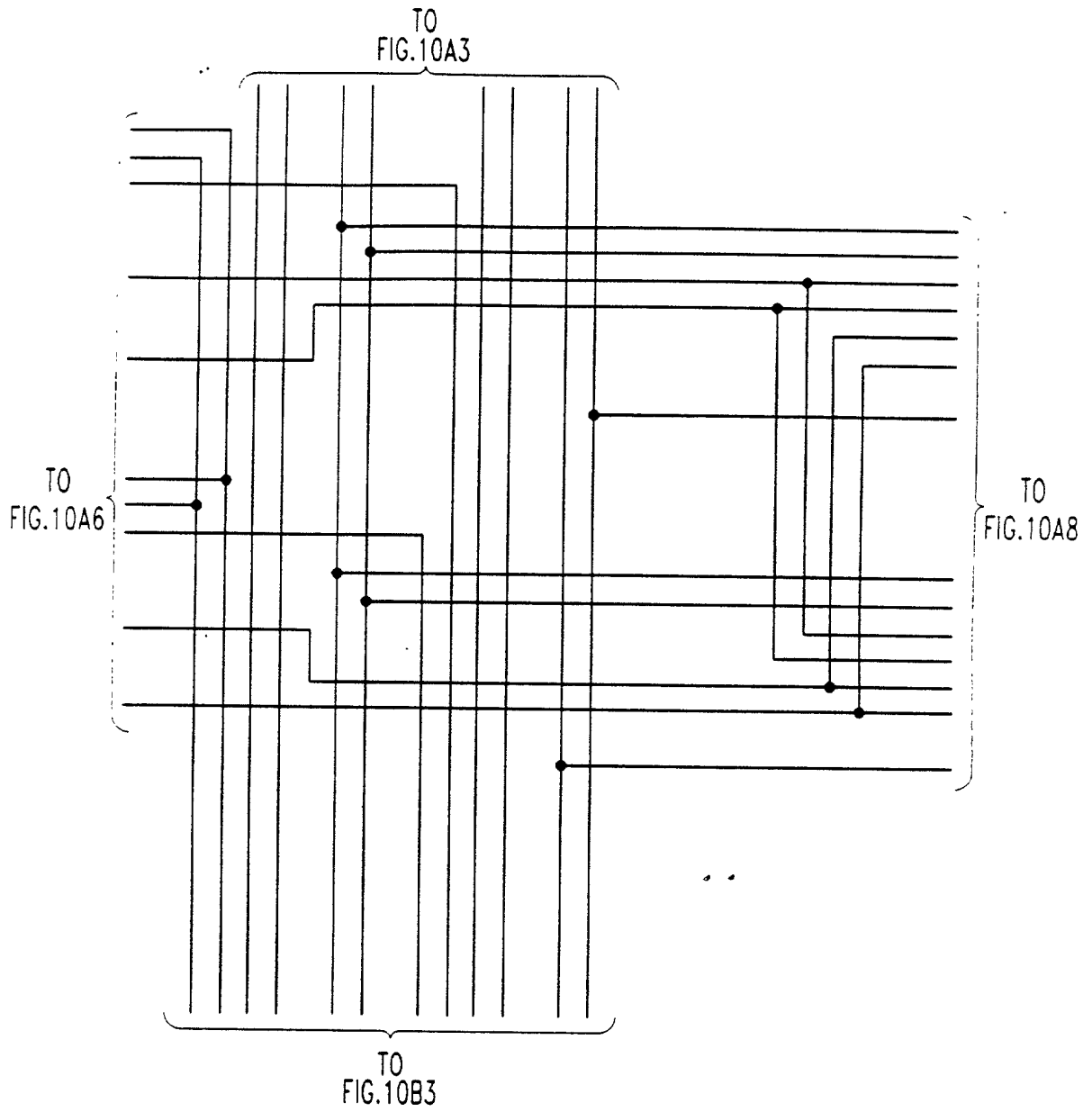


FIG. 10A7

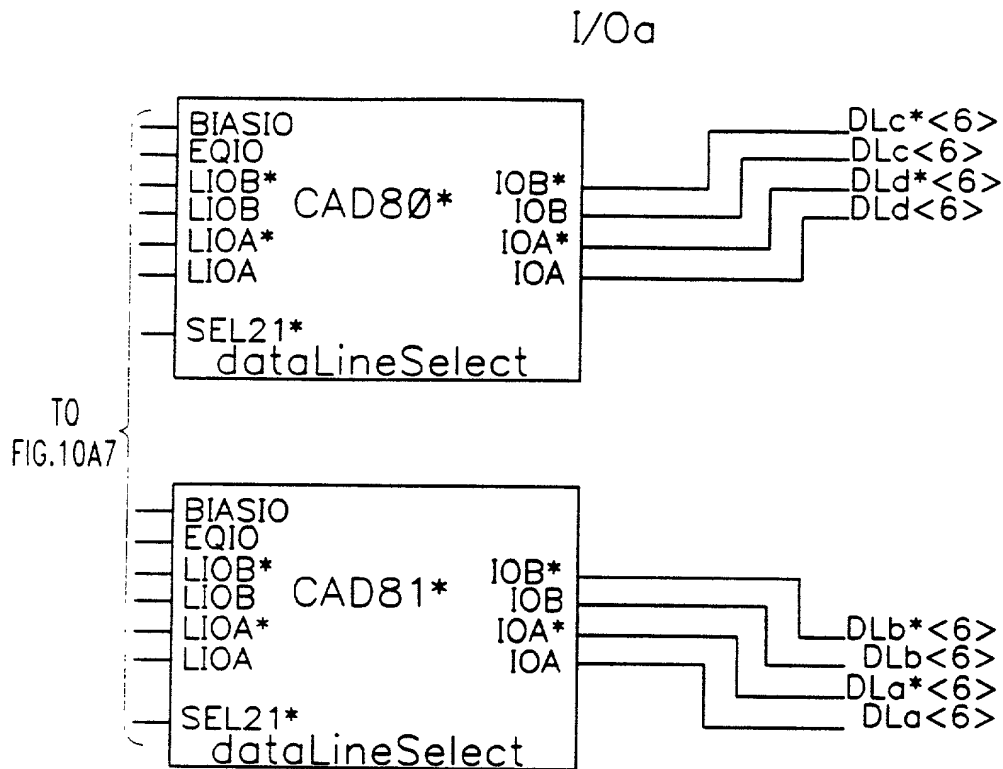


FIG. 10A8

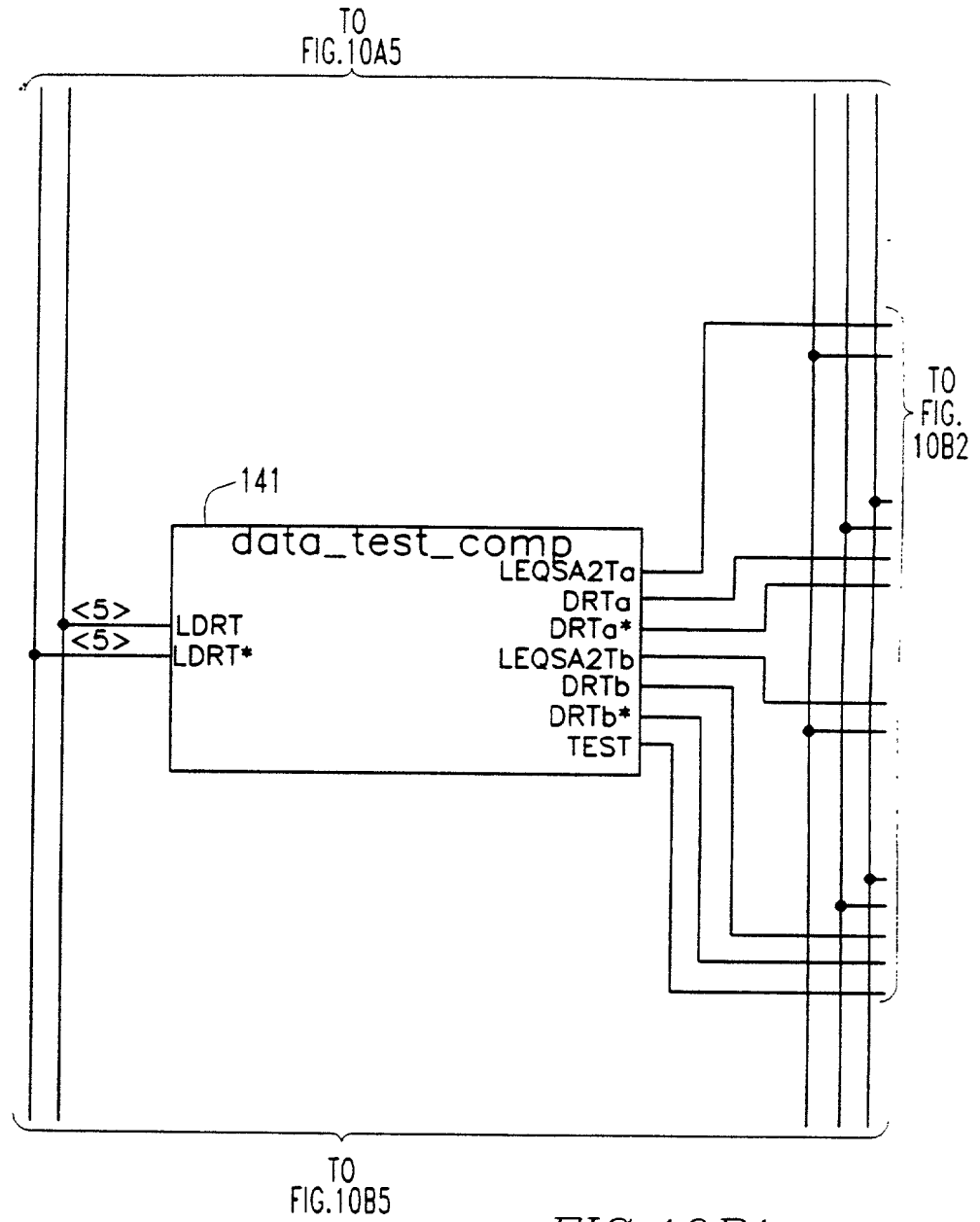
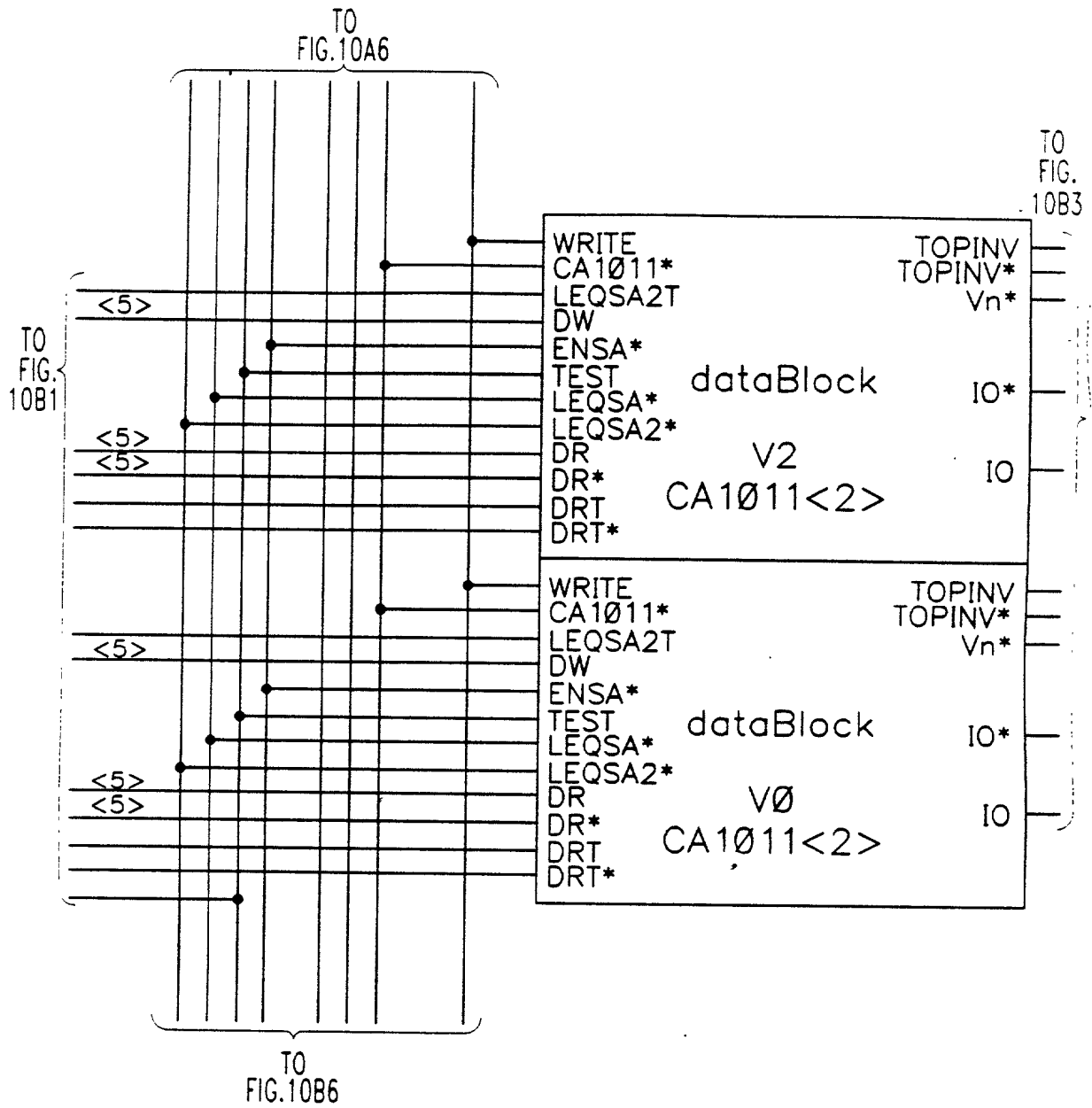


FIG. 10B1



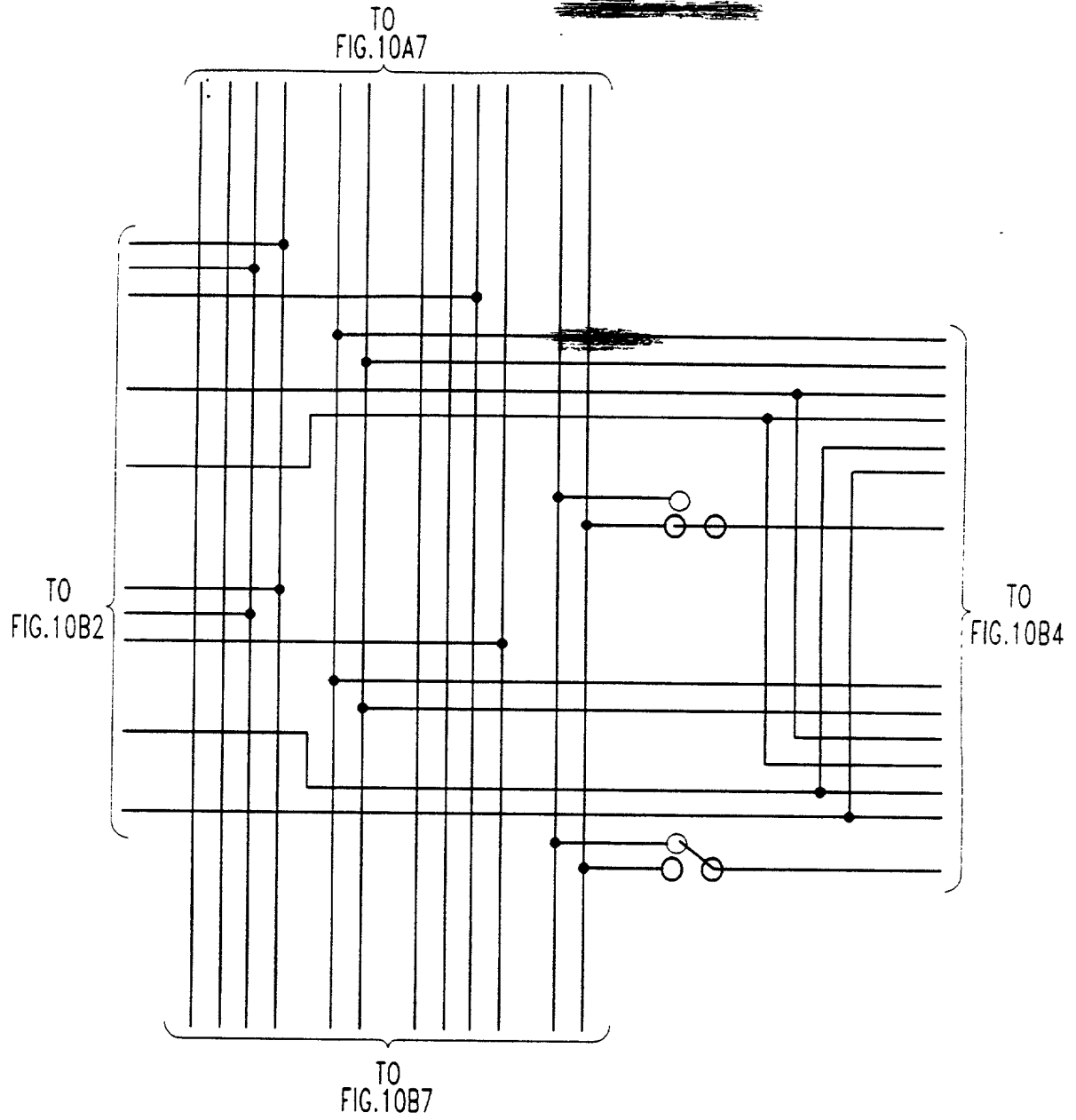


FIG. 10B3

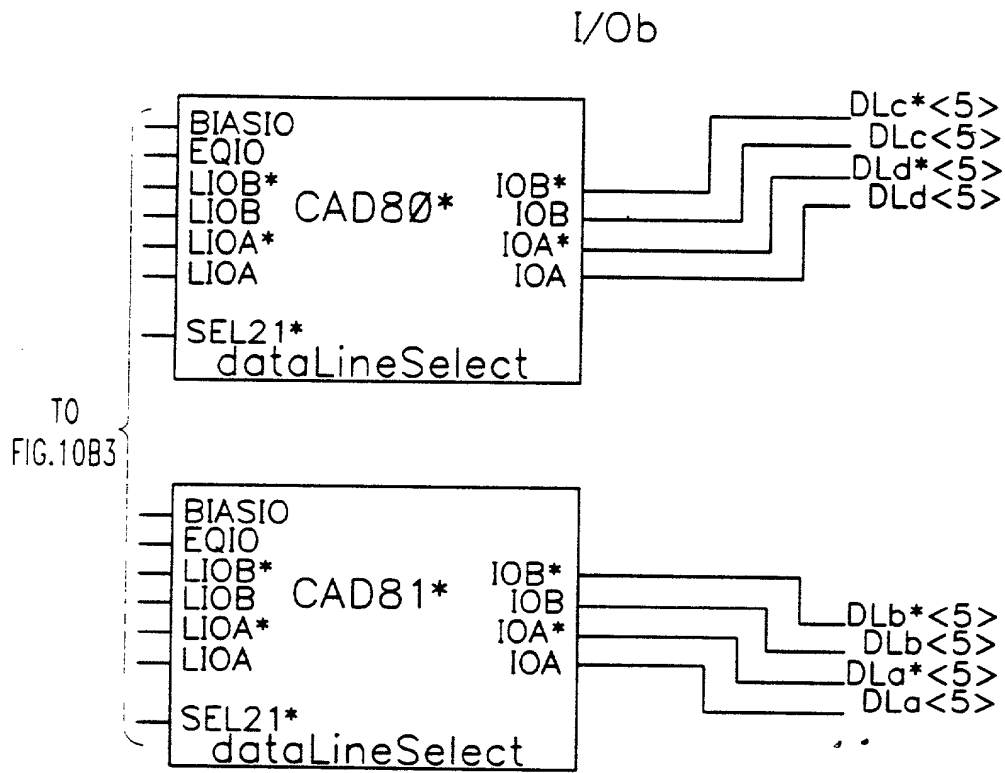


FIG.10B4

FIG. 10B5

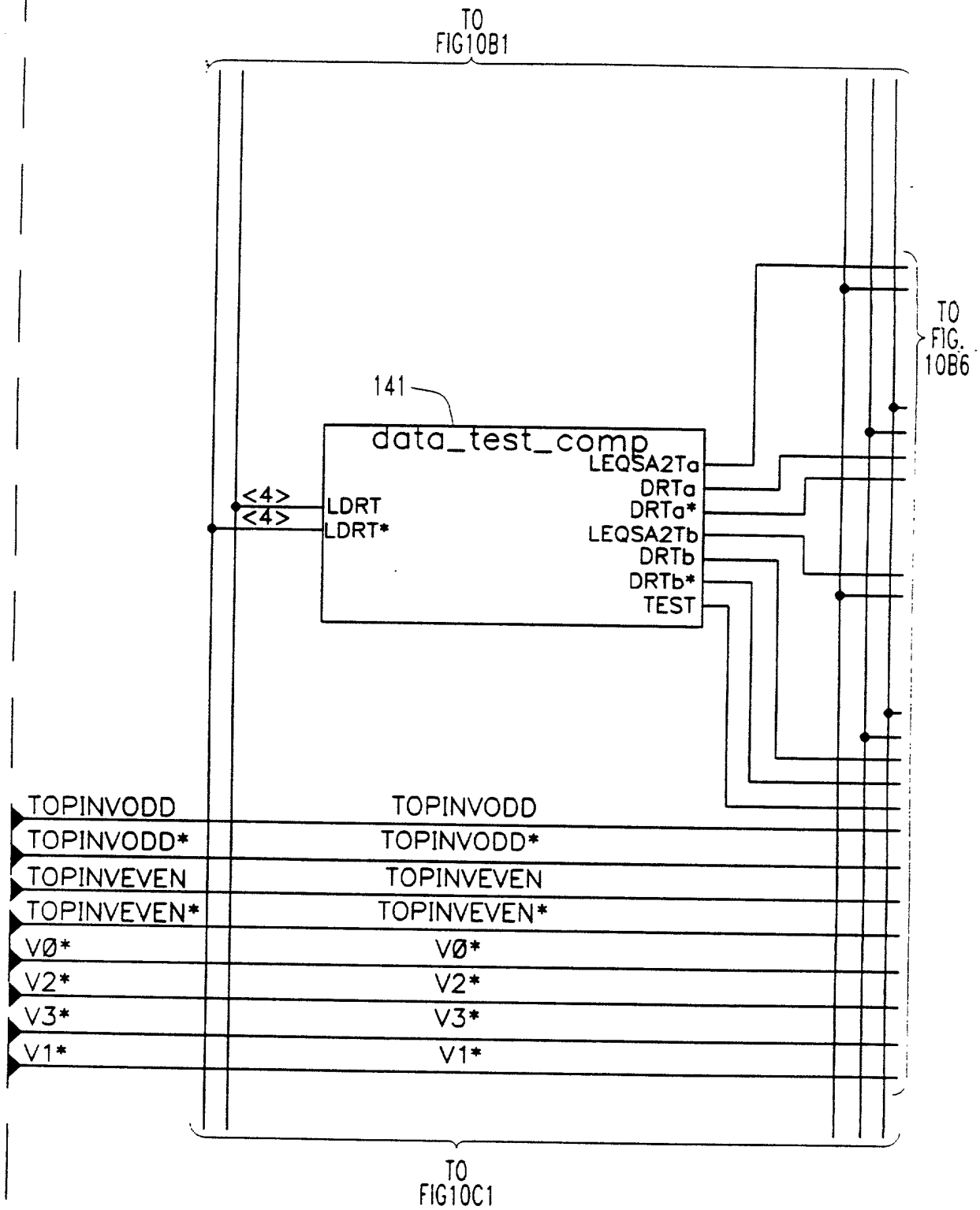


FIG. 10B6

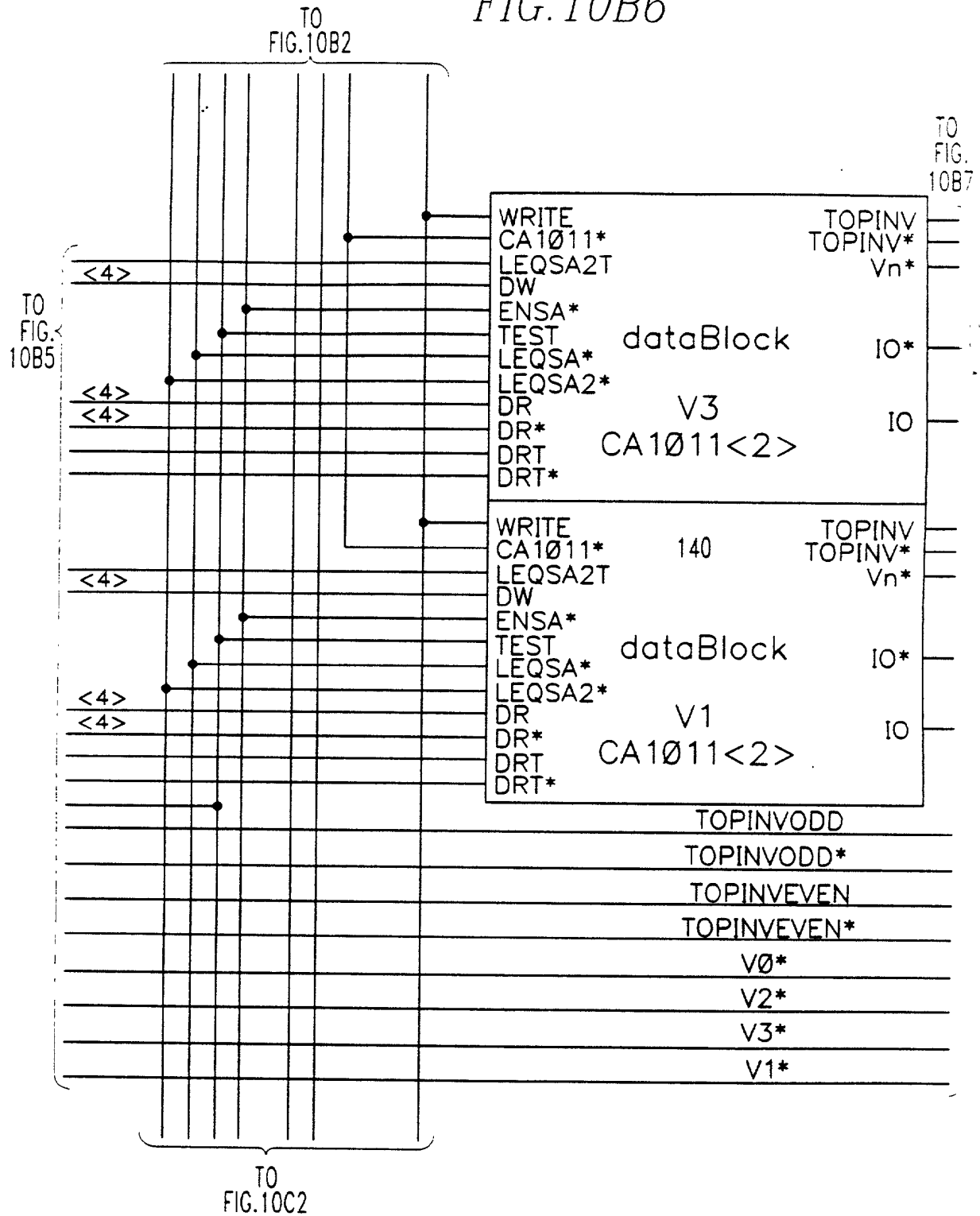


FIG. 10B7

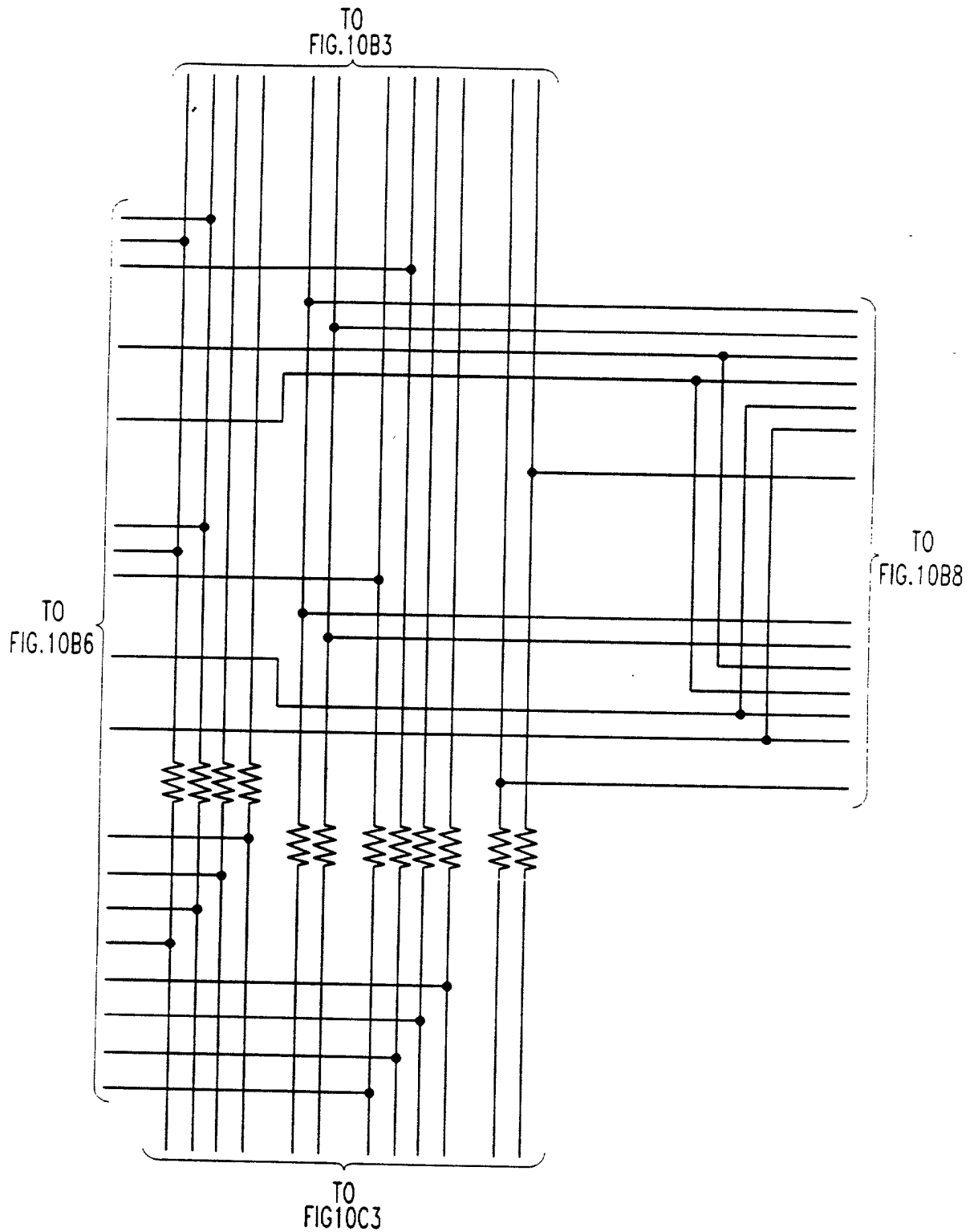
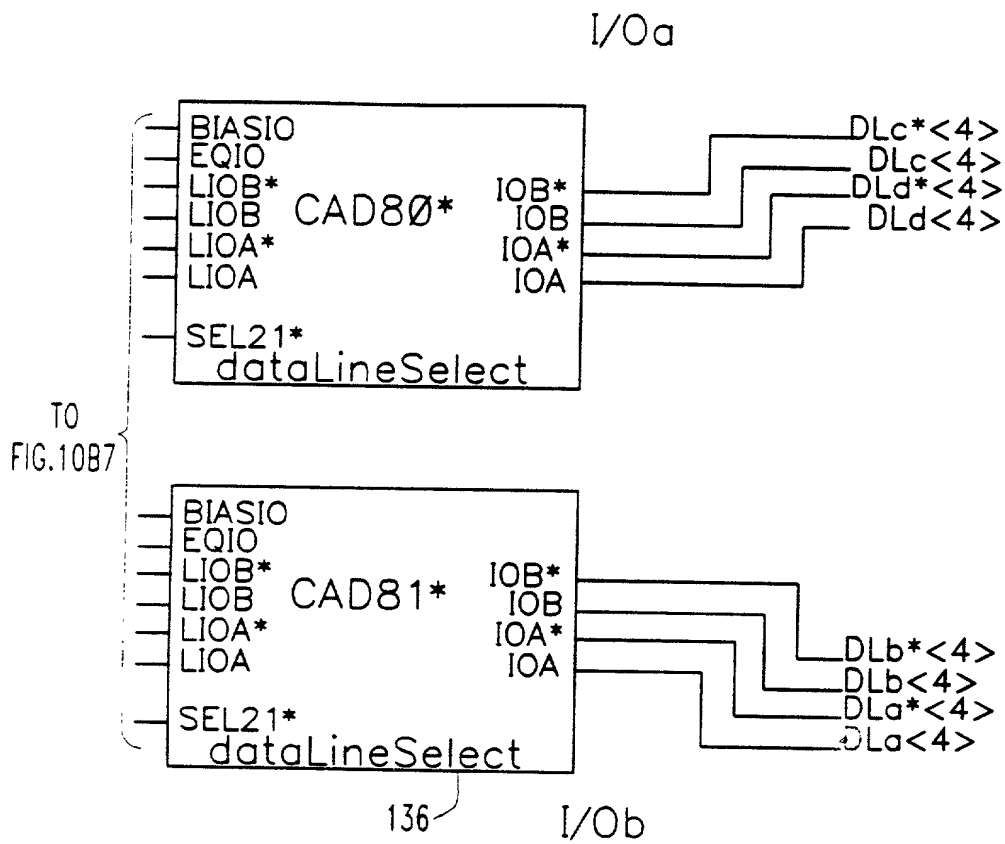
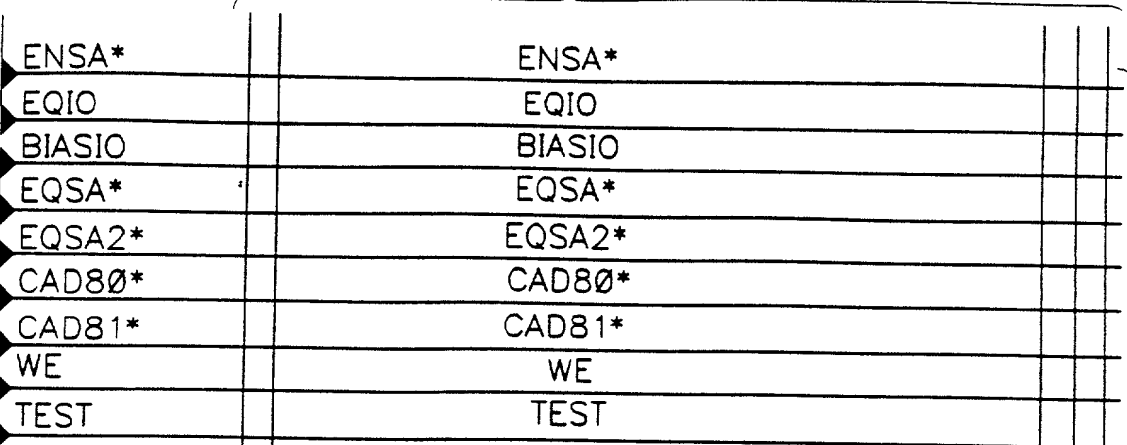


FIG. 10B8

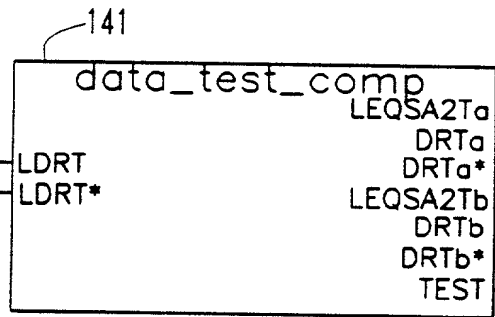


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TO
FIG.10B5



TO
FIG.
10C2



TO
FIG.10C5

FIG.10C1

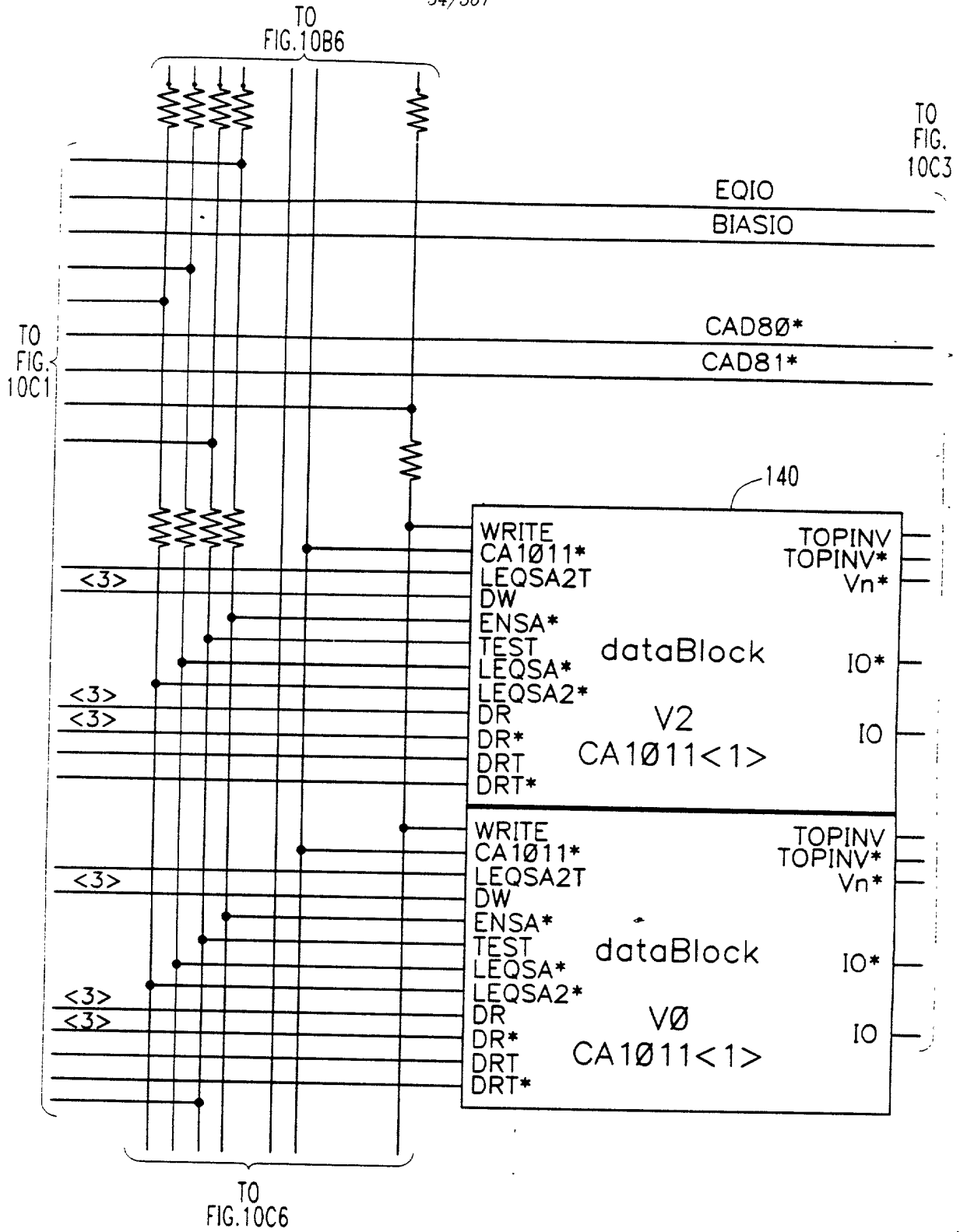


FIG. 10C2

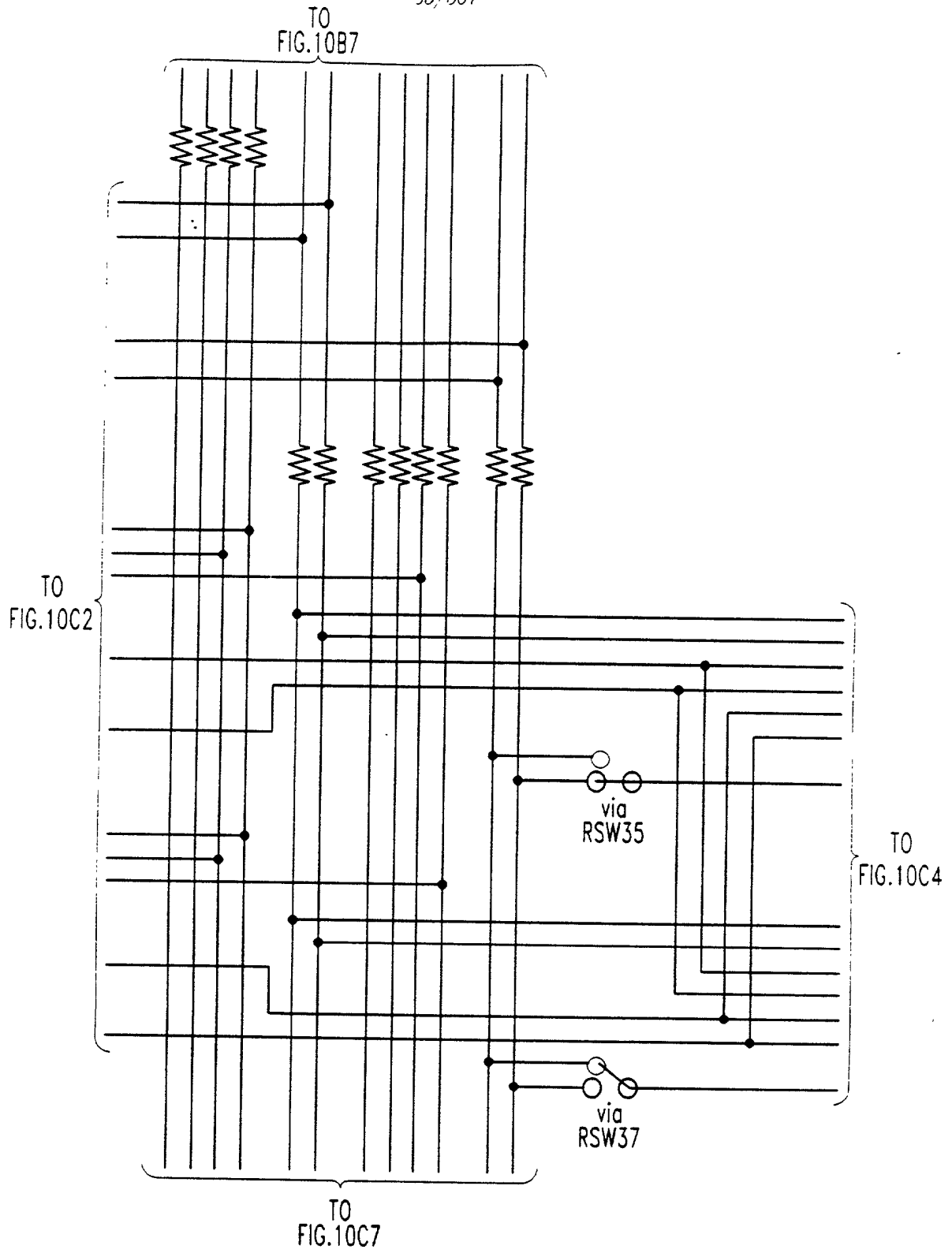
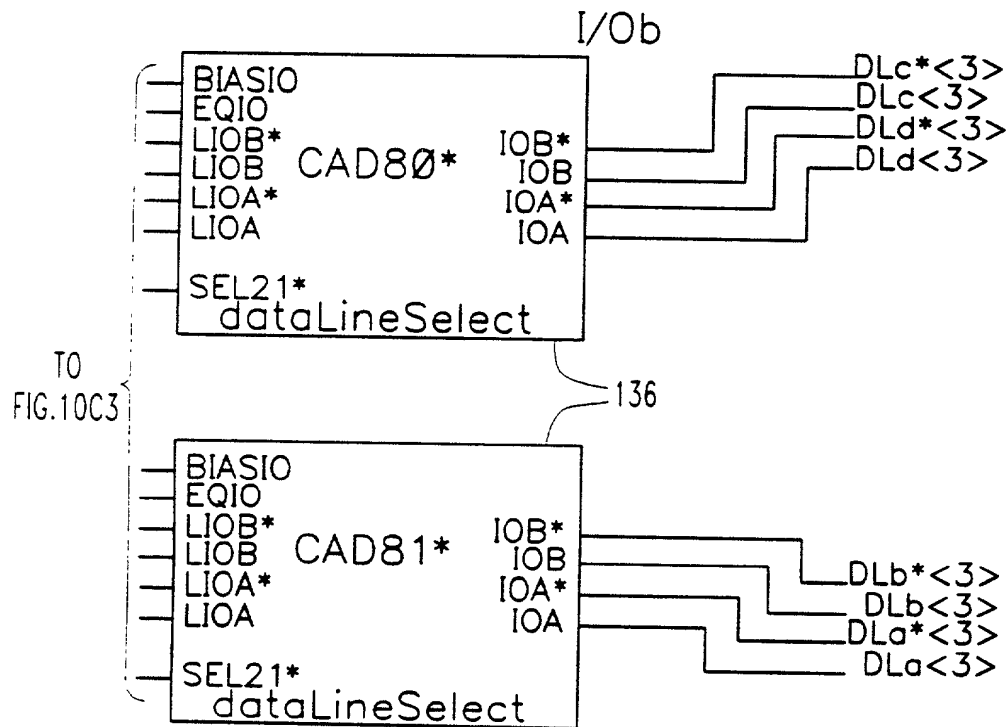


FIG. 10C3

FIG. 10C4



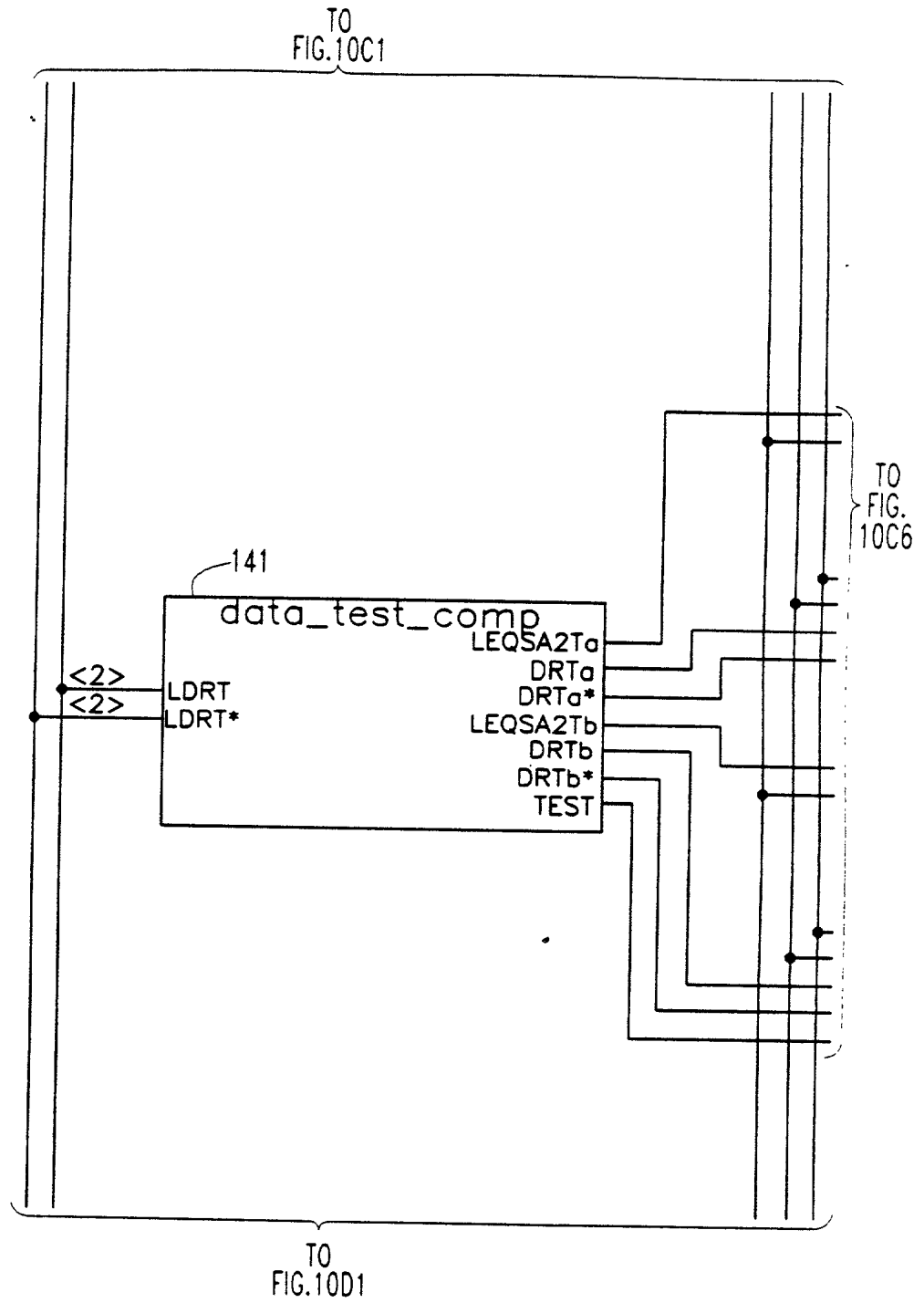


FIG. 10C5

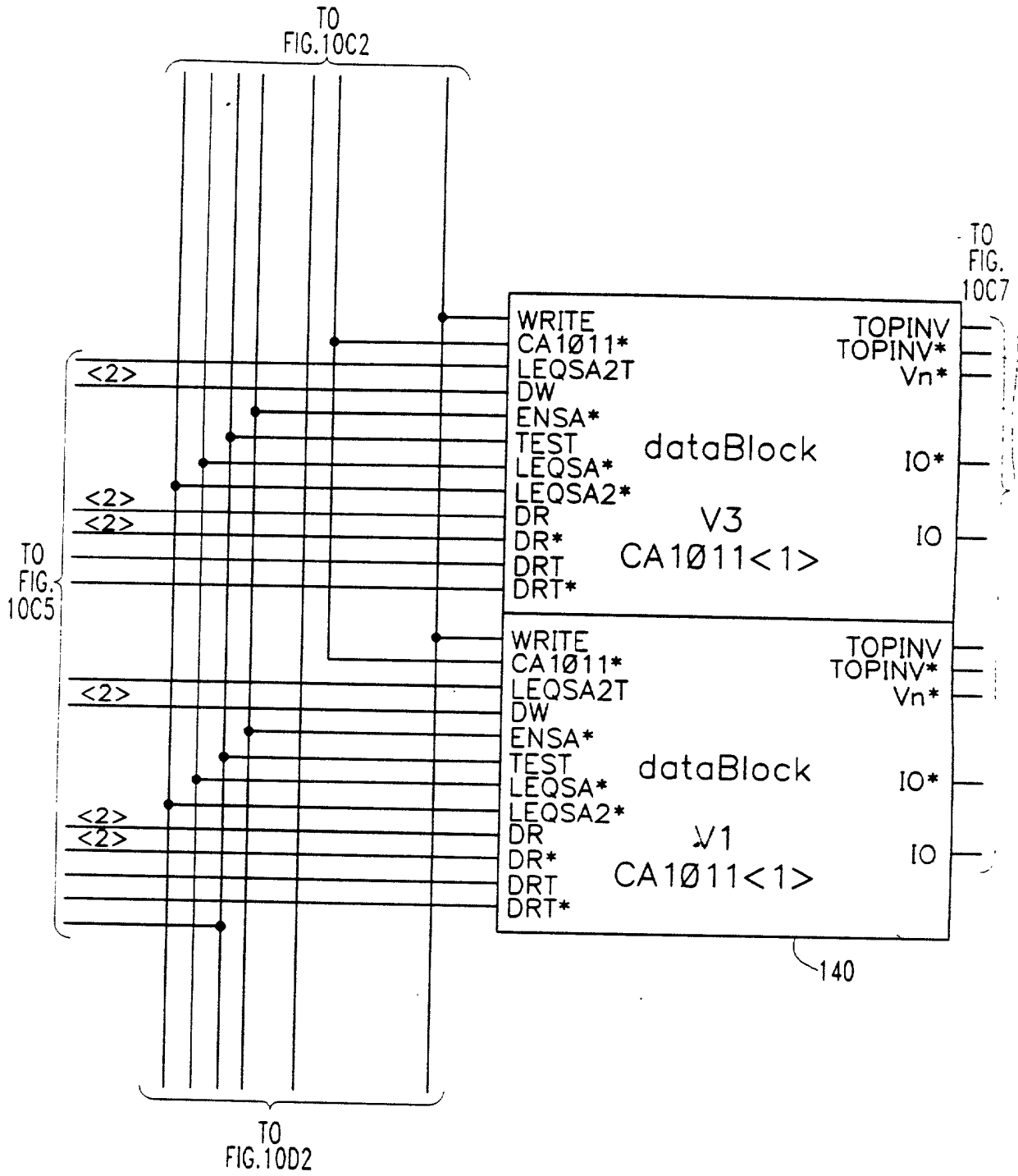


FIG. 10C6

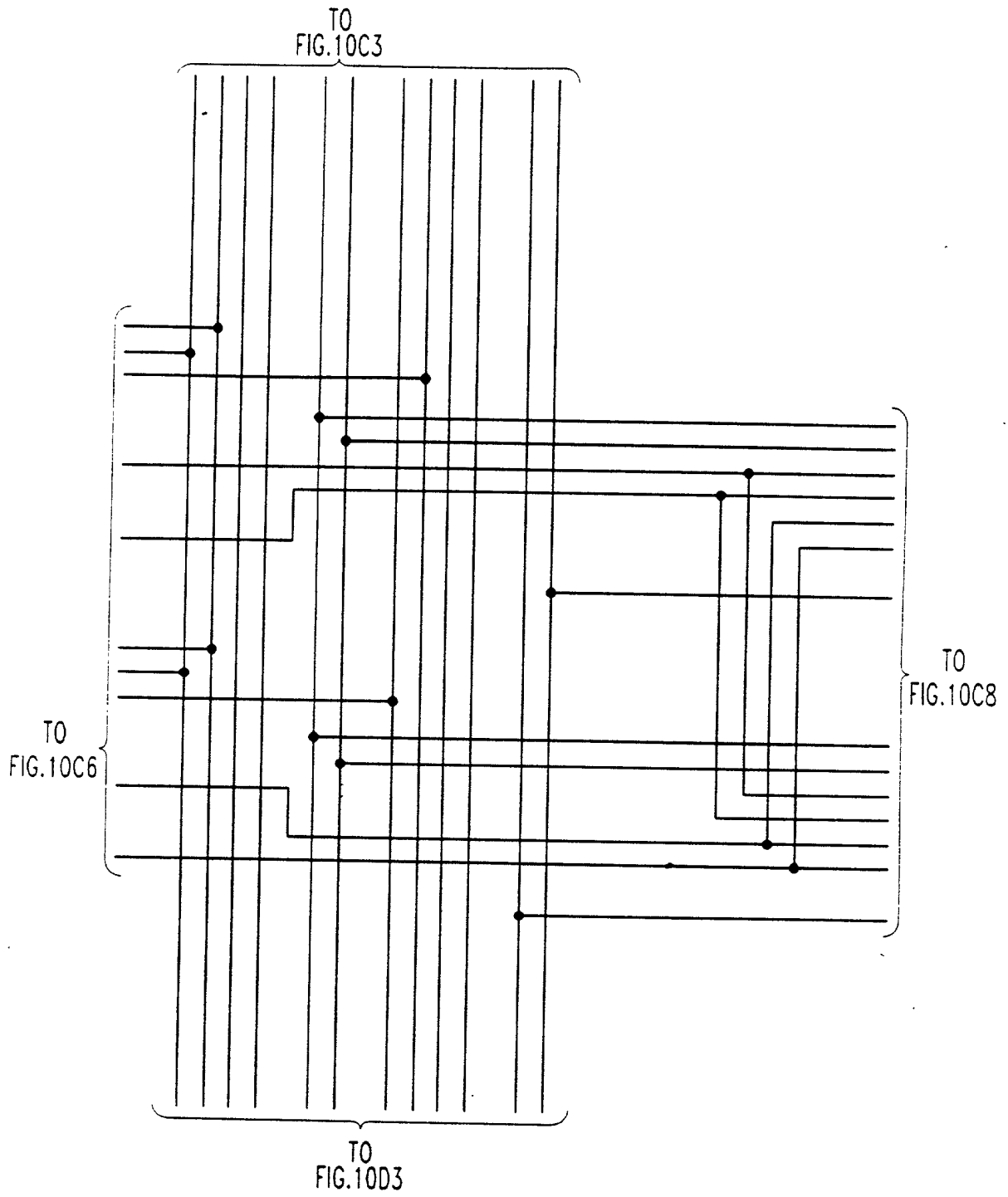


FIG.10C7

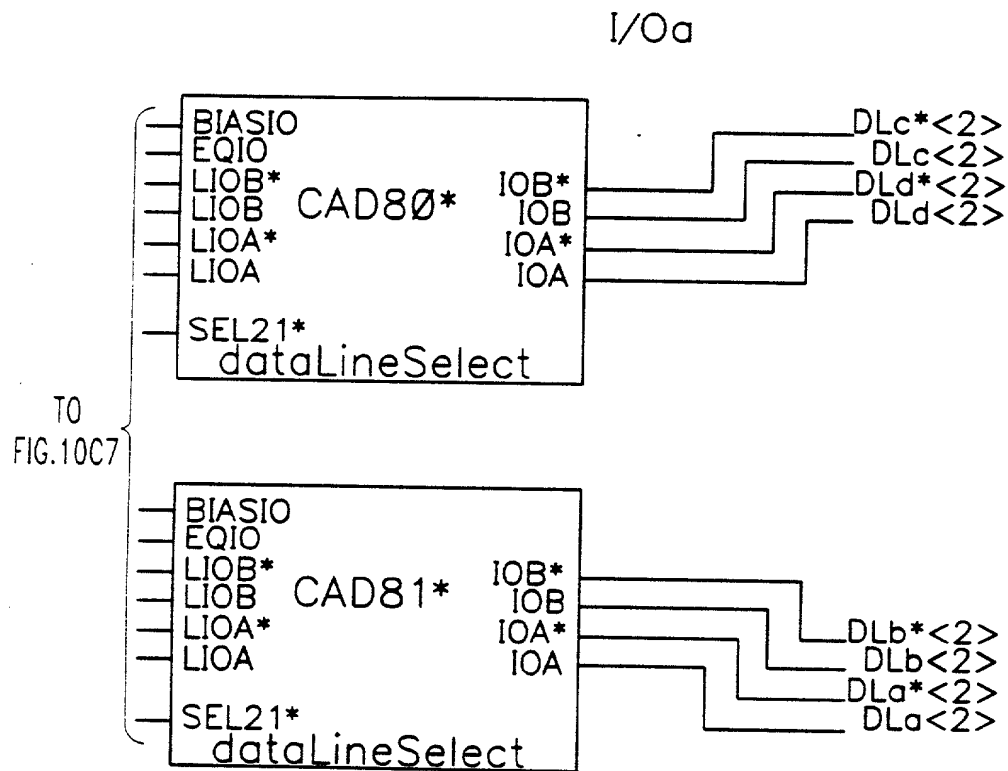


FIG.10C8

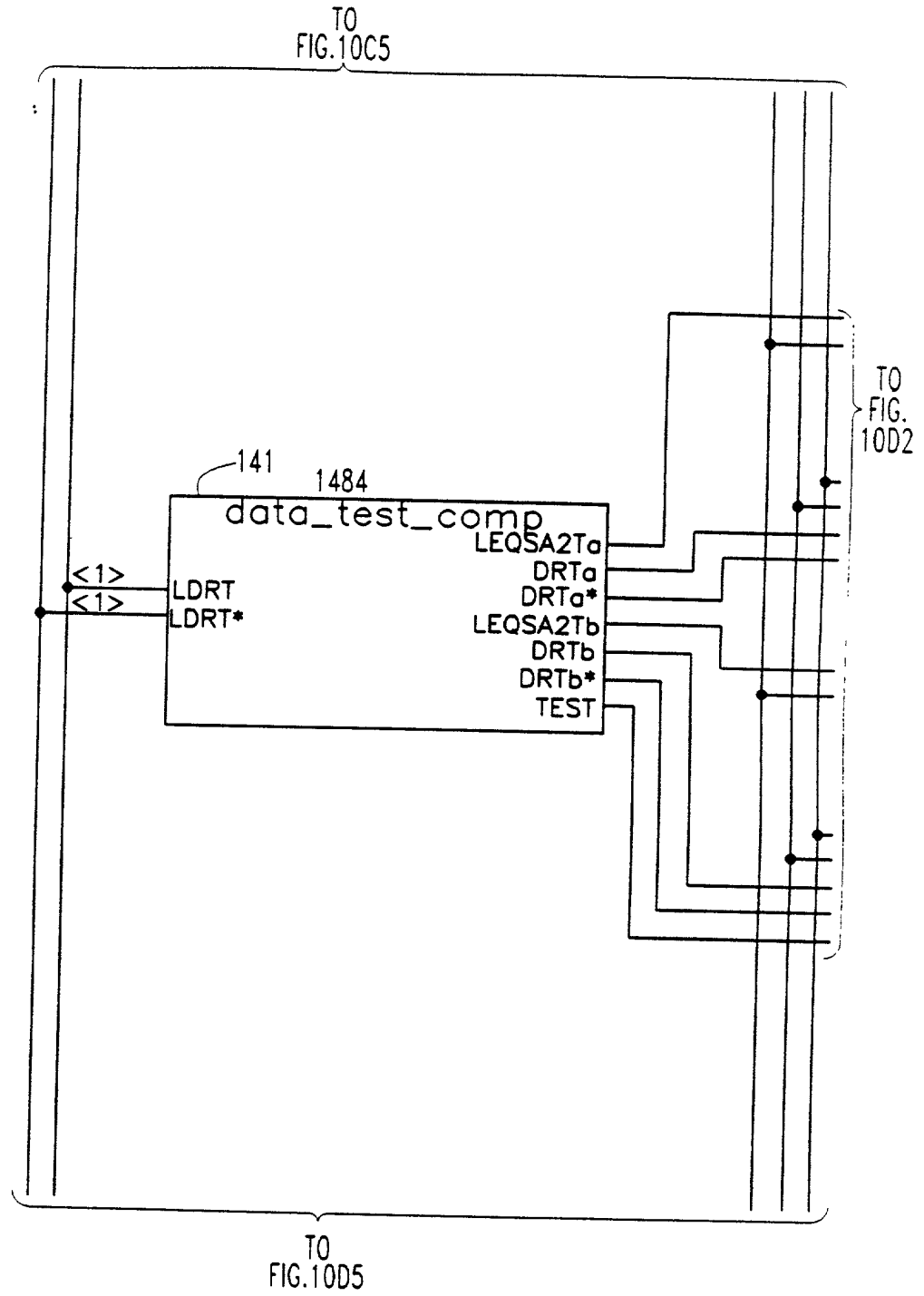


FIG. 10D1

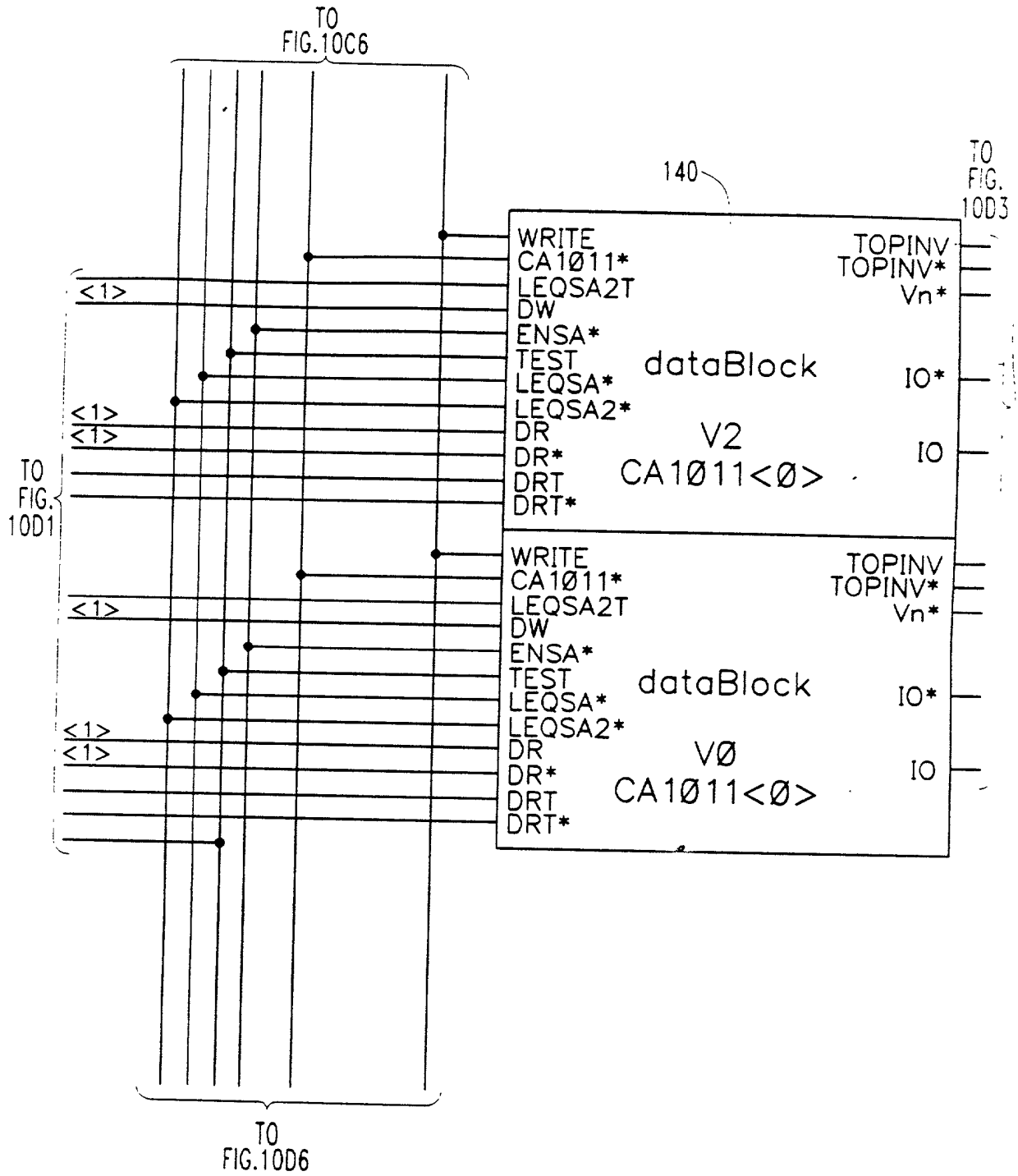
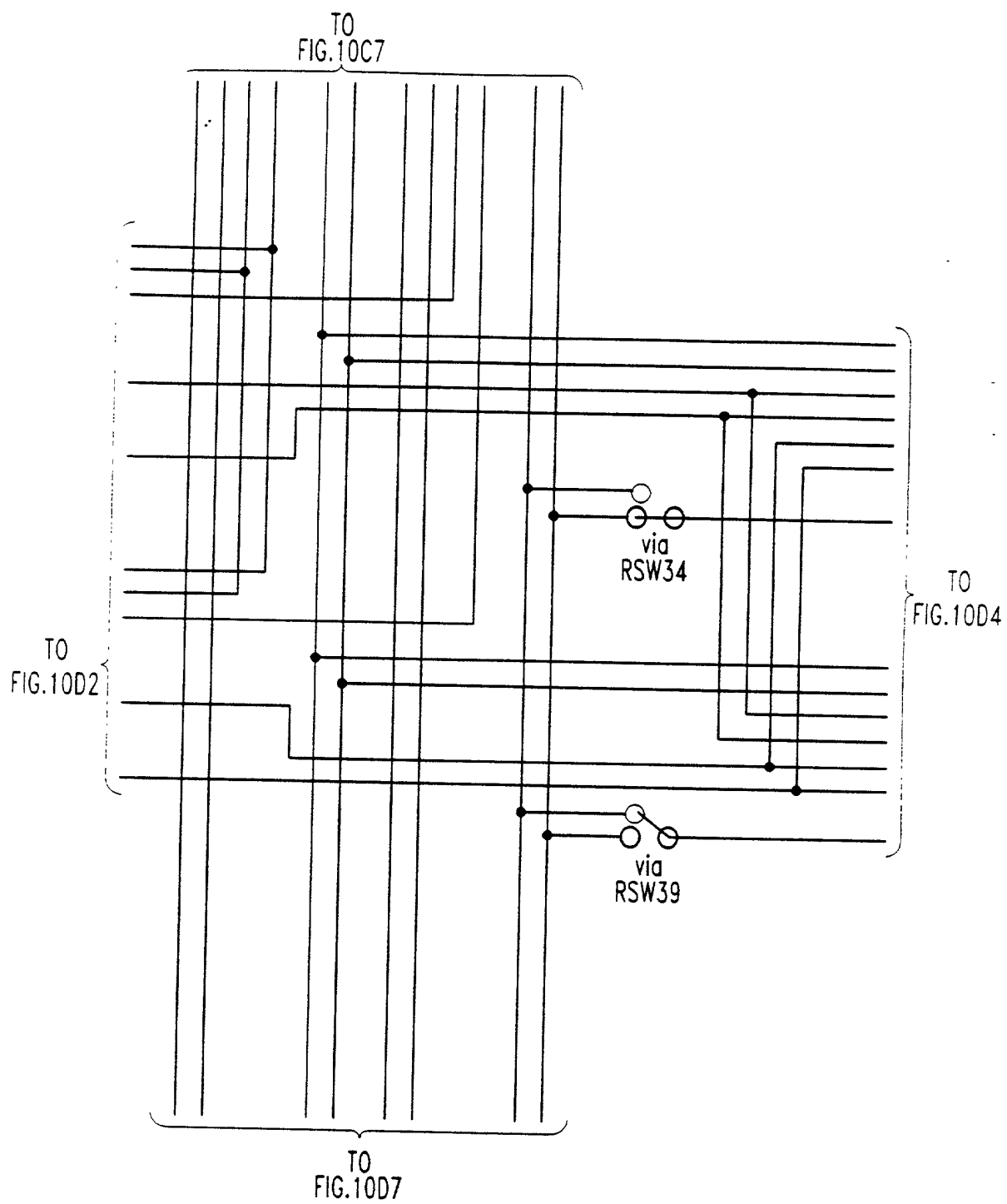
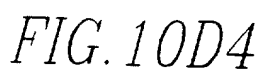


FIG. 10D2

*FIG. 10D3*



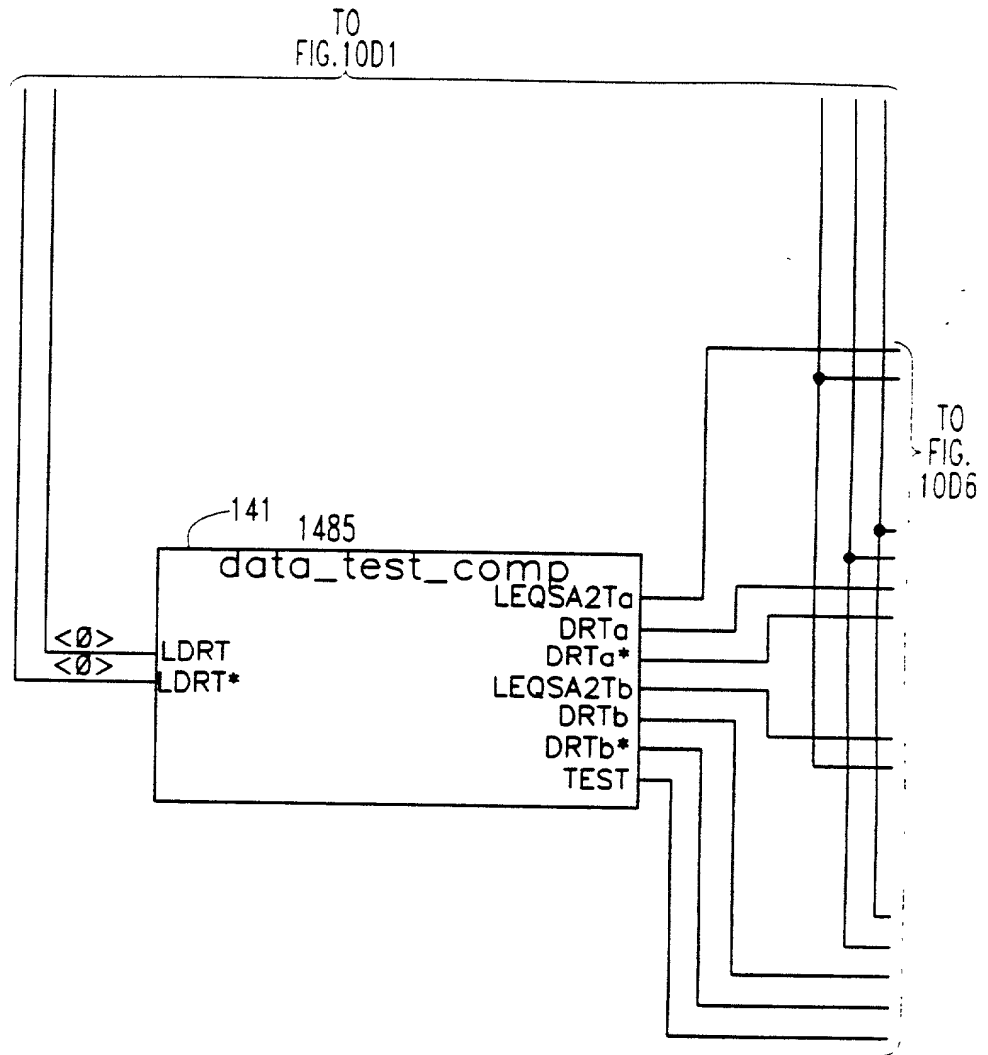


FIG. 10D5

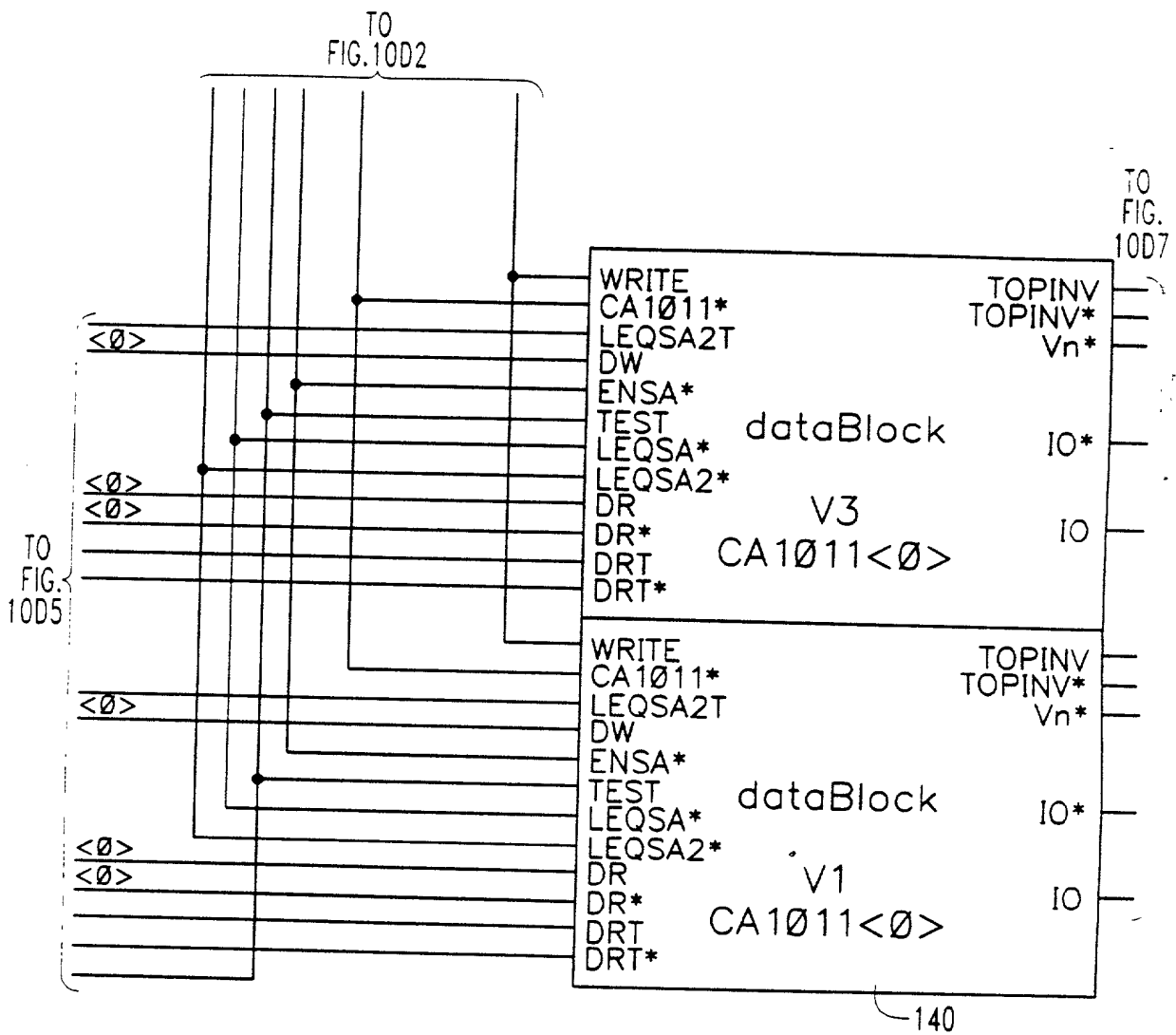


FIG. 10D6

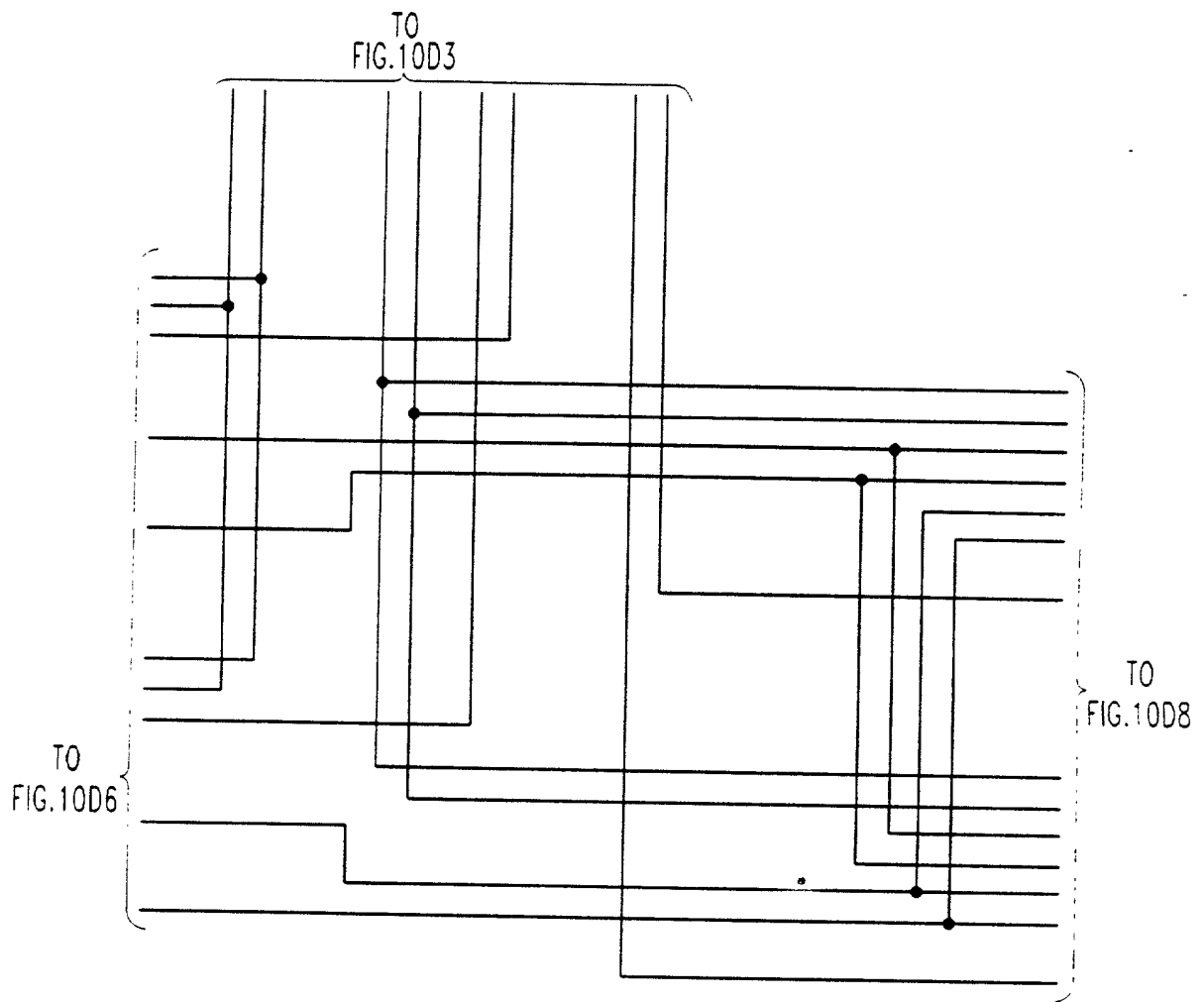


FIG. 10D7

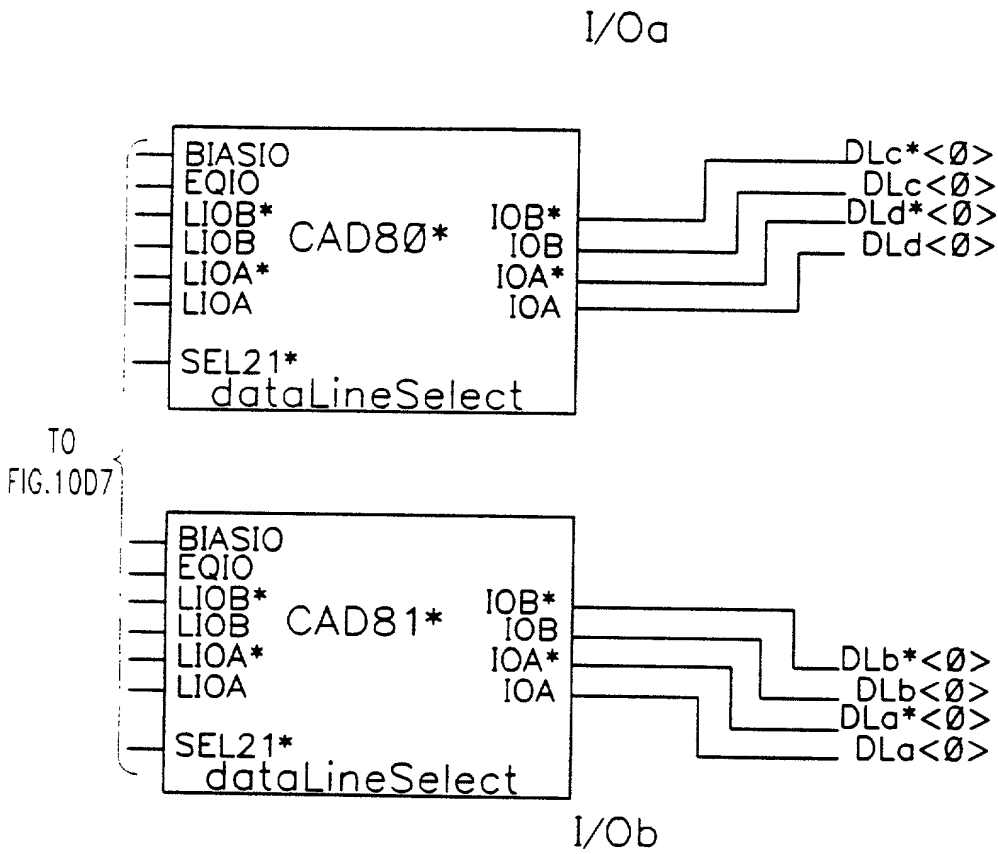


FIG.10D8

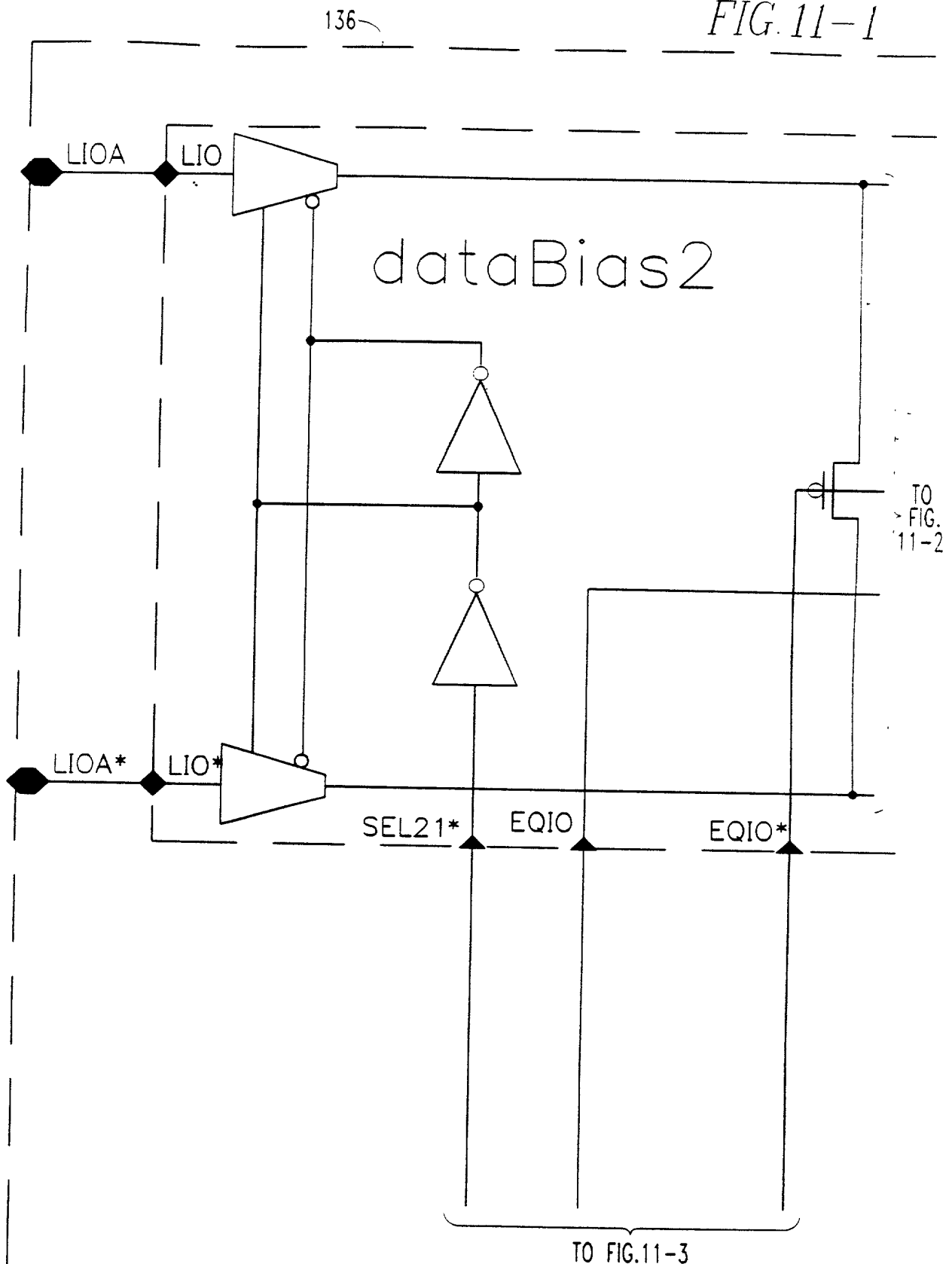
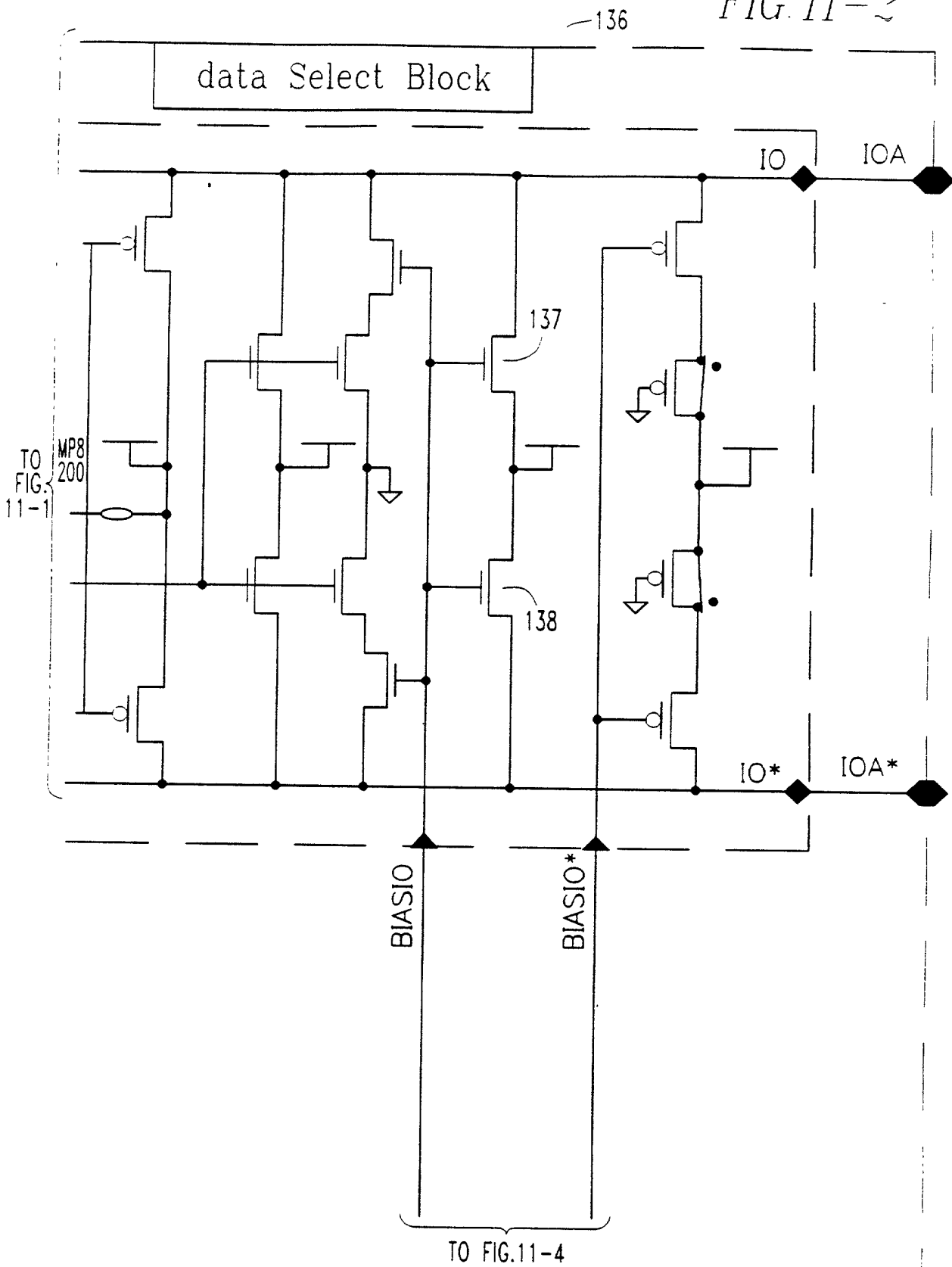


FIG. 11-2



51.367

TO FIG.11-1

TO
FIG.
11-4

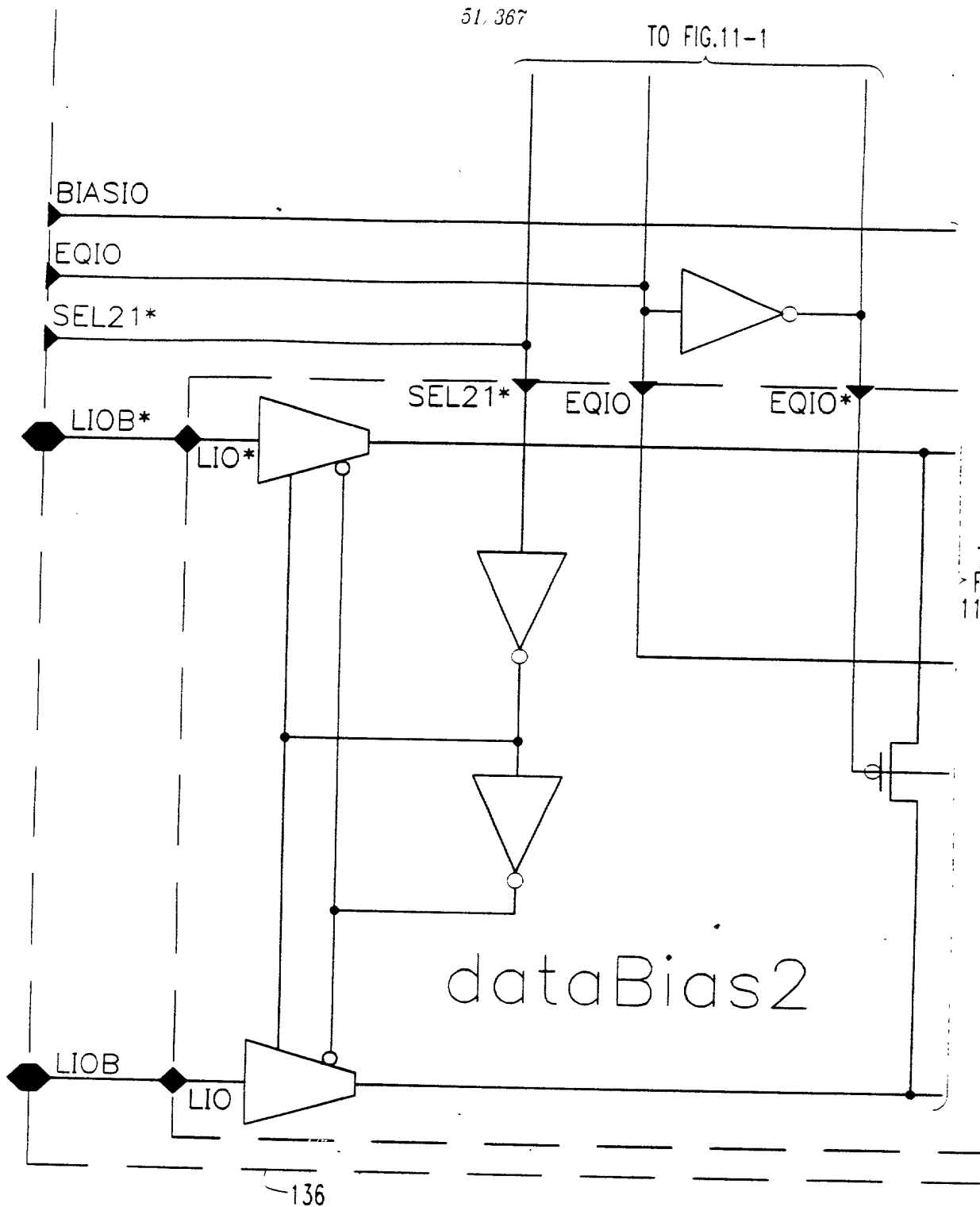


FIG. 11-3

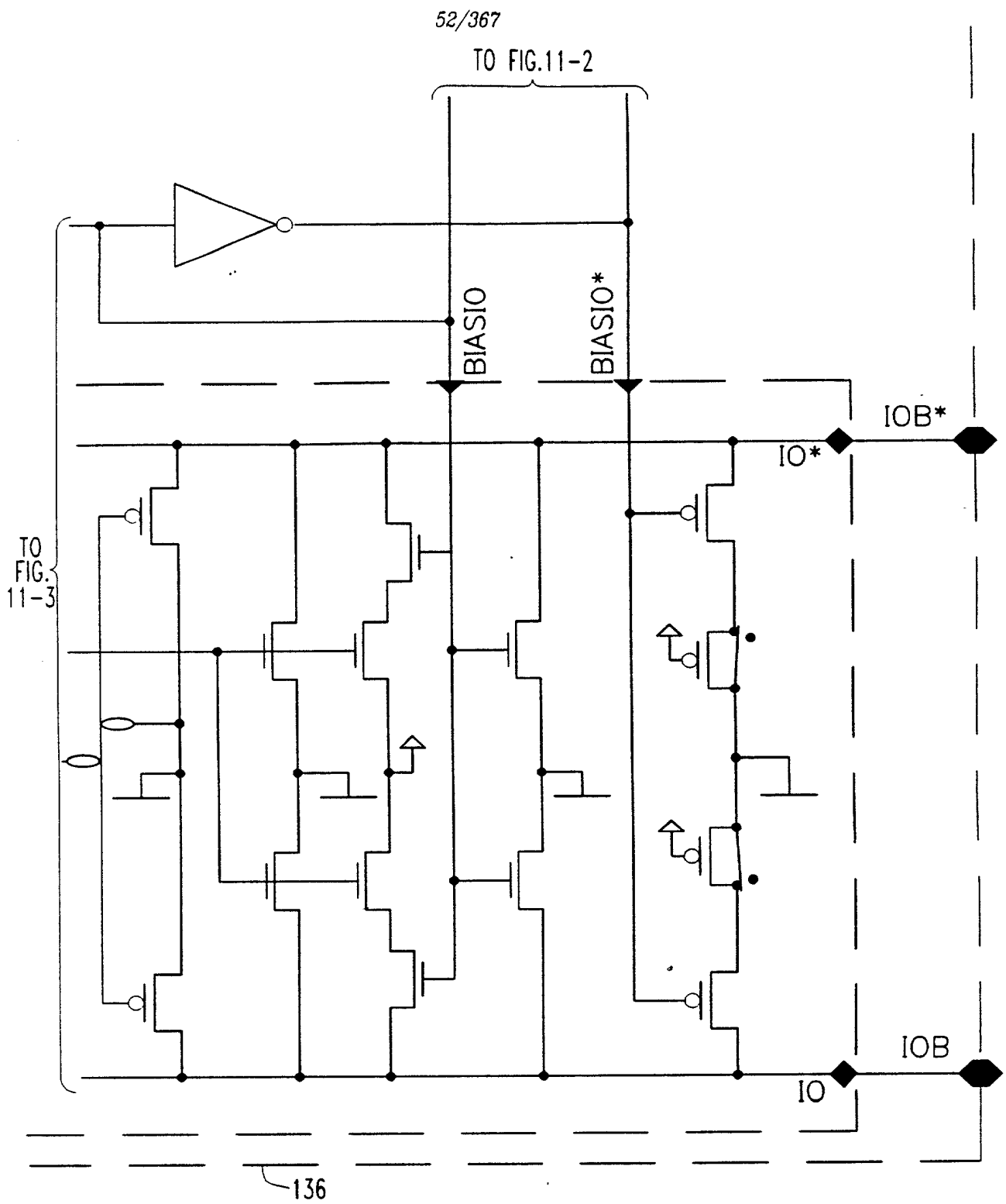


FIG.11-4

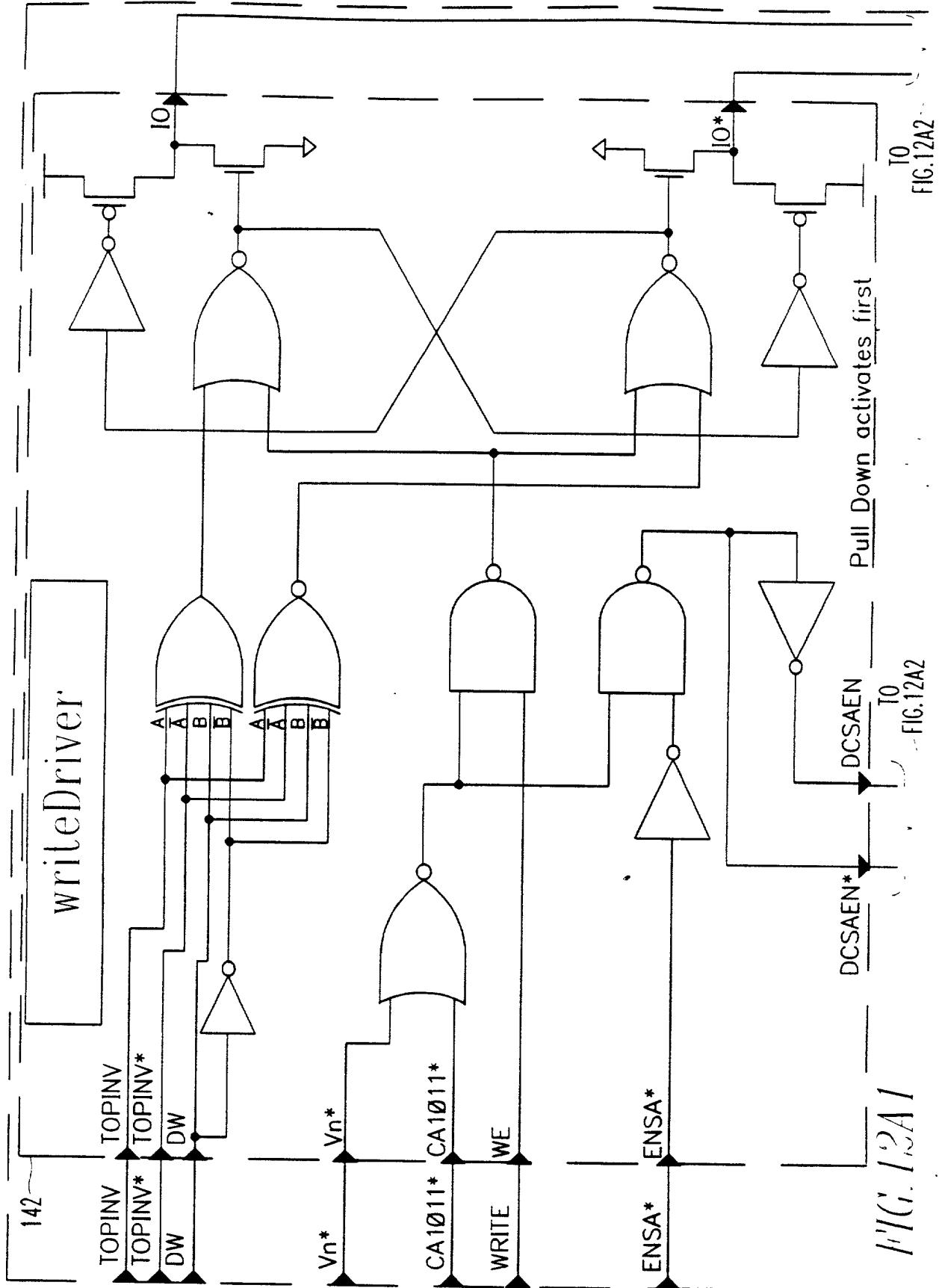


FIG. 12A2

FIG. 12A2

FIG. 12A1

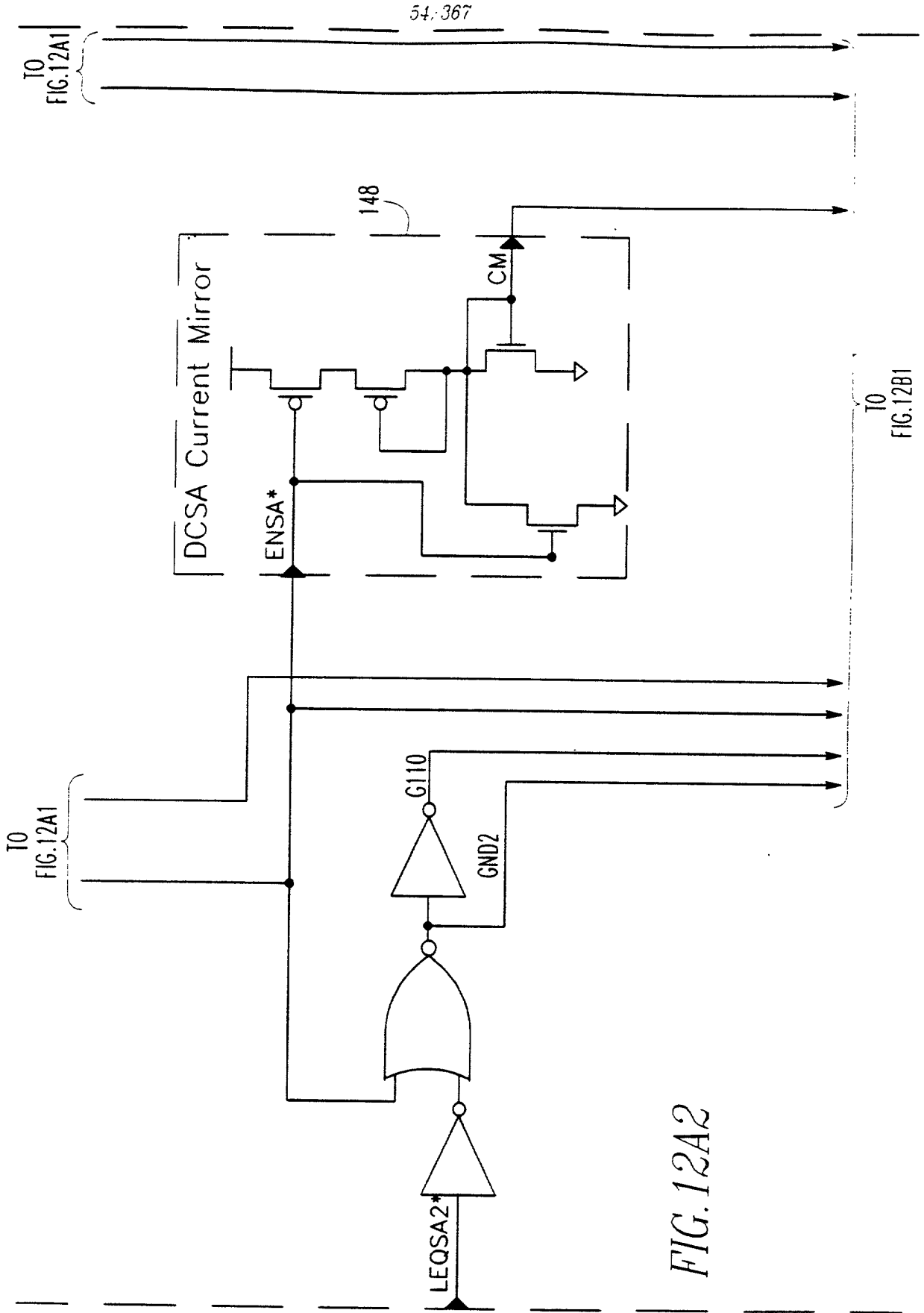
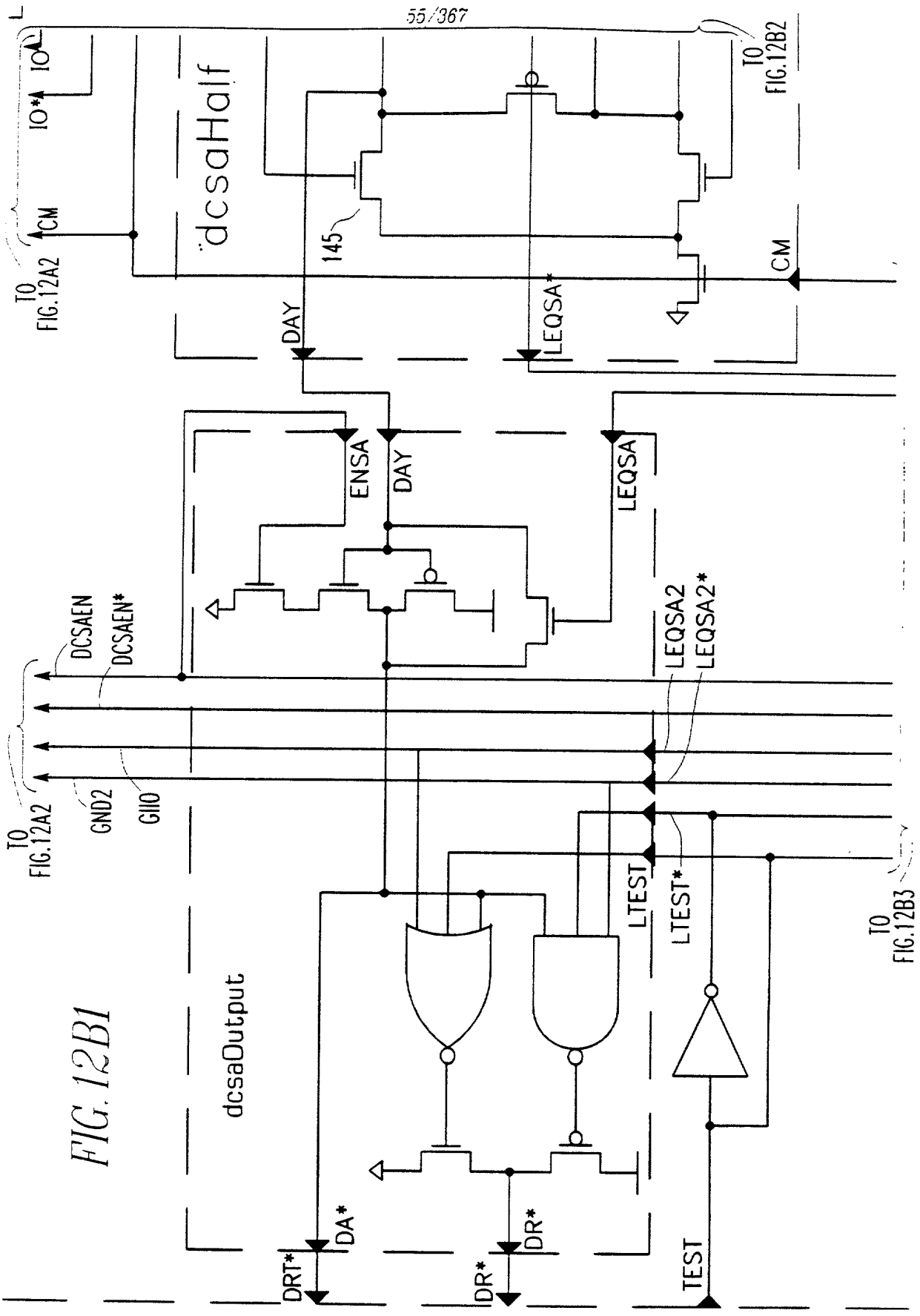


FIG. 12A2



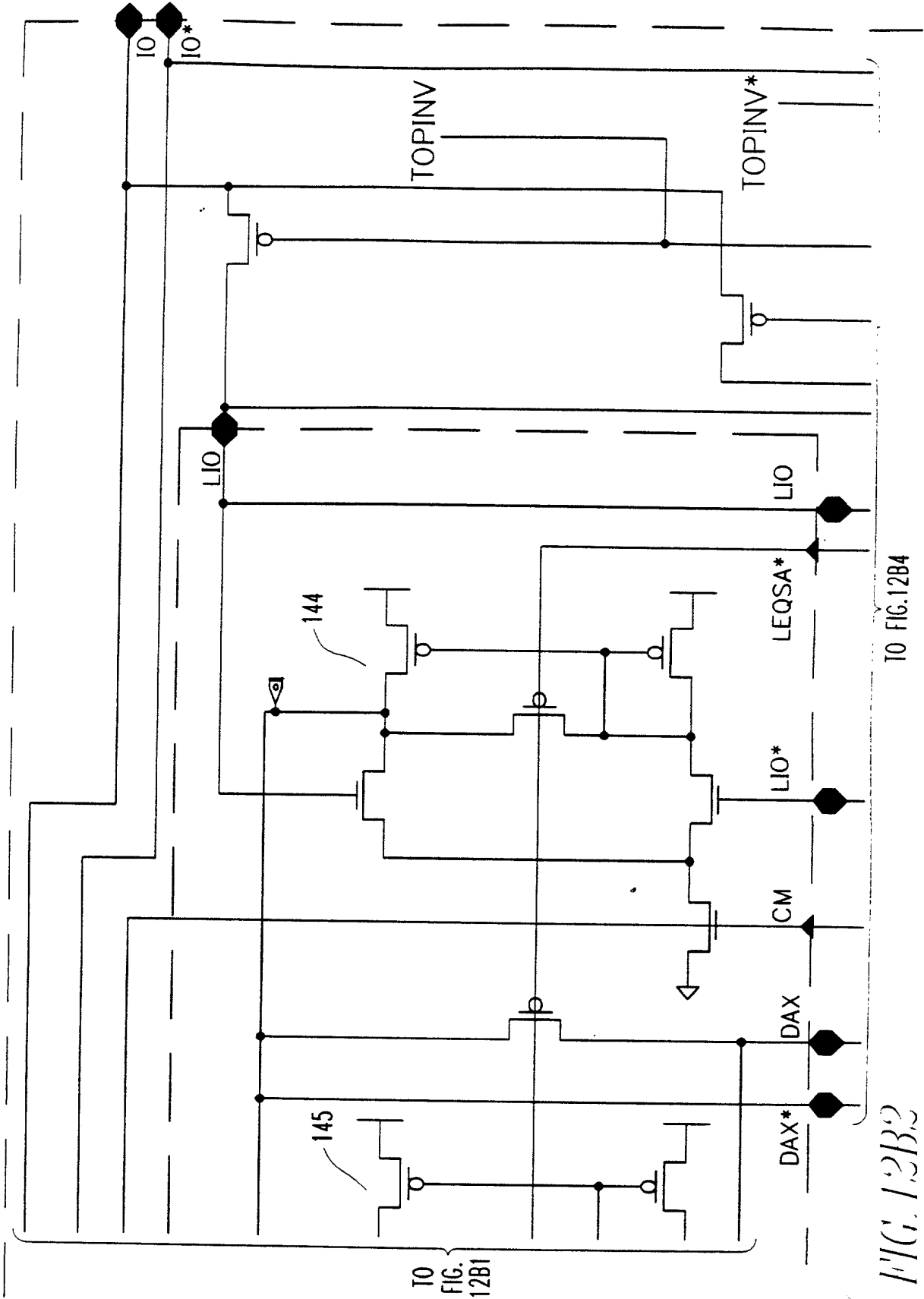
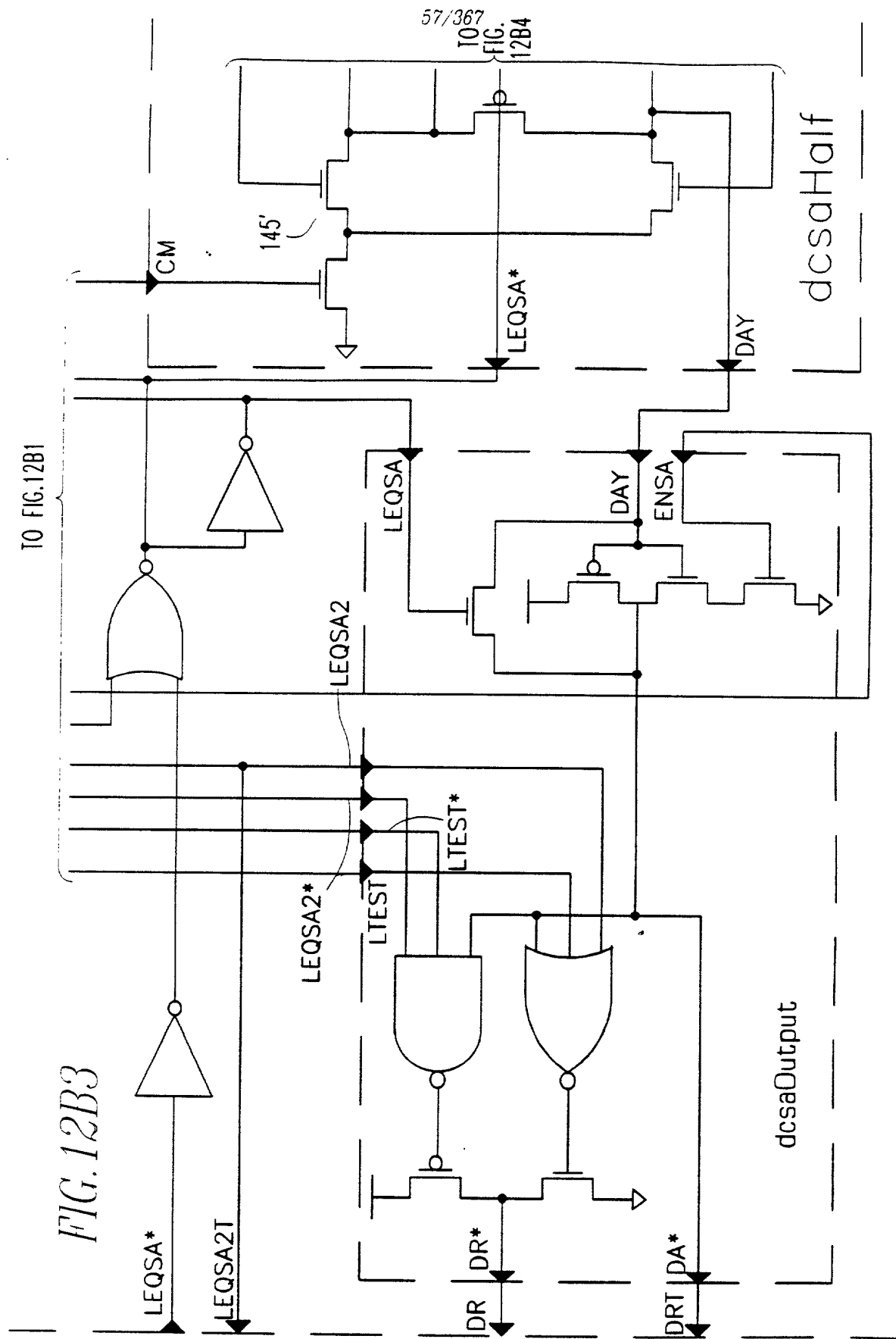


FIG. 12B2

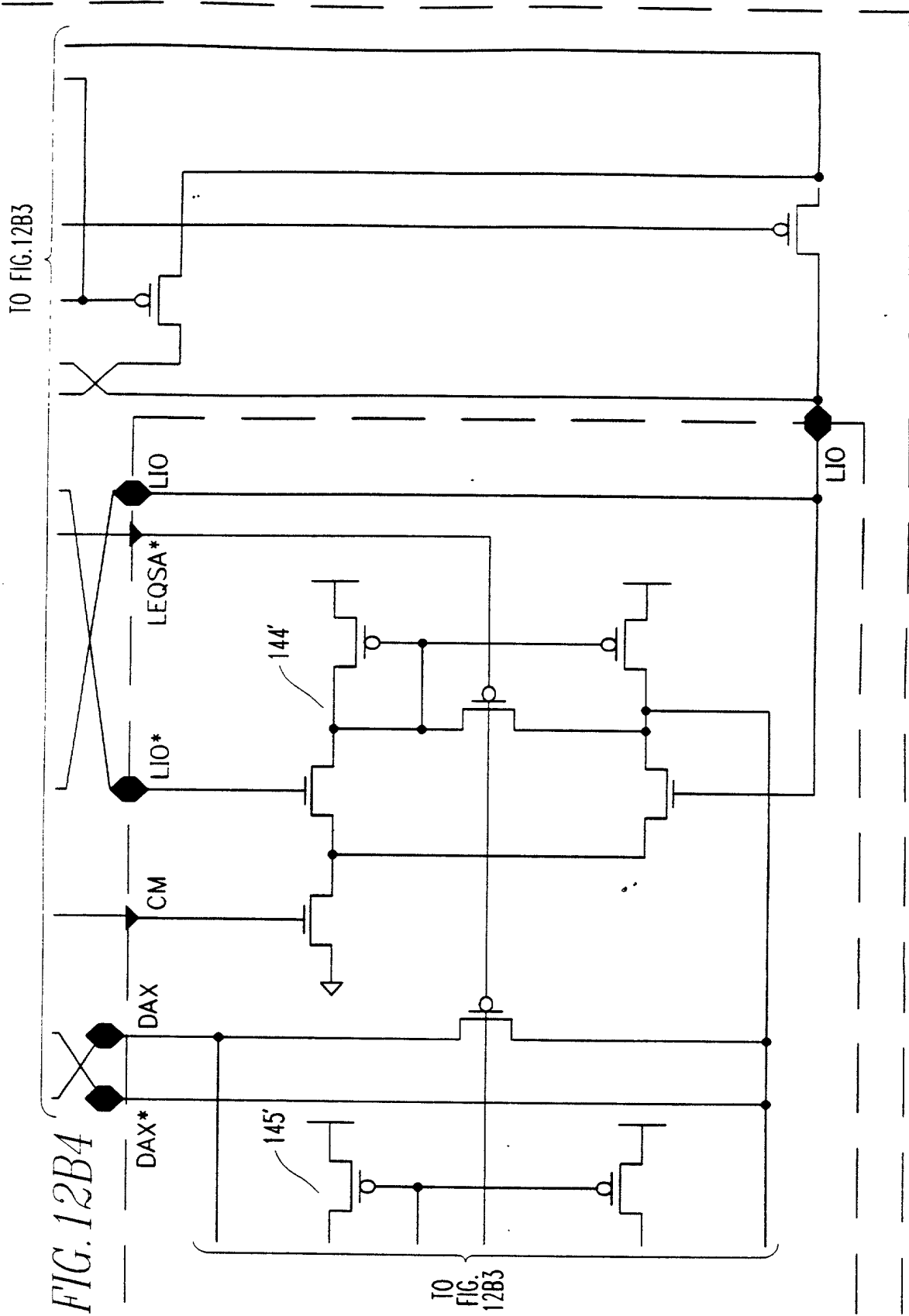
FIG. 12B4

FIG. 12B3

TO FIG. 12B1



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108390
FIG. 12B4



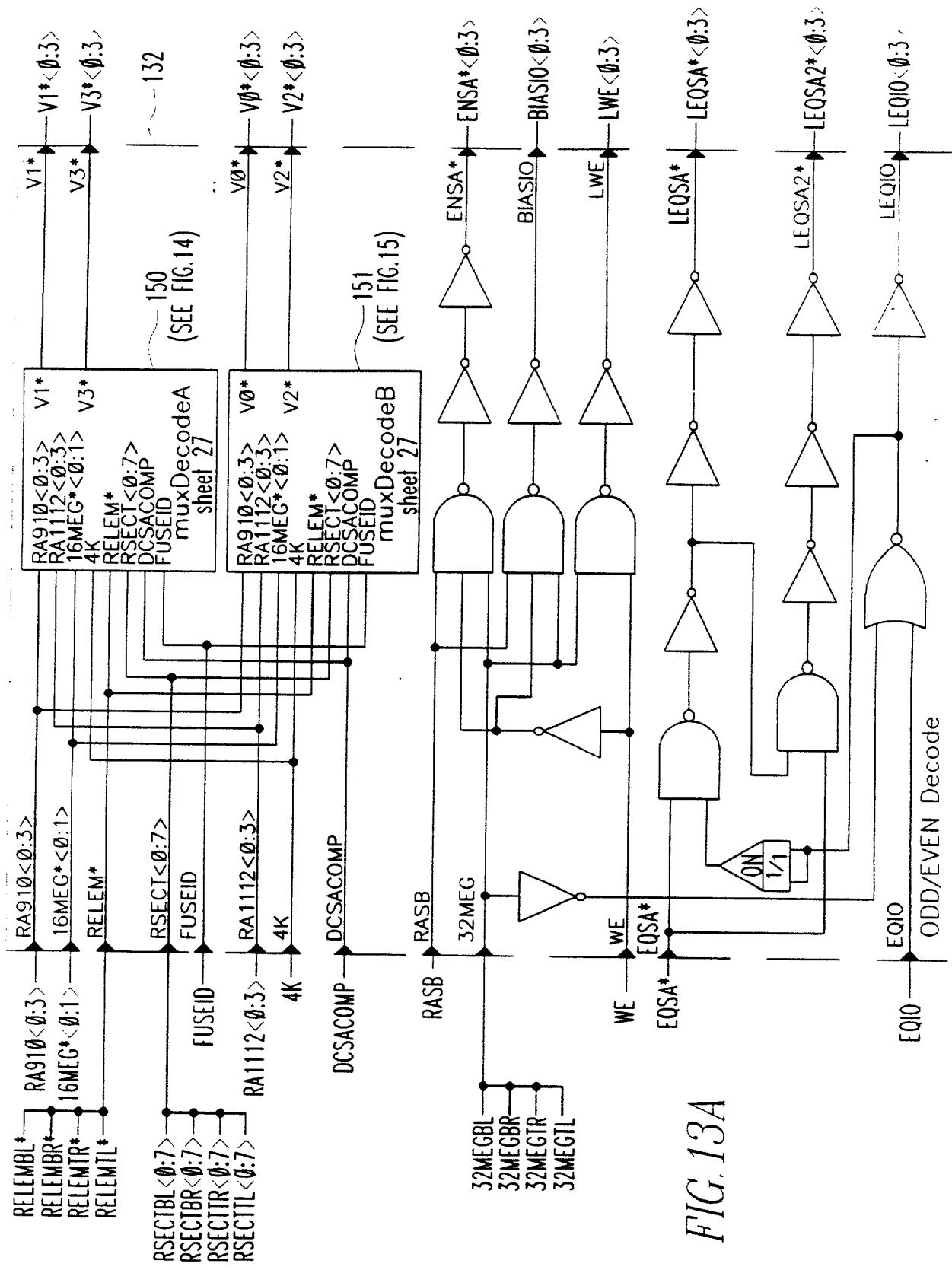


FIG. 13A

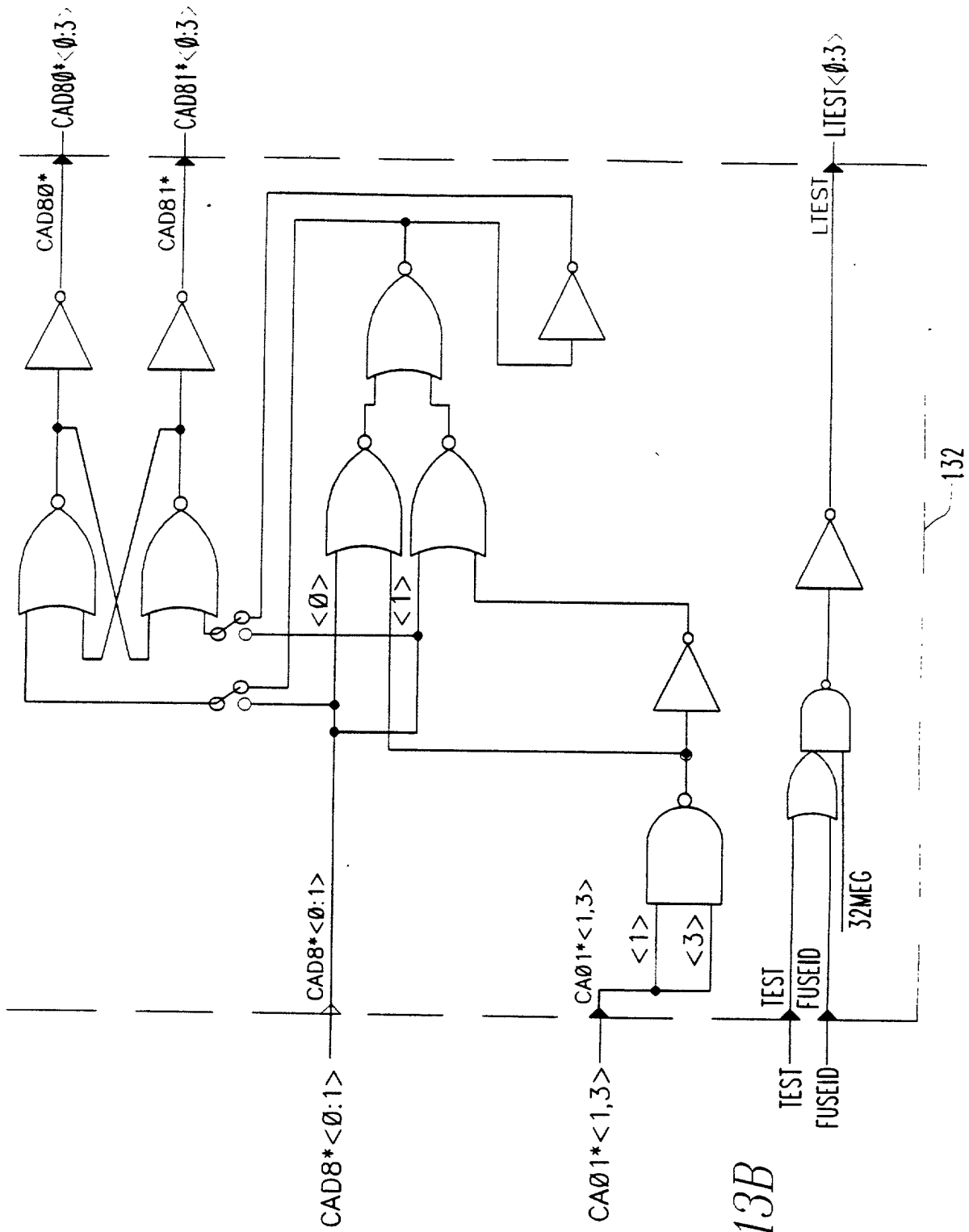


FIG. 13B

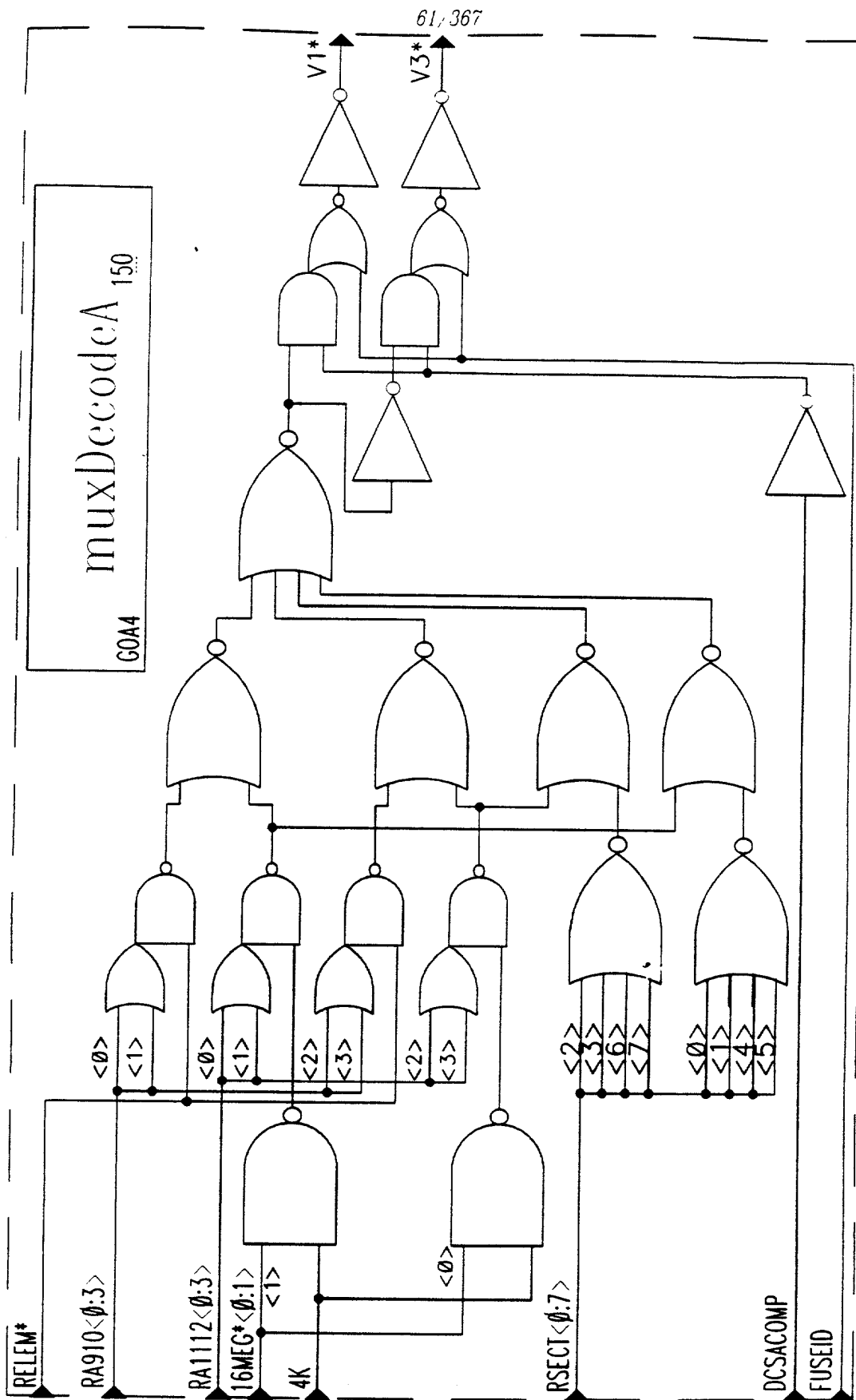


FIG. 11

FIG 15 1

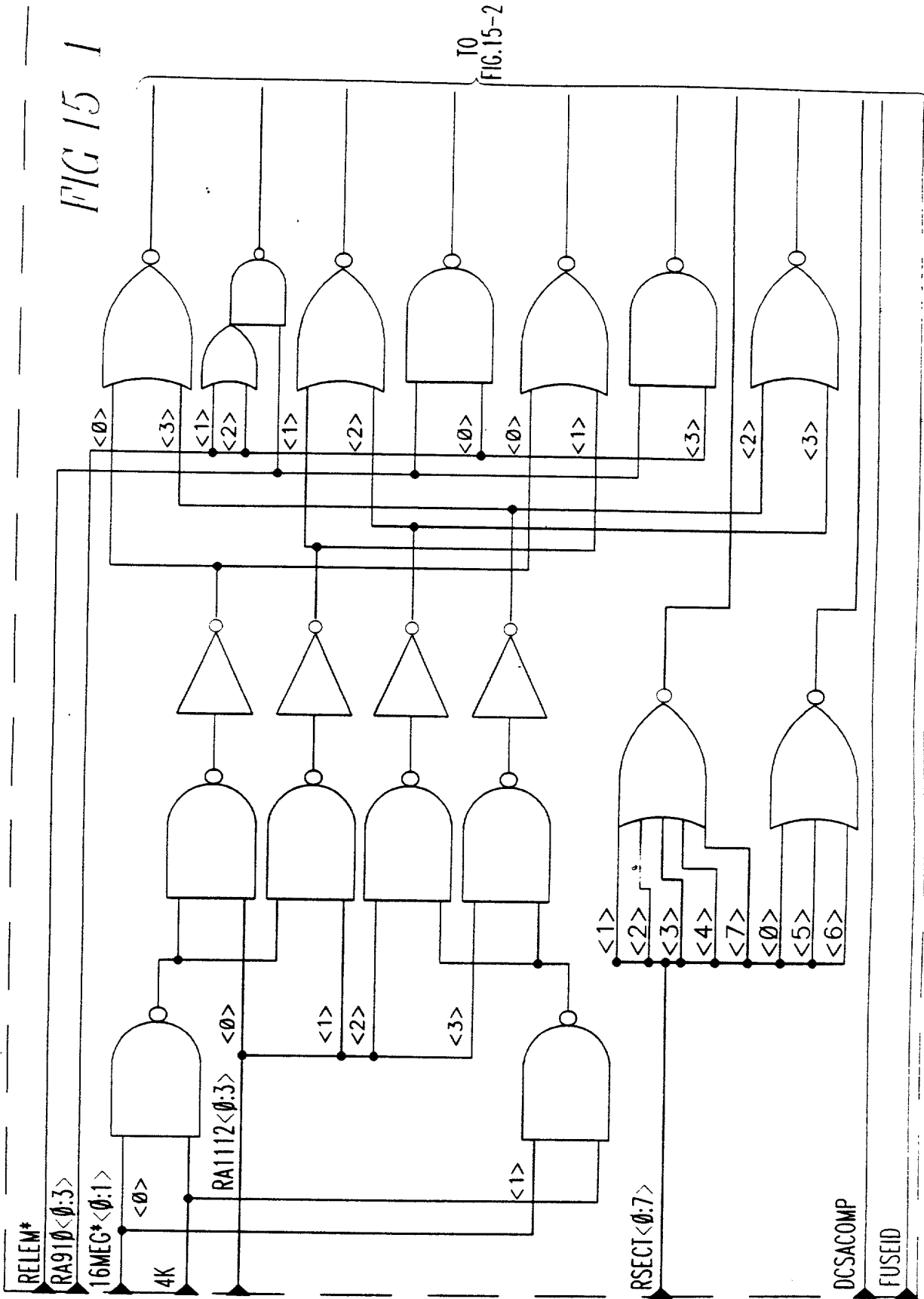


FIG. 15-2

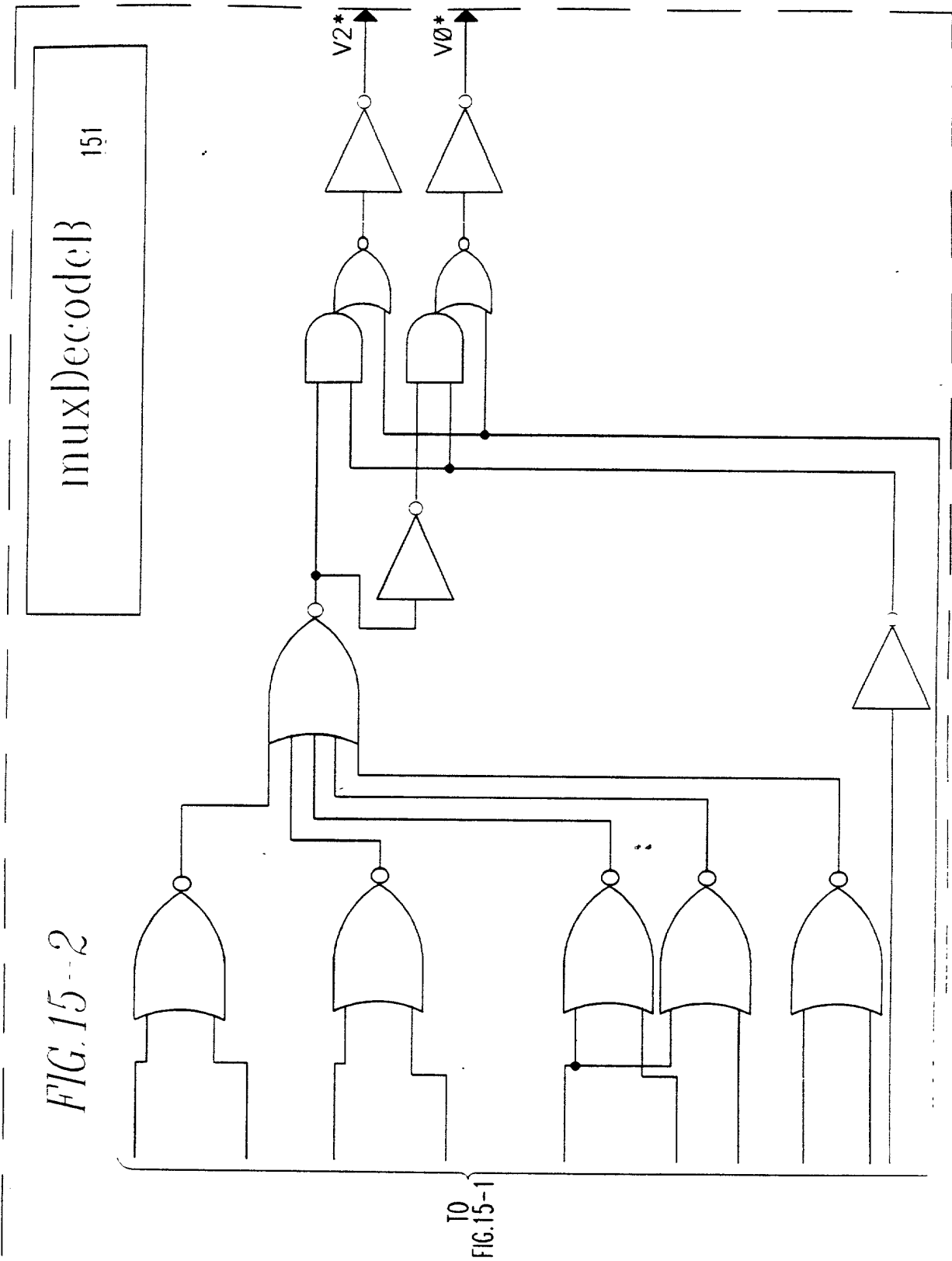
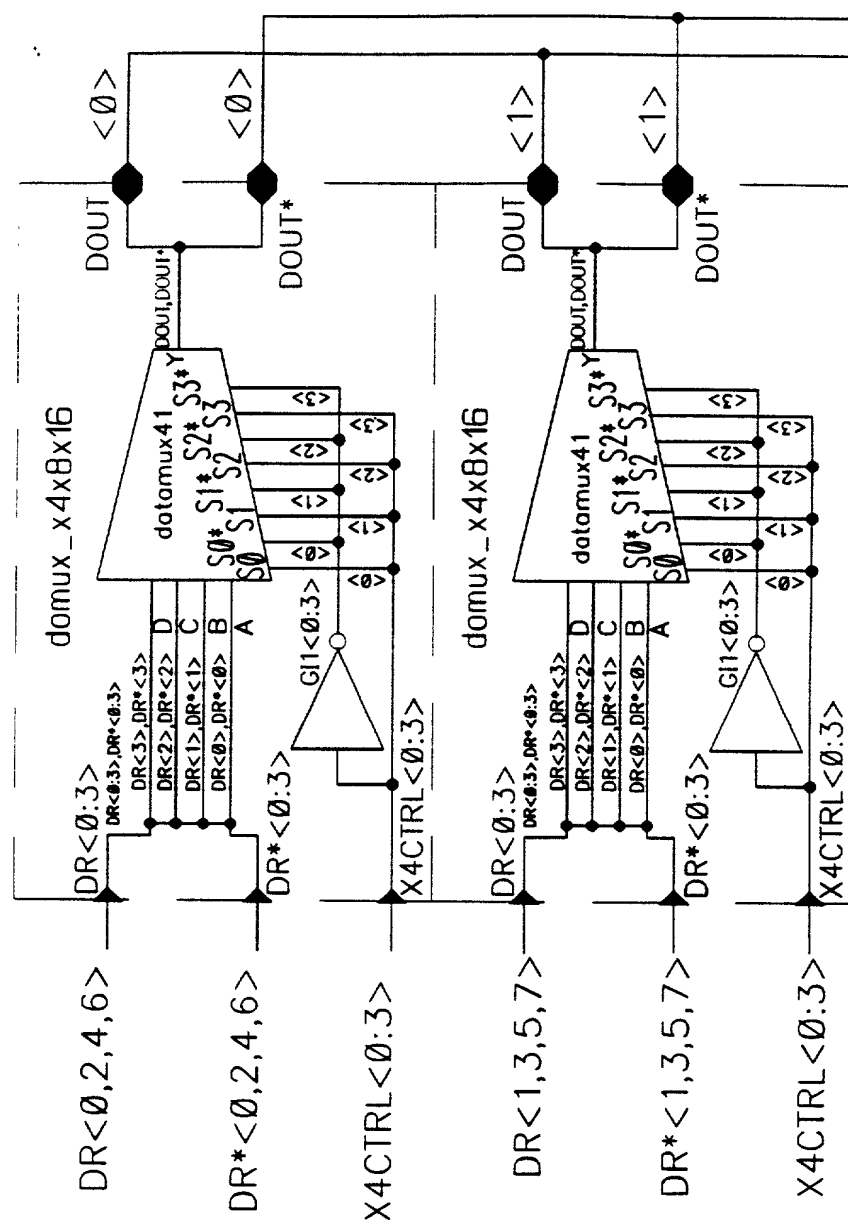
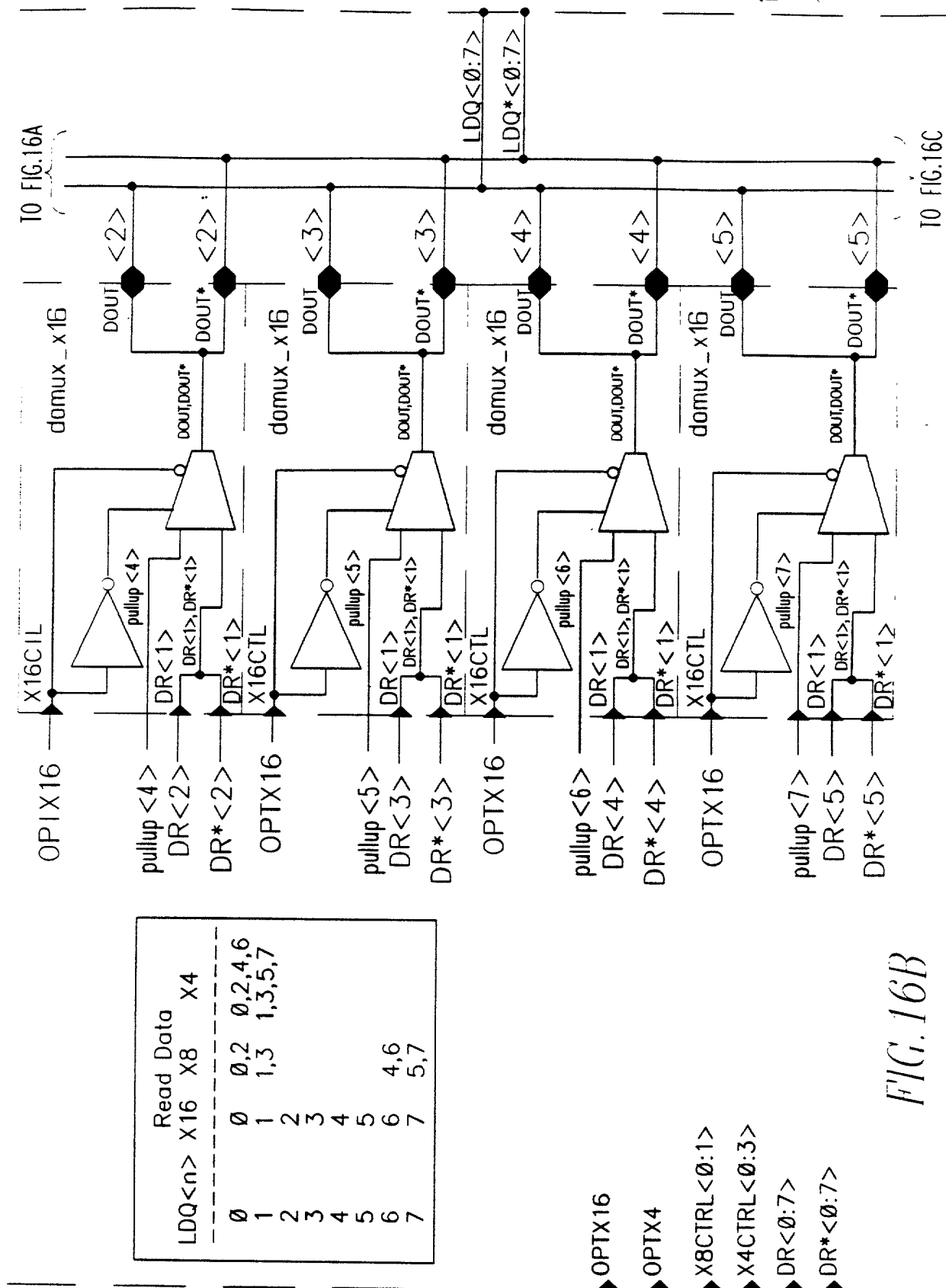


FIG. 16A





Read Data			
LDQ <n>	X16	X8	X4
0	0	0,2	0,2,4,6
1	1	1,3	1,3,5,7
2	2		
3	3		
4	4		
5	5		
6	6	4,6	
7	7	5,7	

FIG. 16B

- OPTX16
- OPTX4
- X8CTRL<0:1>
- X4CTRL<0:3>
- DR<0:7>
- DR*<0:7>

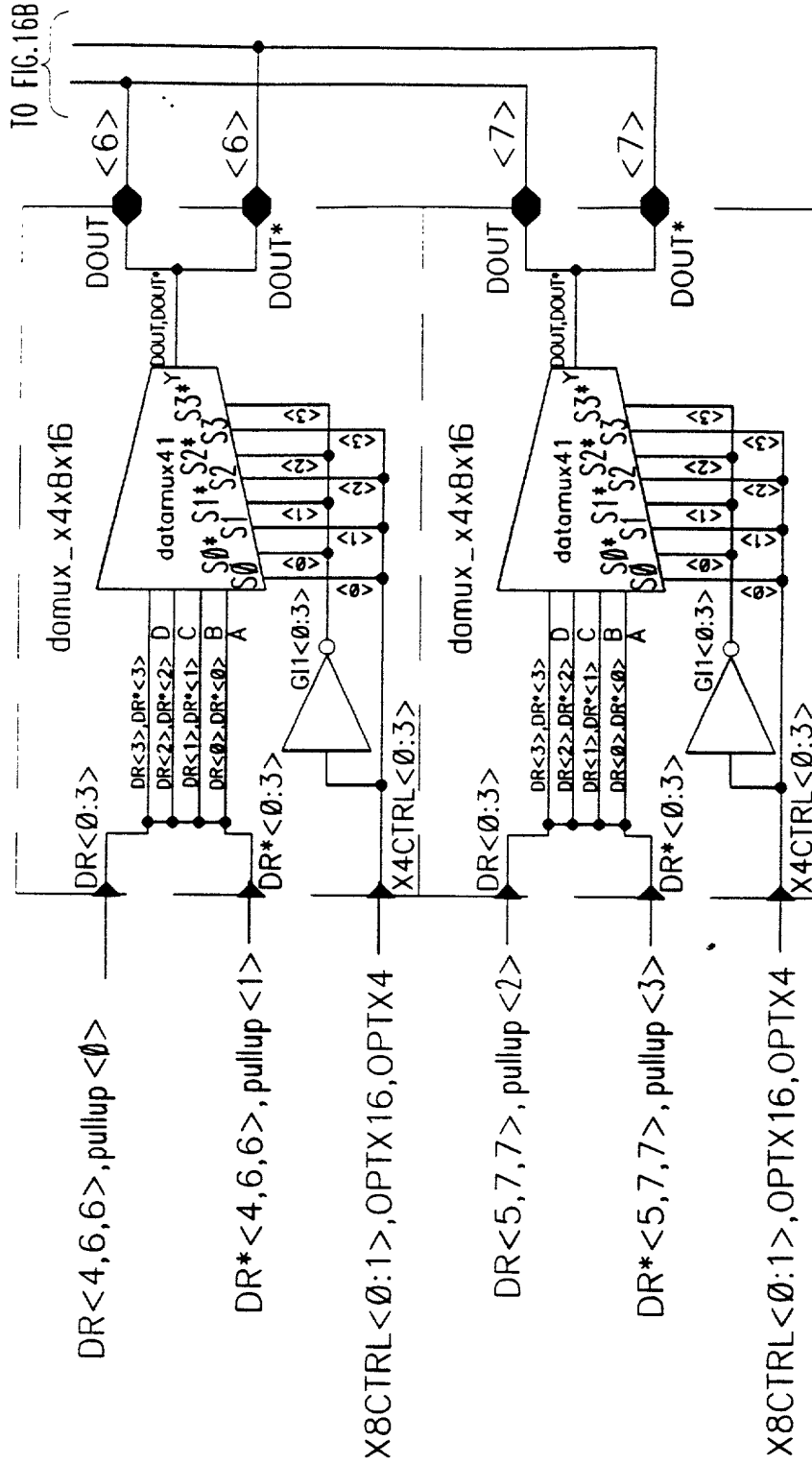


FIG. 16C

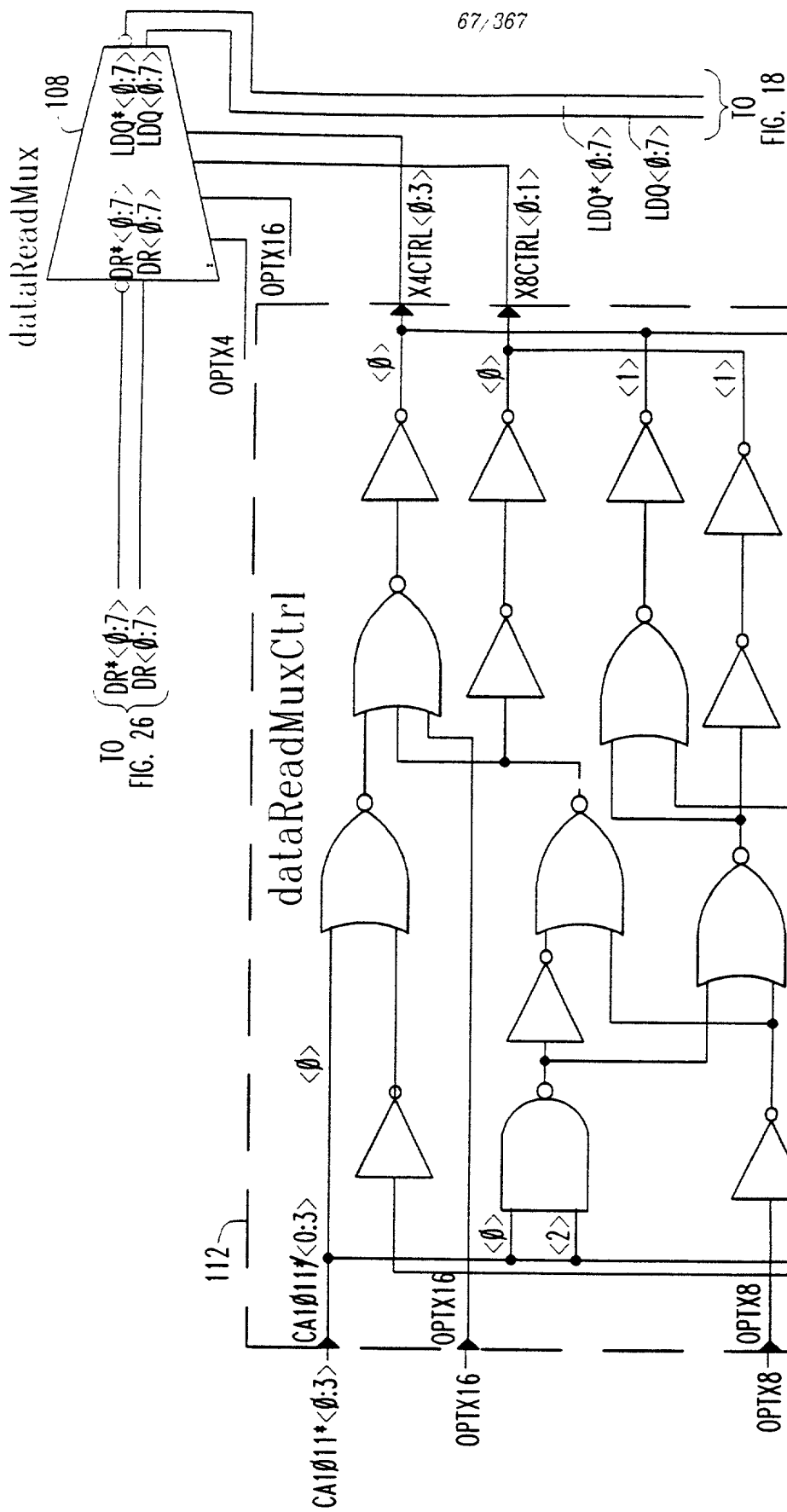


FIG. 17



DATA OUTPUT BUFFER

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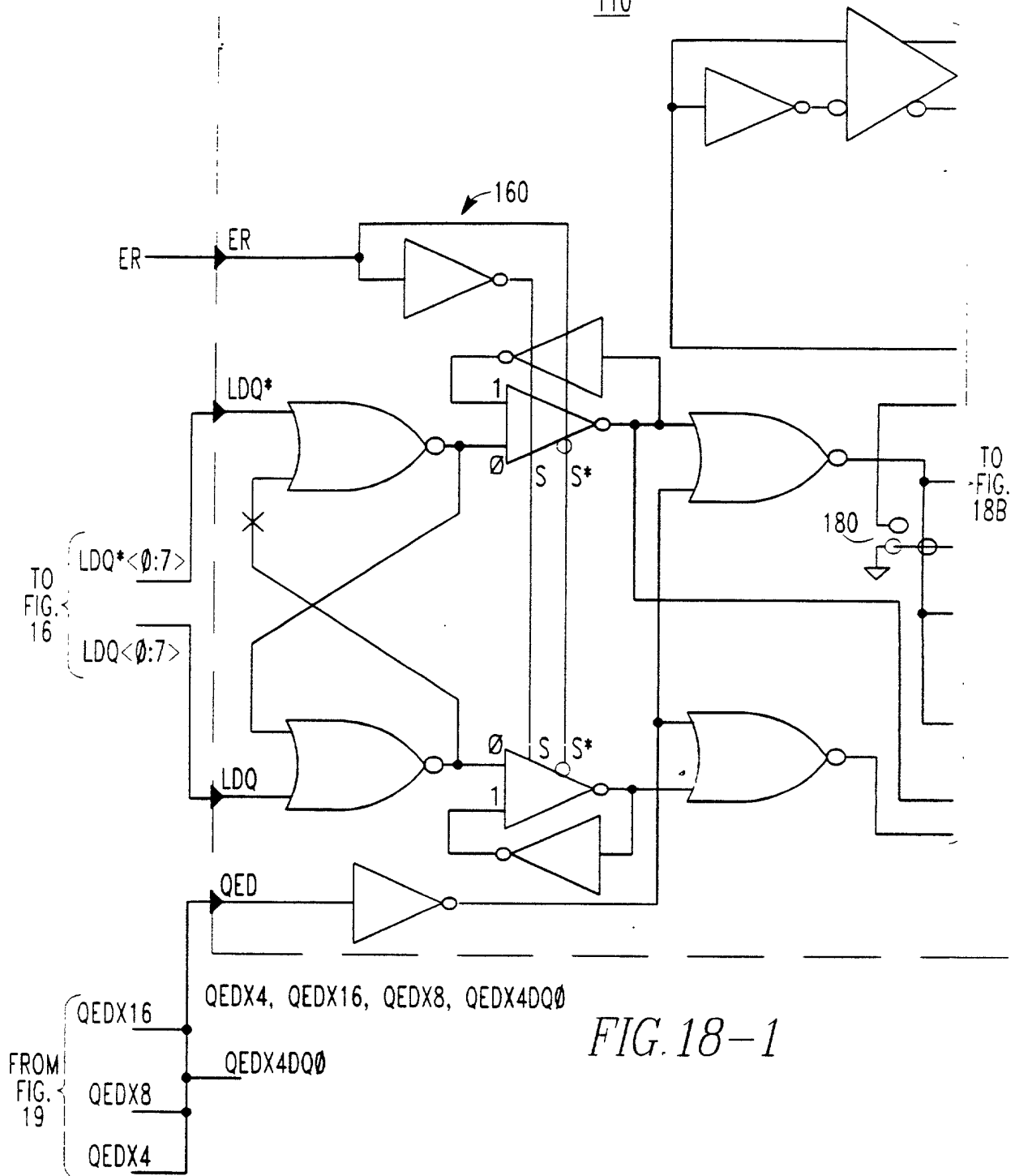


FIG. 18-1

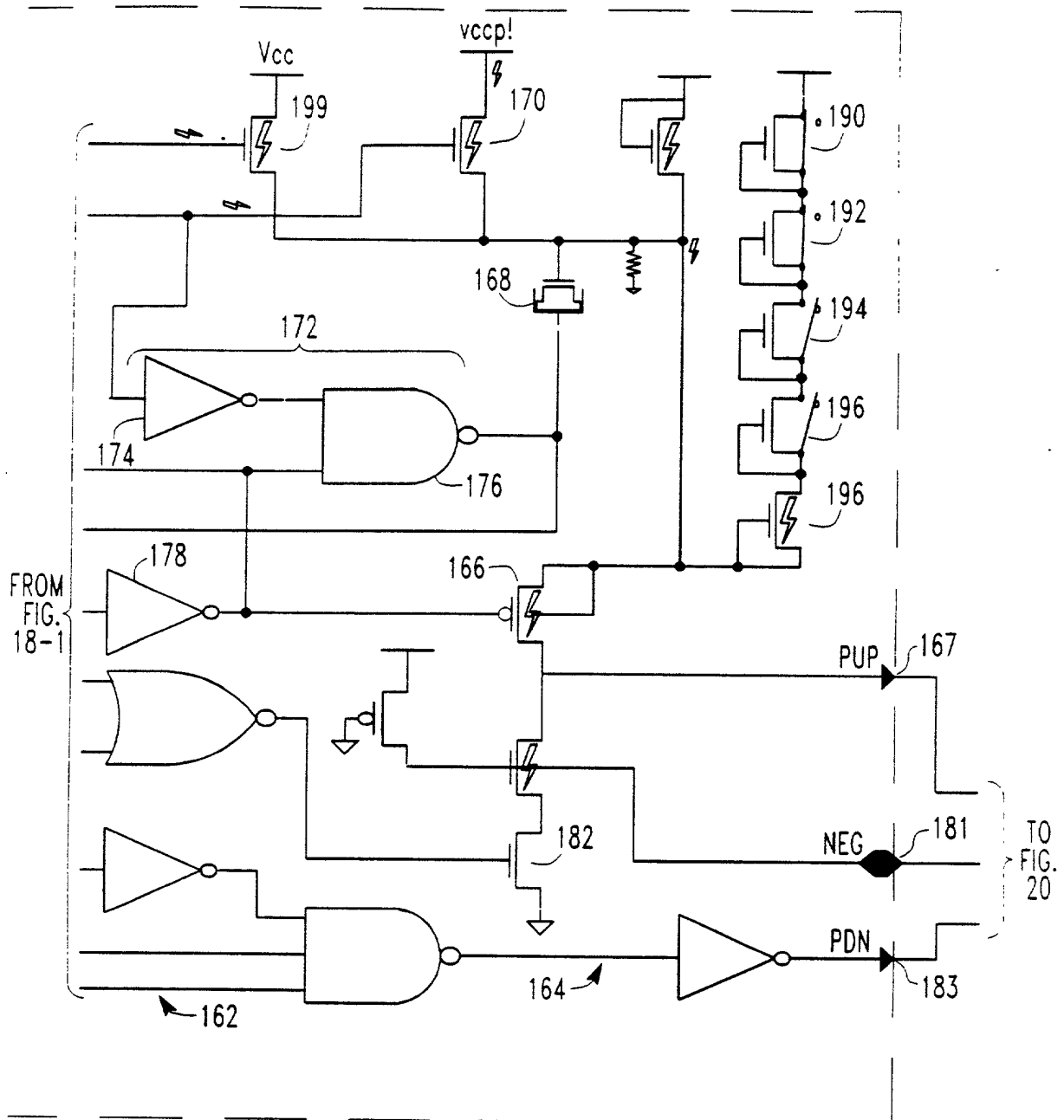


FIG. 18-2

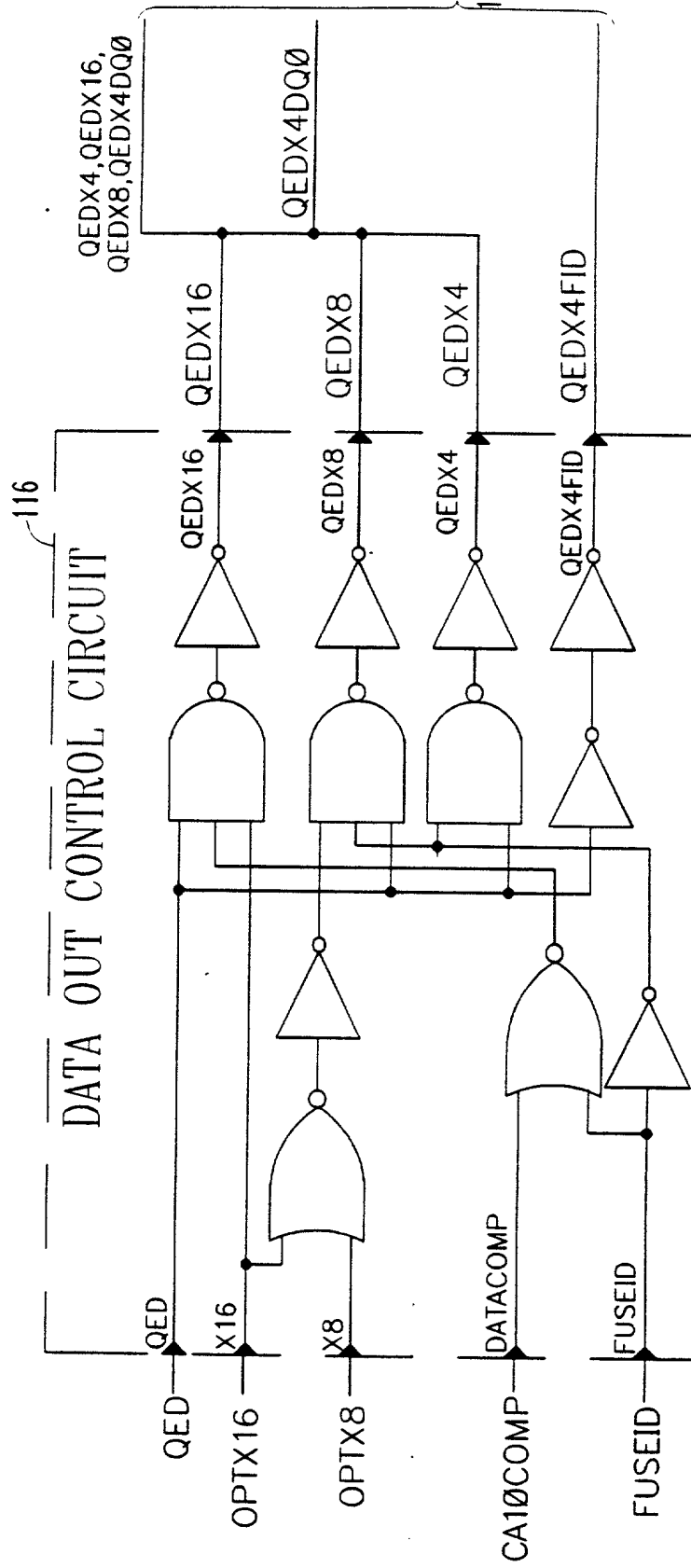


FIG. 19

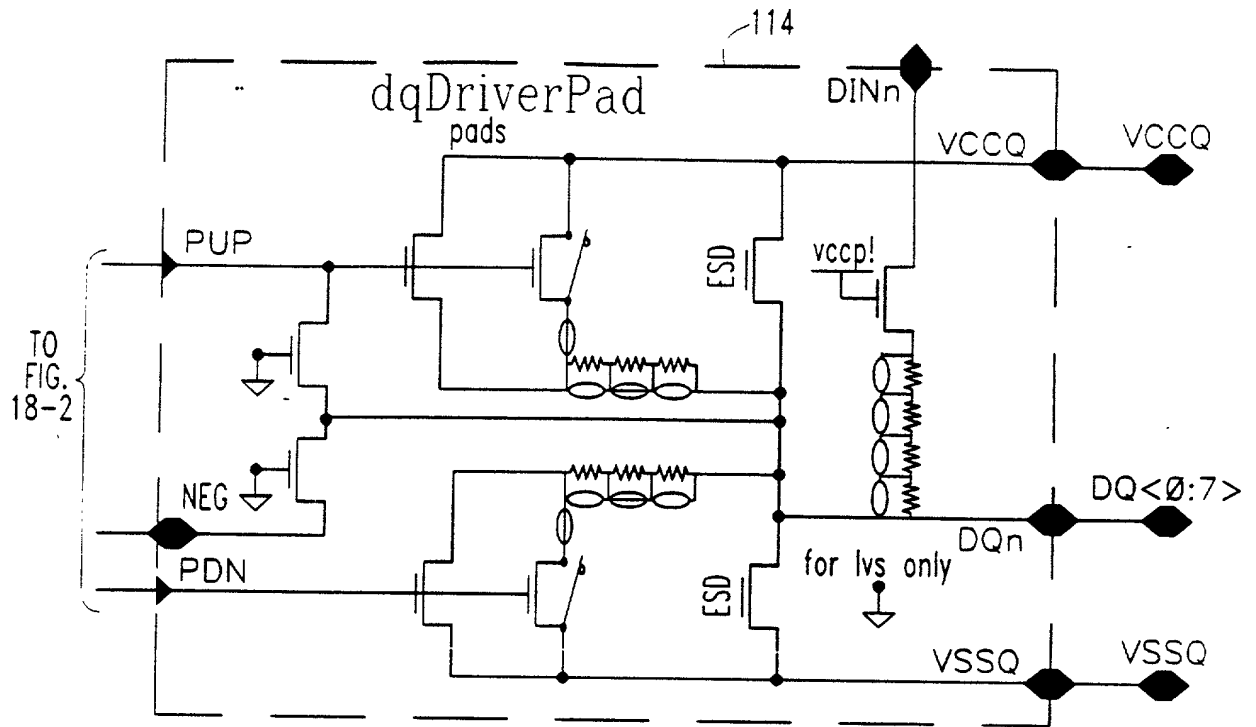


FIG. 20

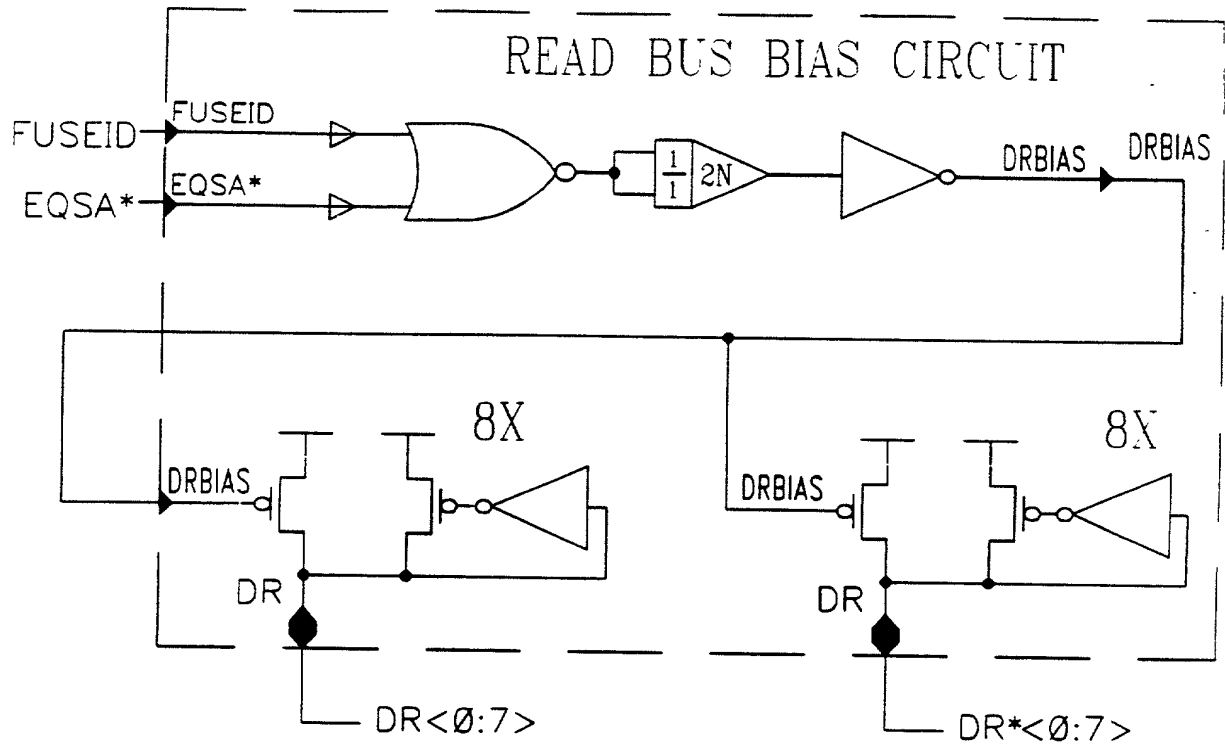
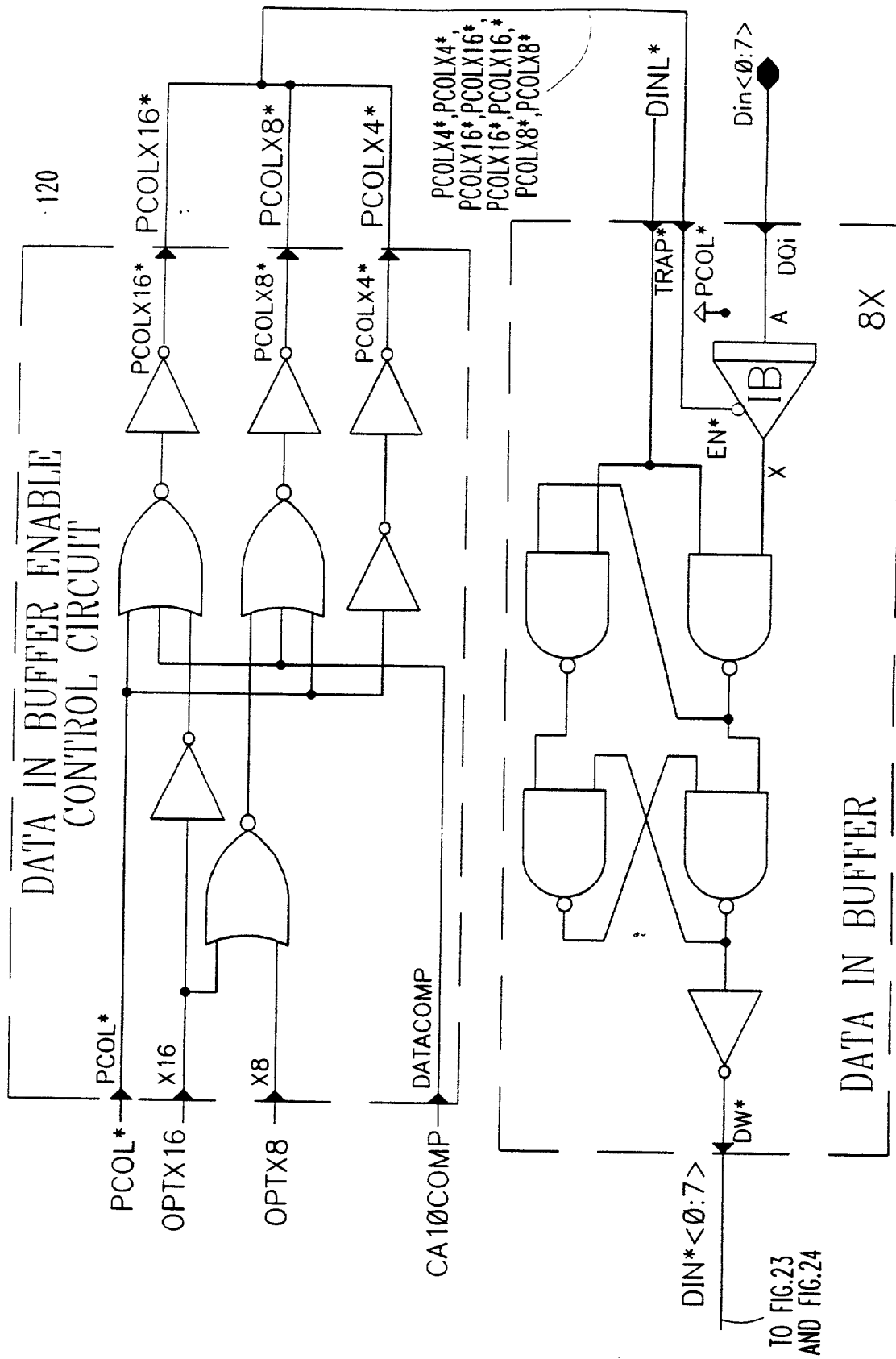
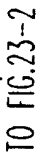


FIG. 21



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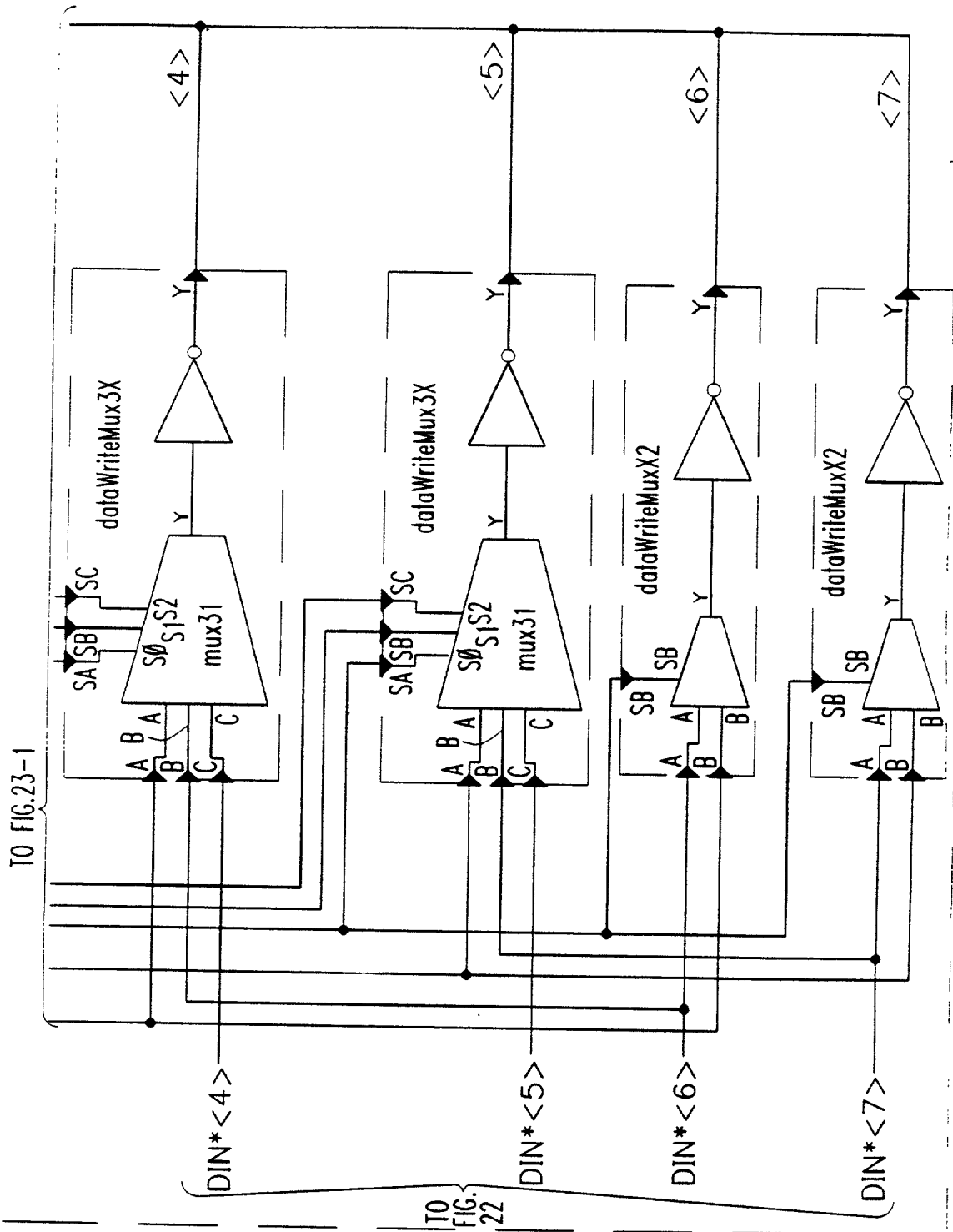
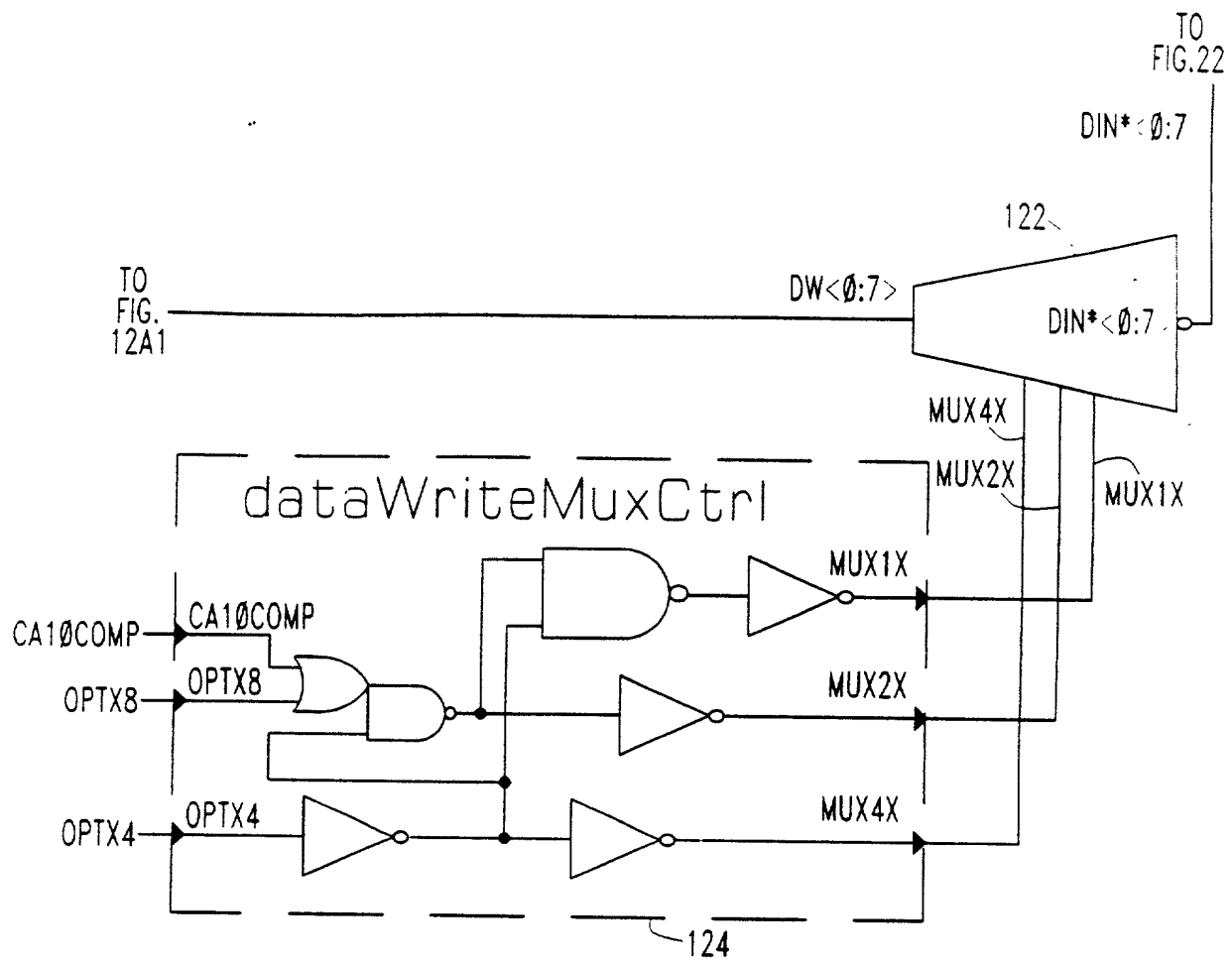


FIG. 23-2



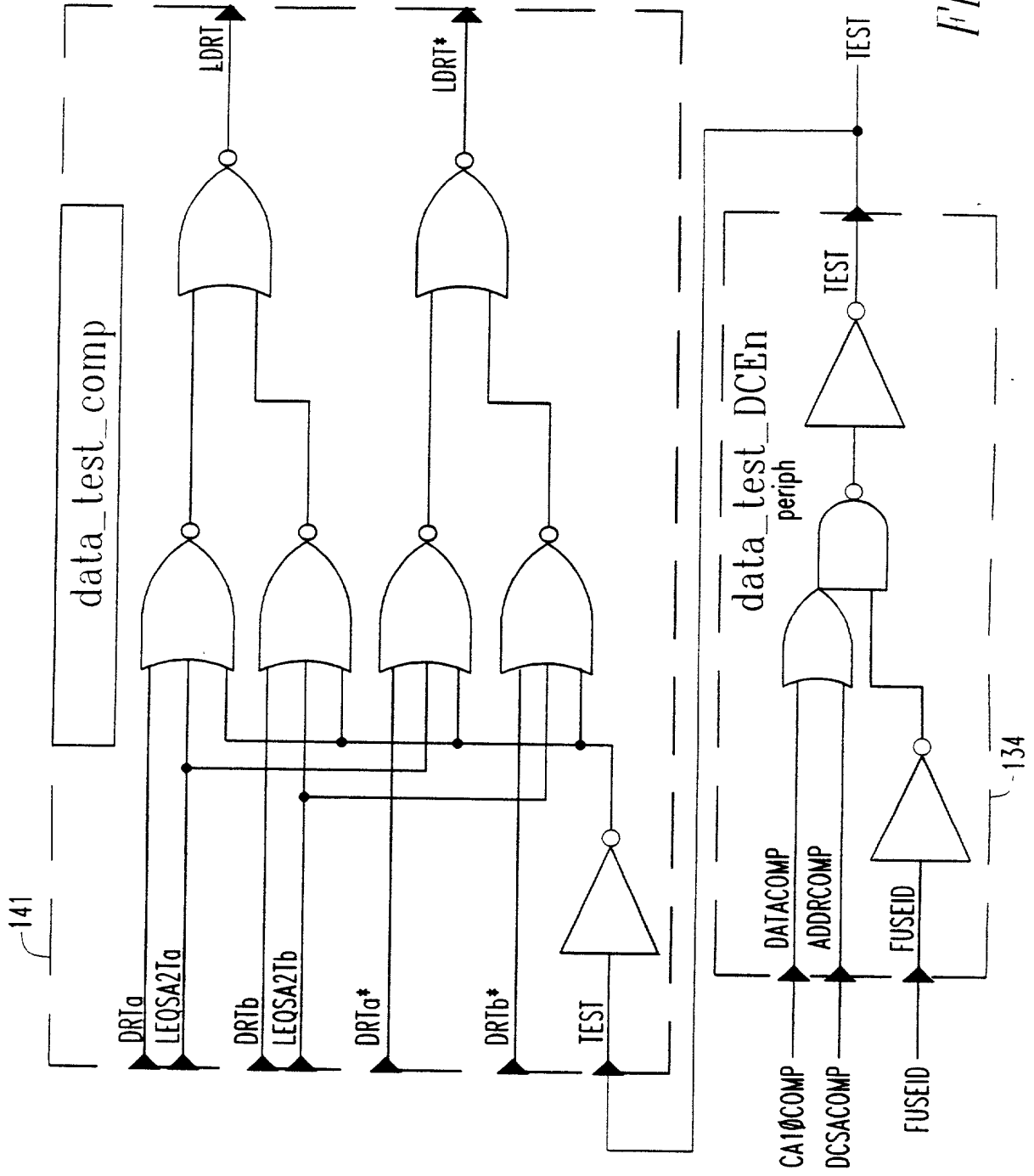


FIG. 25

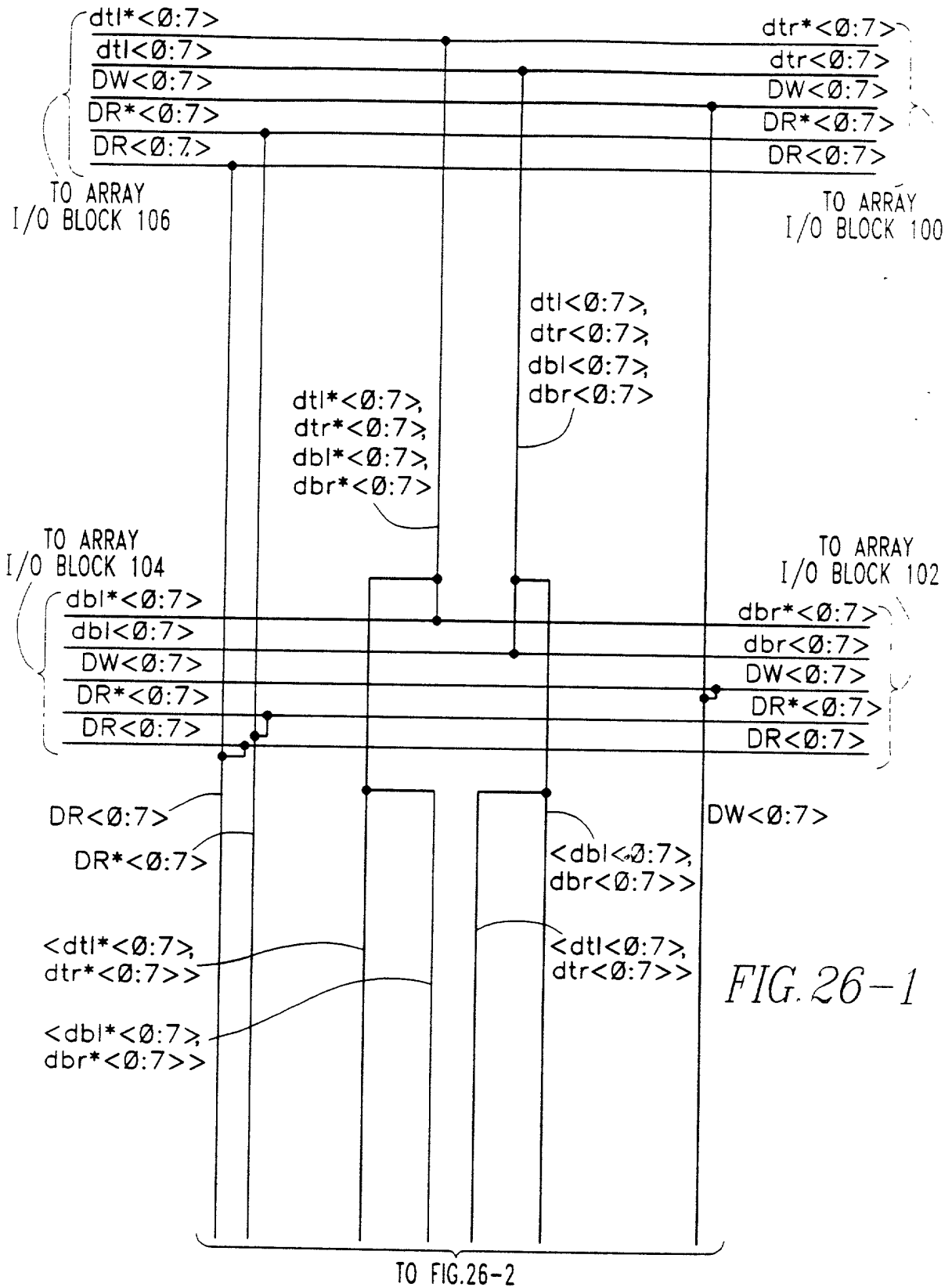


FIG. 26-1

FROM FIG.26-1

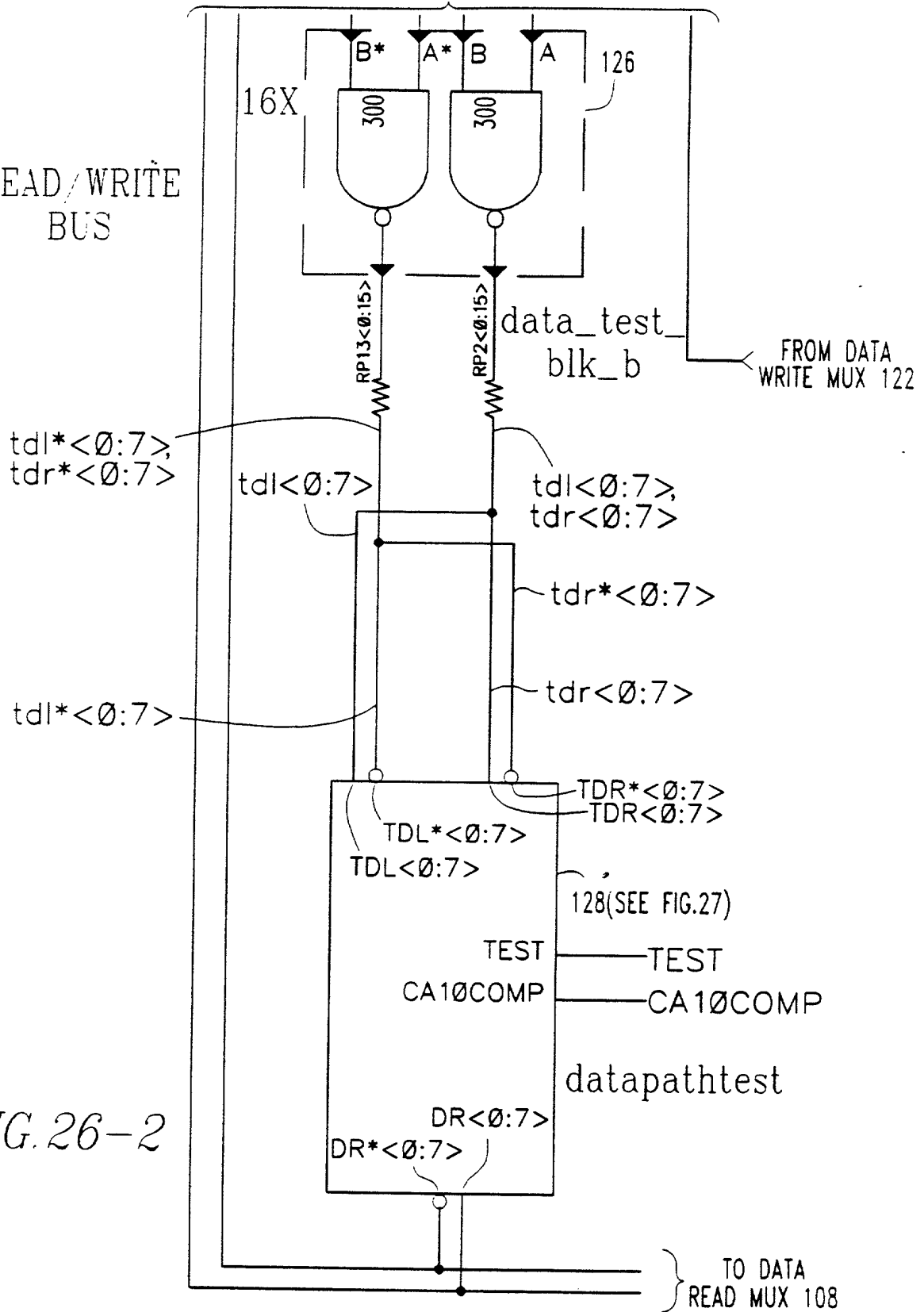
READ/WRITE
BUS

FIG.26-2

FIG. 27-1

CA10COMP

TEST

TDL<0:7>

TDL*<0:7>

<0>

<1>

<2>

<3>

<4>

<5>

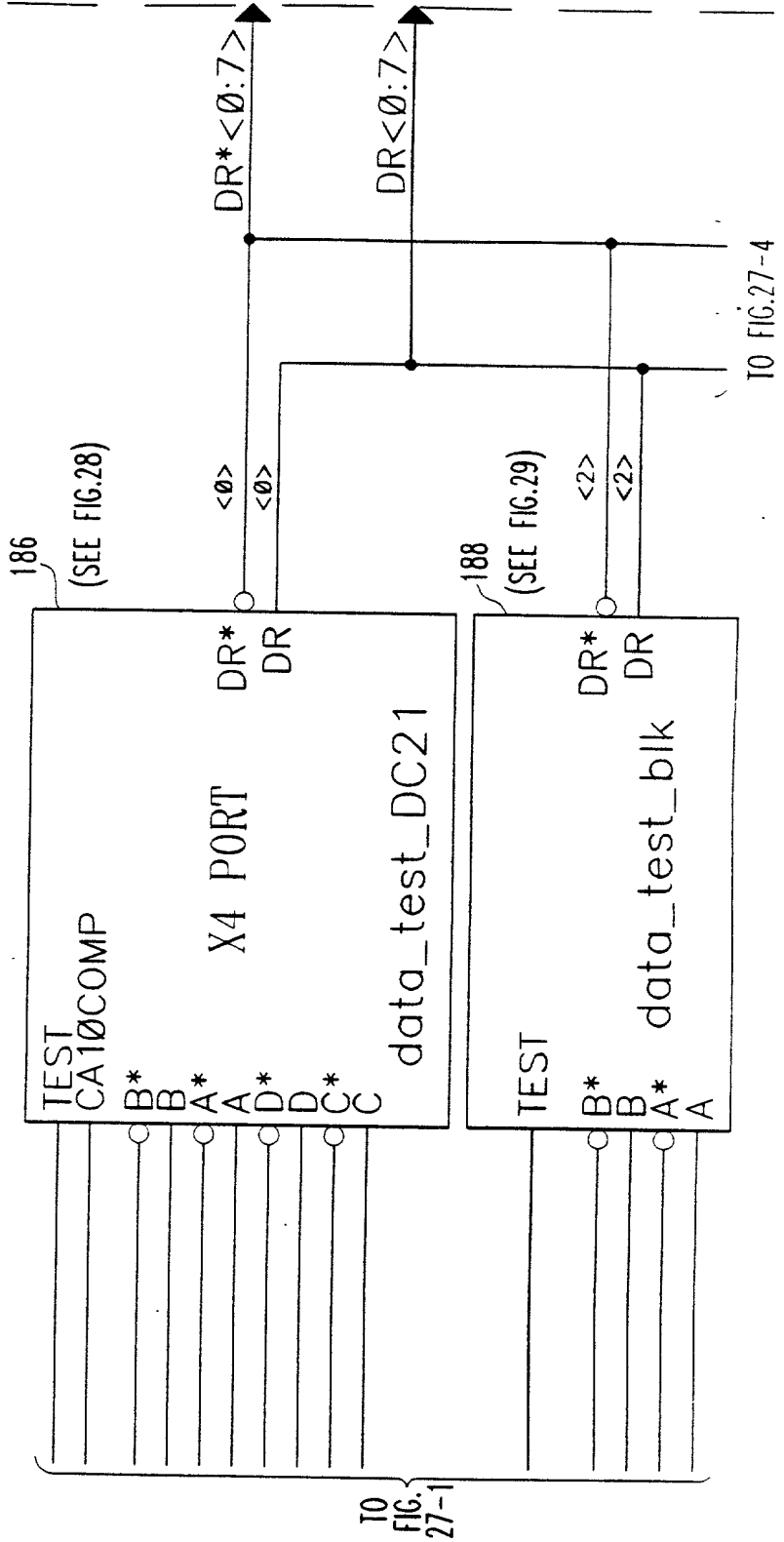
<6>

<7>

10 FIG. 27-3

FIG. 27-2

dataPathTest
Block 128



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TO
FIG.
27-4

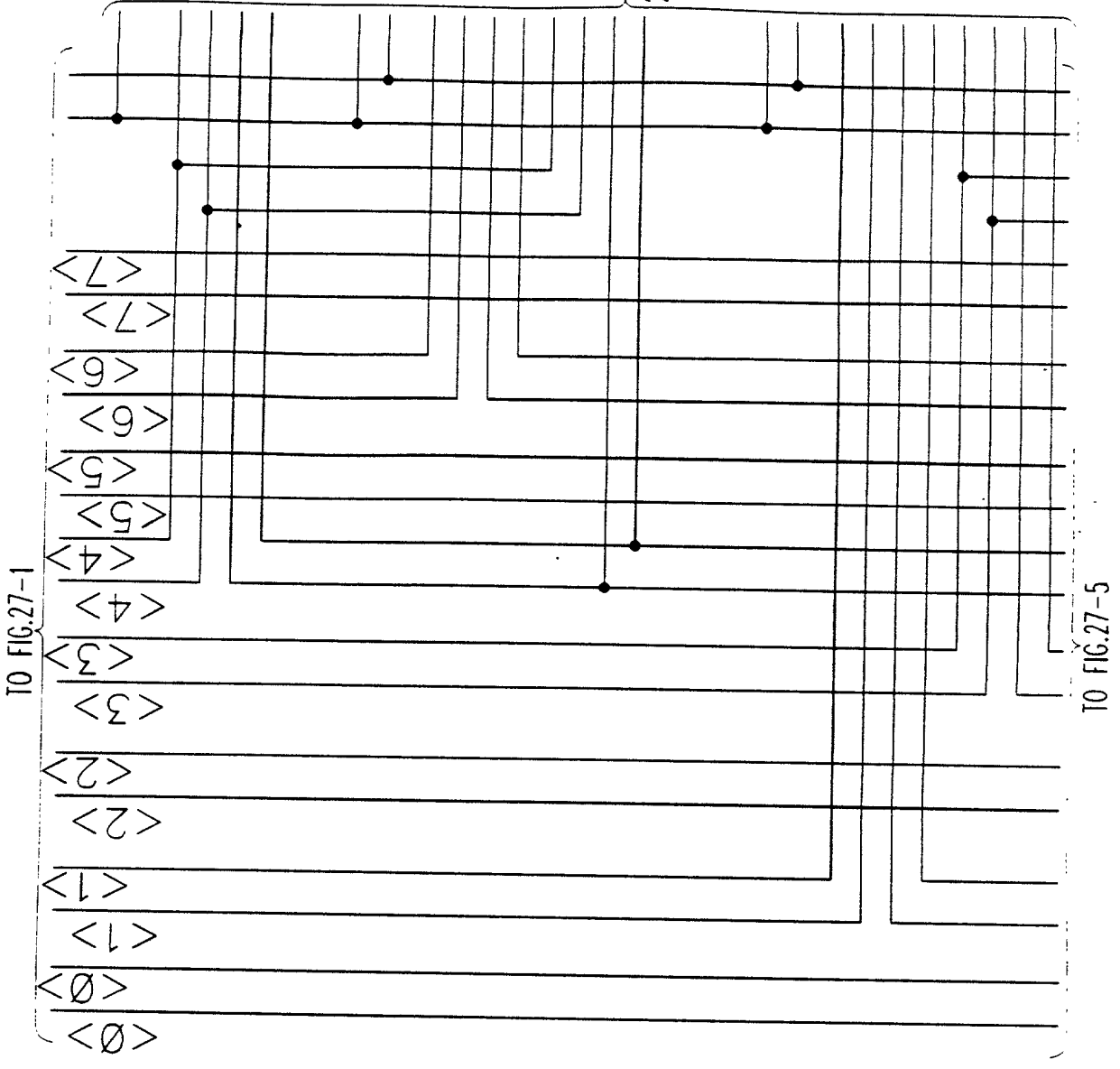


FIG. 27-3

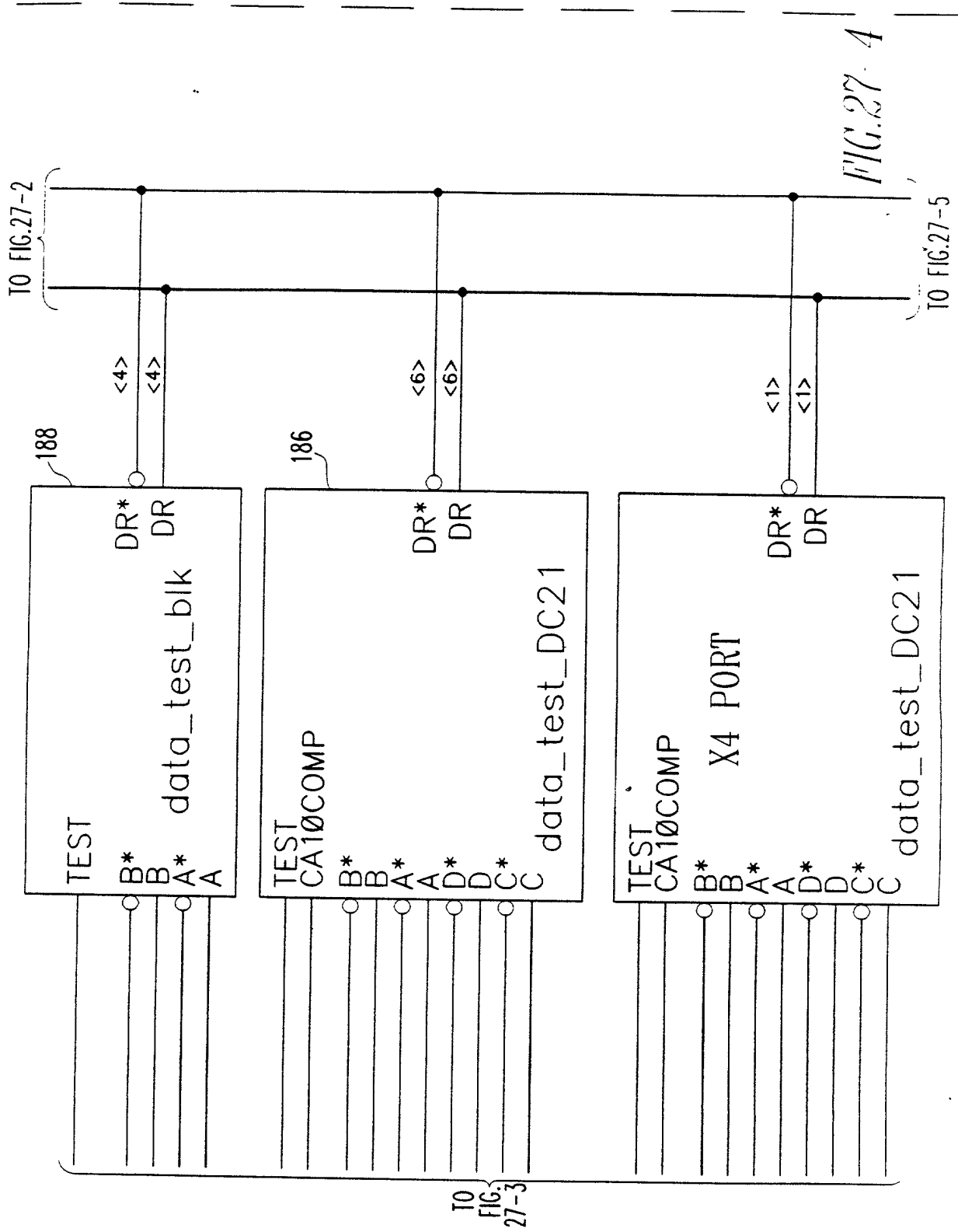
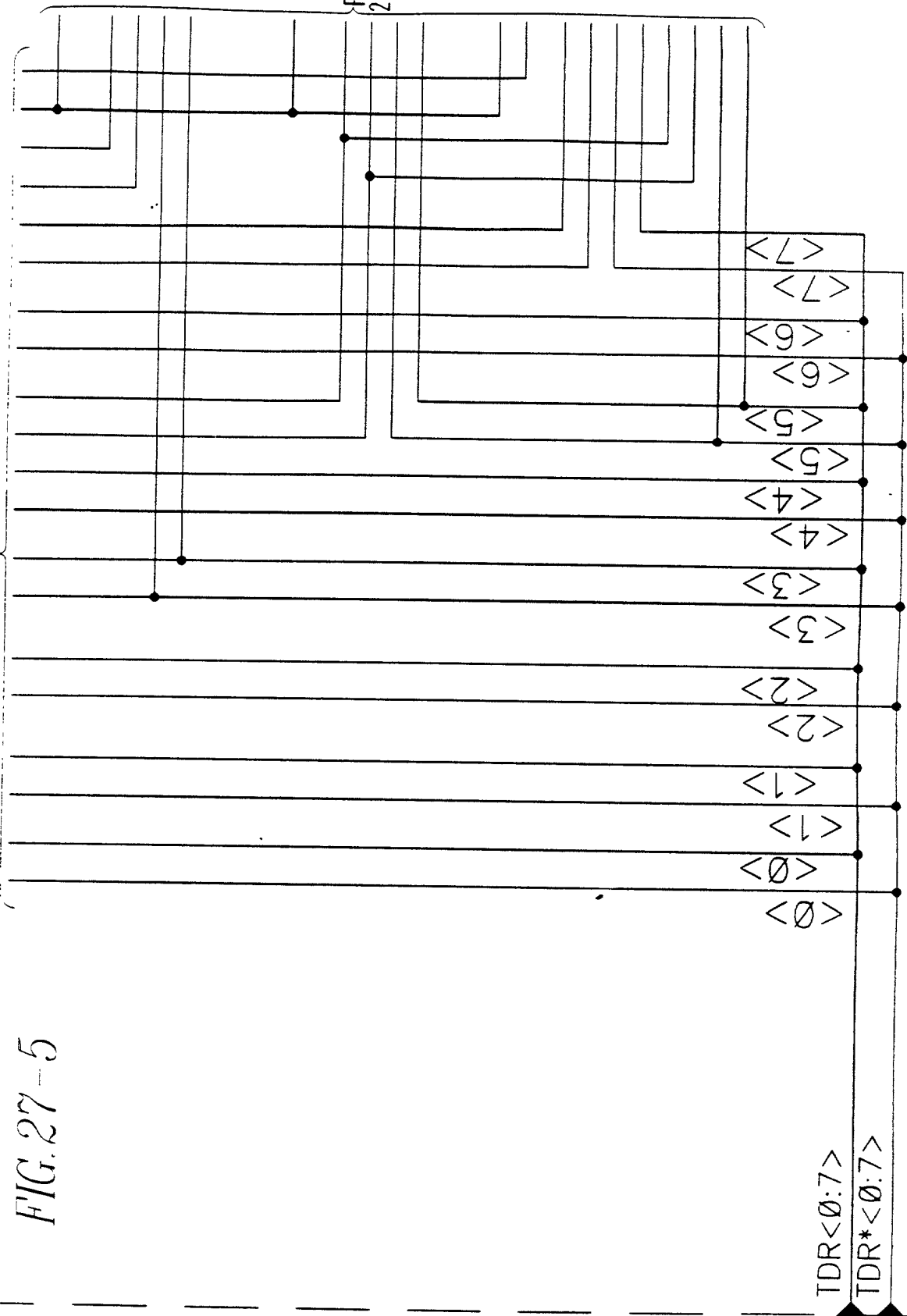


FIG. 27-5

IO FIG. 27-3



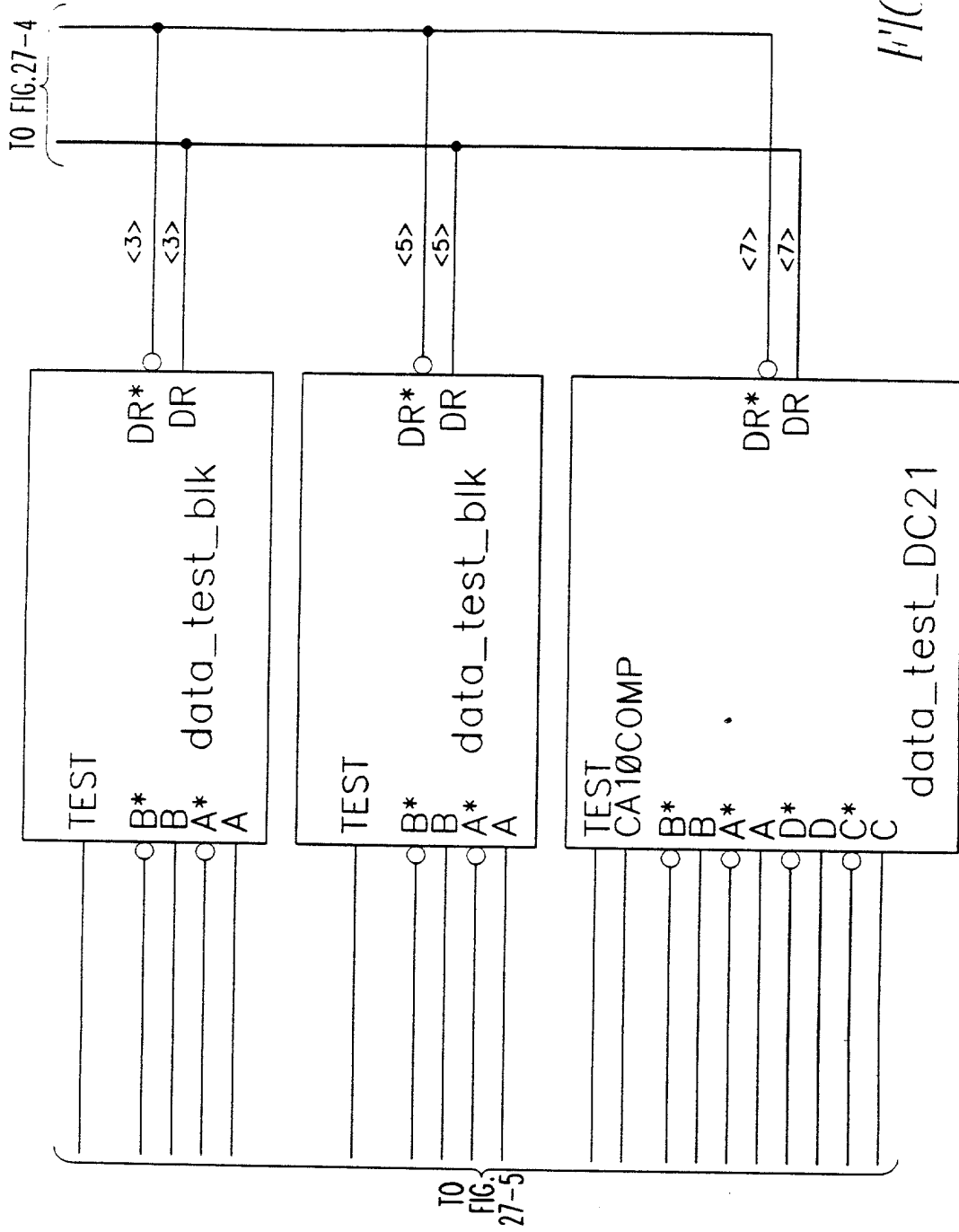


FIG. 27-6

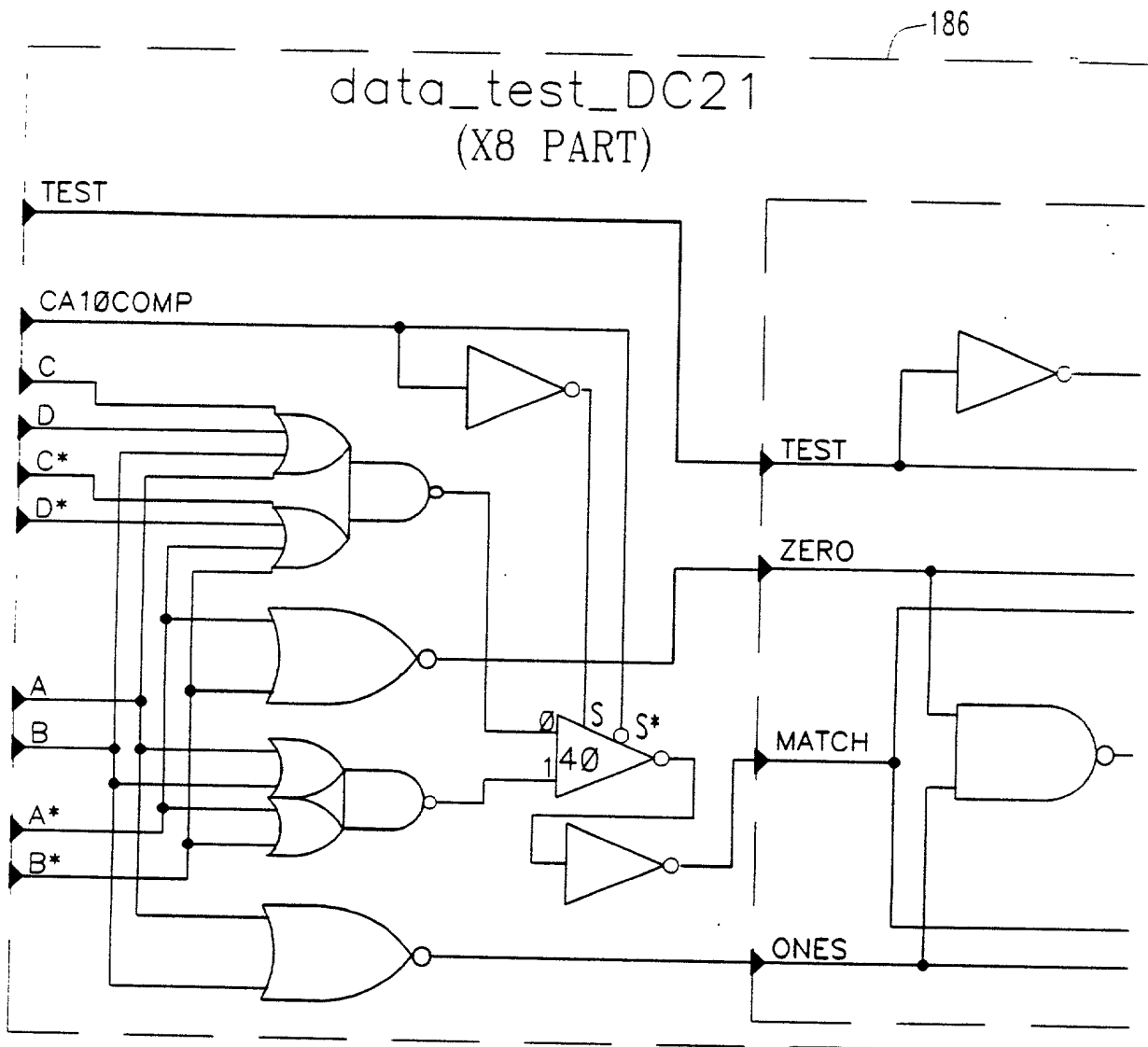


FIG. 28-1

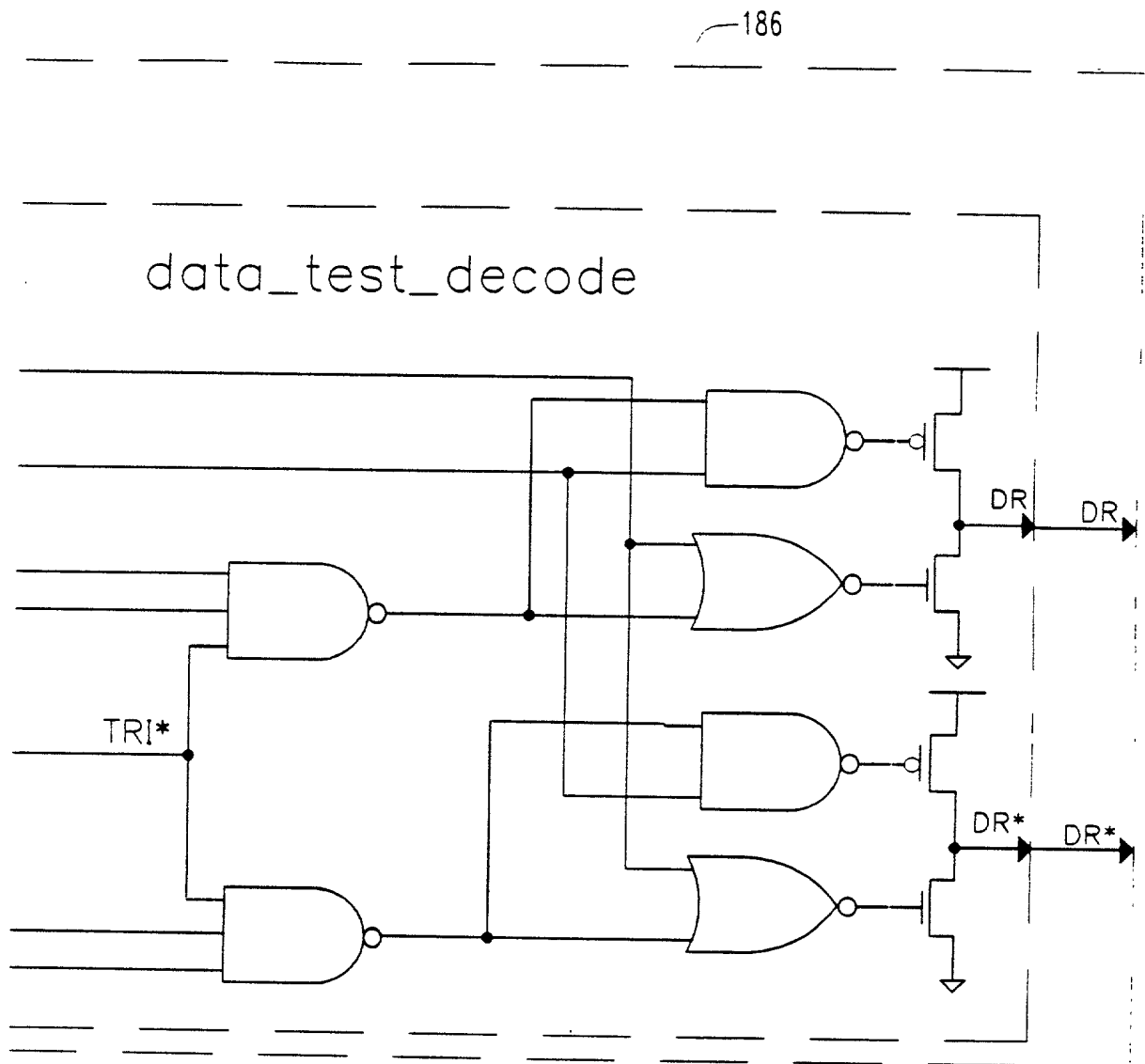


FIG. 28-2

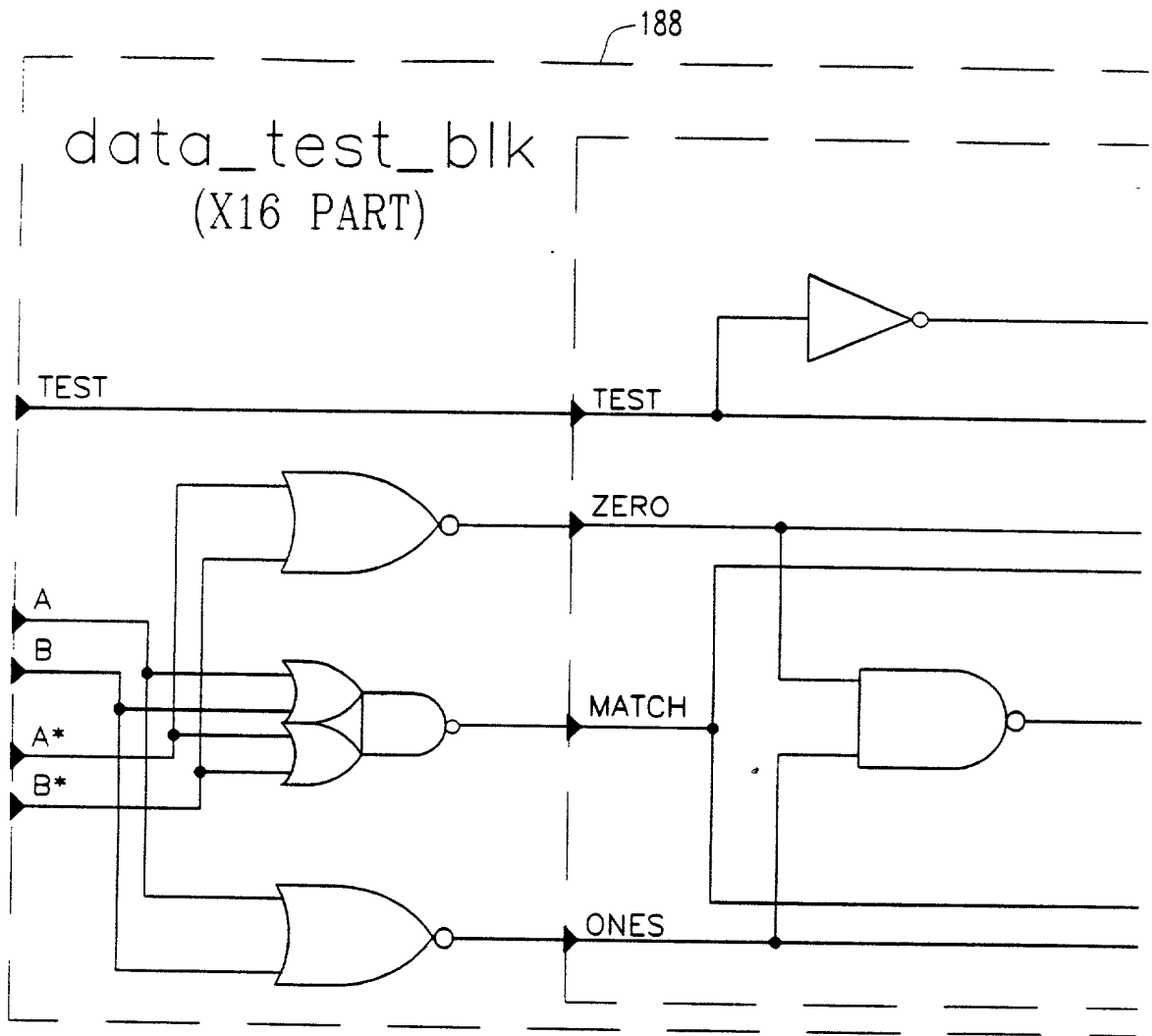


FIG. 29-1

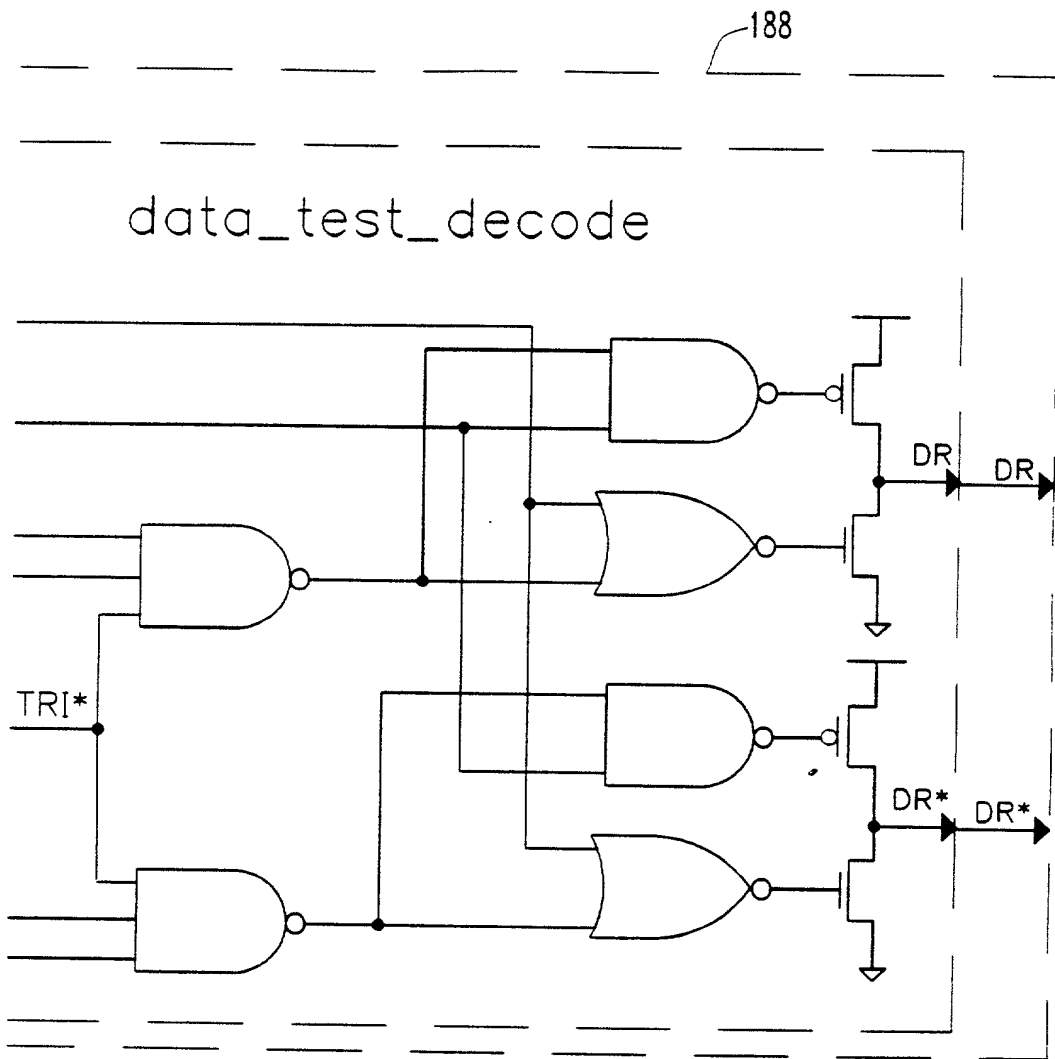
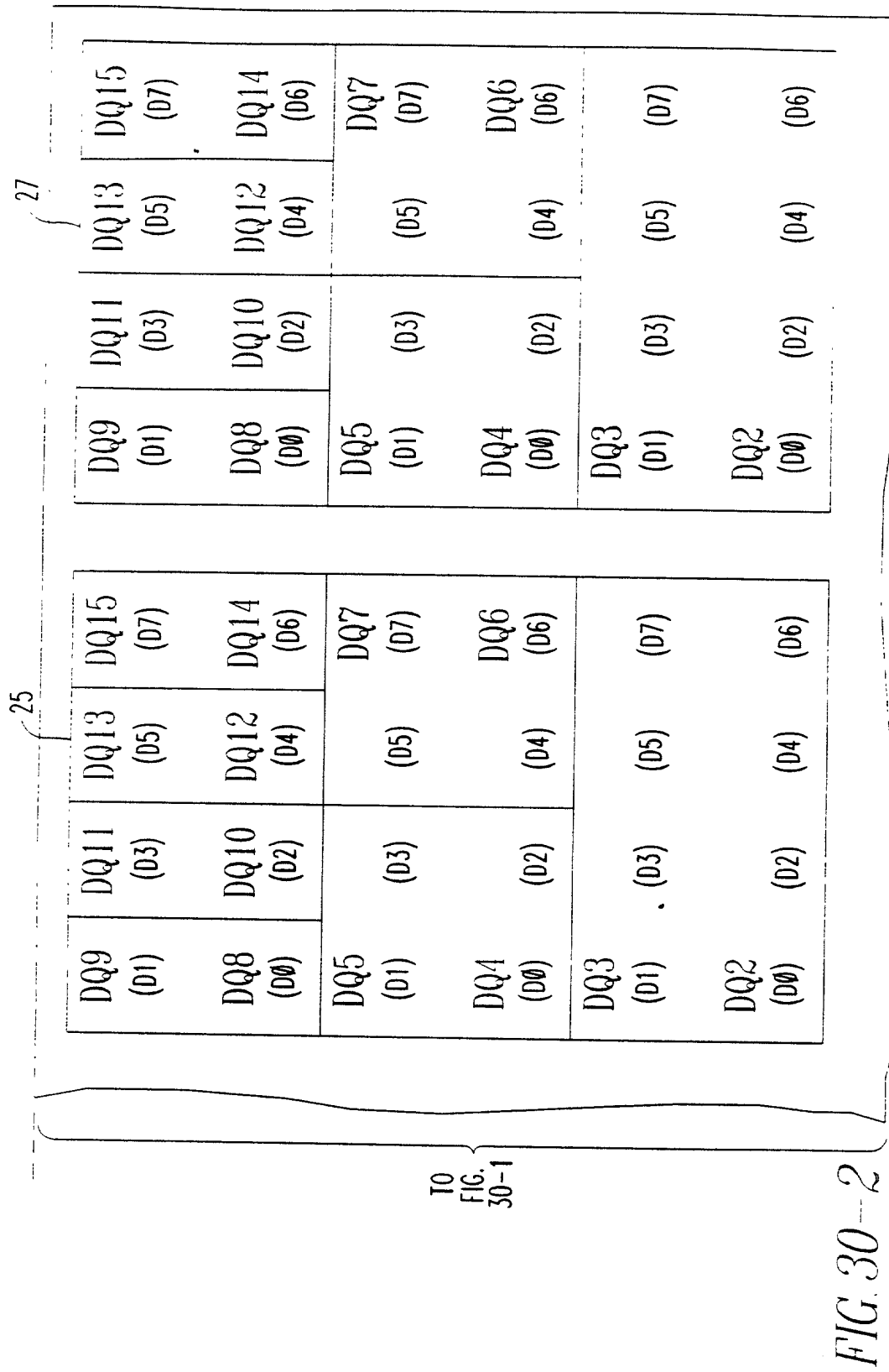


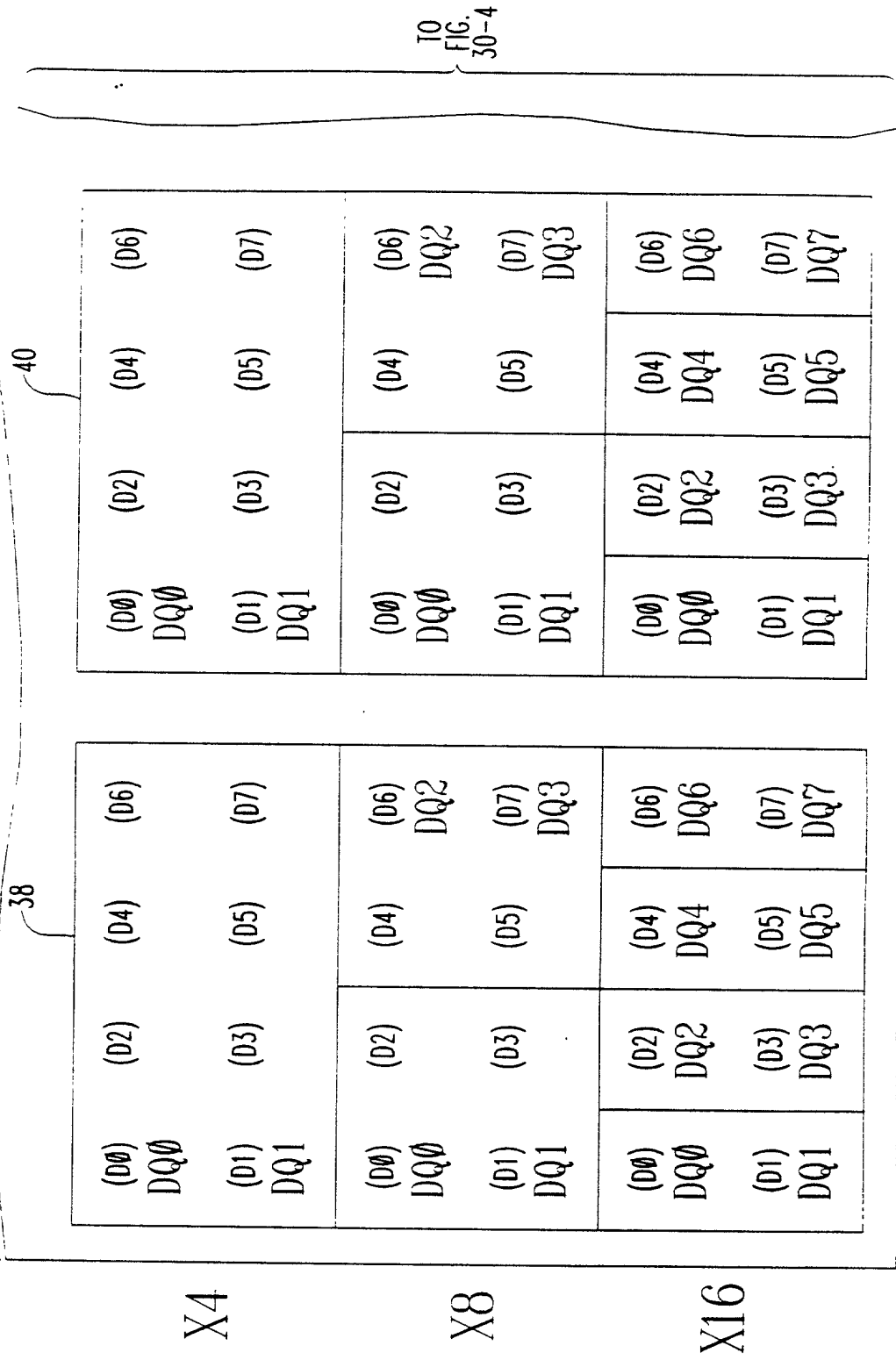
FIG. 29-2

TO FIG. 30-3



10 FIG. 30-4

TO FIG. 30-1



TO FIG. 30-2

31			(D0) DQ2	(D2)	(D4)	(D6)
			(D1) DQ3	(D3)	(D5)	(D7)
33			(D0) DQ4	(D2)	(D4)	(D6) DQ6
			(D1) DQ5	(D3)	(D5)	(D7) DQ7
			(D0) DQ8	(D2) DQ10	(D4) DQ12	(D6) DQ14
			(D1) DQ9	(D3) DQ11	(D5) DQ13	(D7) DQ15

TO
FIG.
30-3

FIG. 30-1

X4	VSSQ	N/C	VSSQ	N/C	N/C	
X8	VSSQ	DQ3	VSSQ	DQ2	N/C	
X16	VSSQ	DQ7	VSSQ	DQ6	DQ5	
	1	2	3	4	5	6
X16	VCCQ	DQ0	VCCQ	DQ1	DQ2	VCCQ
X8	VCCQ	DQ0	VCCQ	DQ1	N/C	N/C
X4	VCCQ	DQ0	VCCQ	DQ1	N/C	N/C

TO FIG. 31A2

FIG. 31A1

TO FIG. 31A1

N/C	N/C	VSSQ	VSS	DVC2.L Probe	NCSV	VCC1 Probe
N/C	N/C	VSSQ	VSS		NCSV	
VSSQ	DQ4	VSSQ	VSS		NCSV	
12	13	14	15	16	17	18
DQ3	VCCQ	VCCQ	VCCX			WE
N/C	VCCQ	VCCQ	VCCX			WE
N/C	VCCQ	VCCQ	VCCX			WE
				19	20	21
						22
						23

FIG.31A2

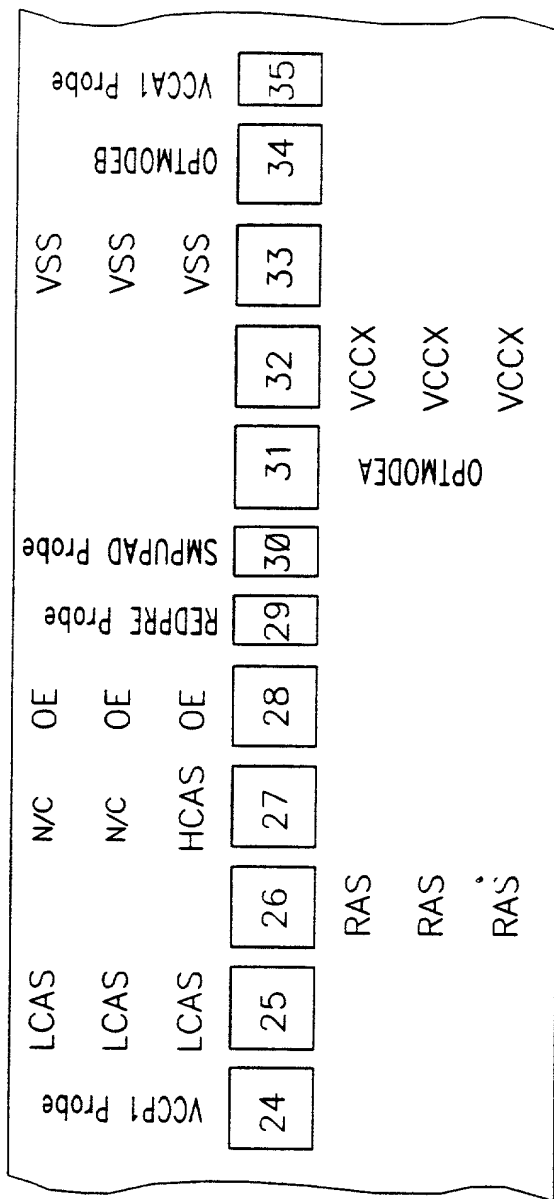


FIG. 31B1

FIG. 31B1

TO FIG. 31B2

TO FIG. 31B1
↓

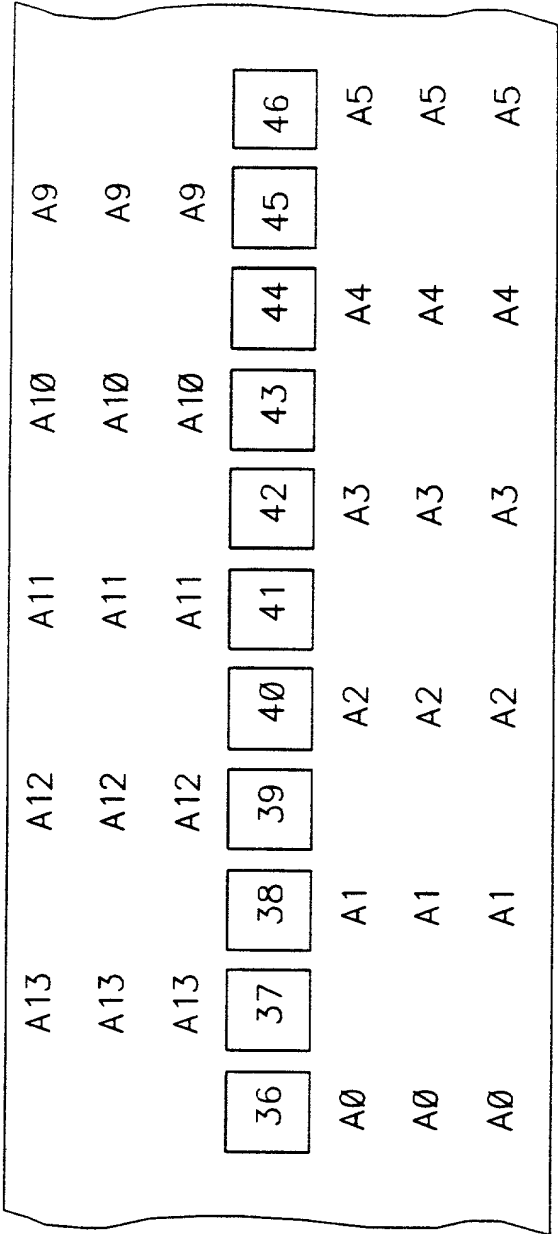


FIG. 31B2

TO FIG. 31C2

FIG. 31C1

[illegible]

FIG. 31C2

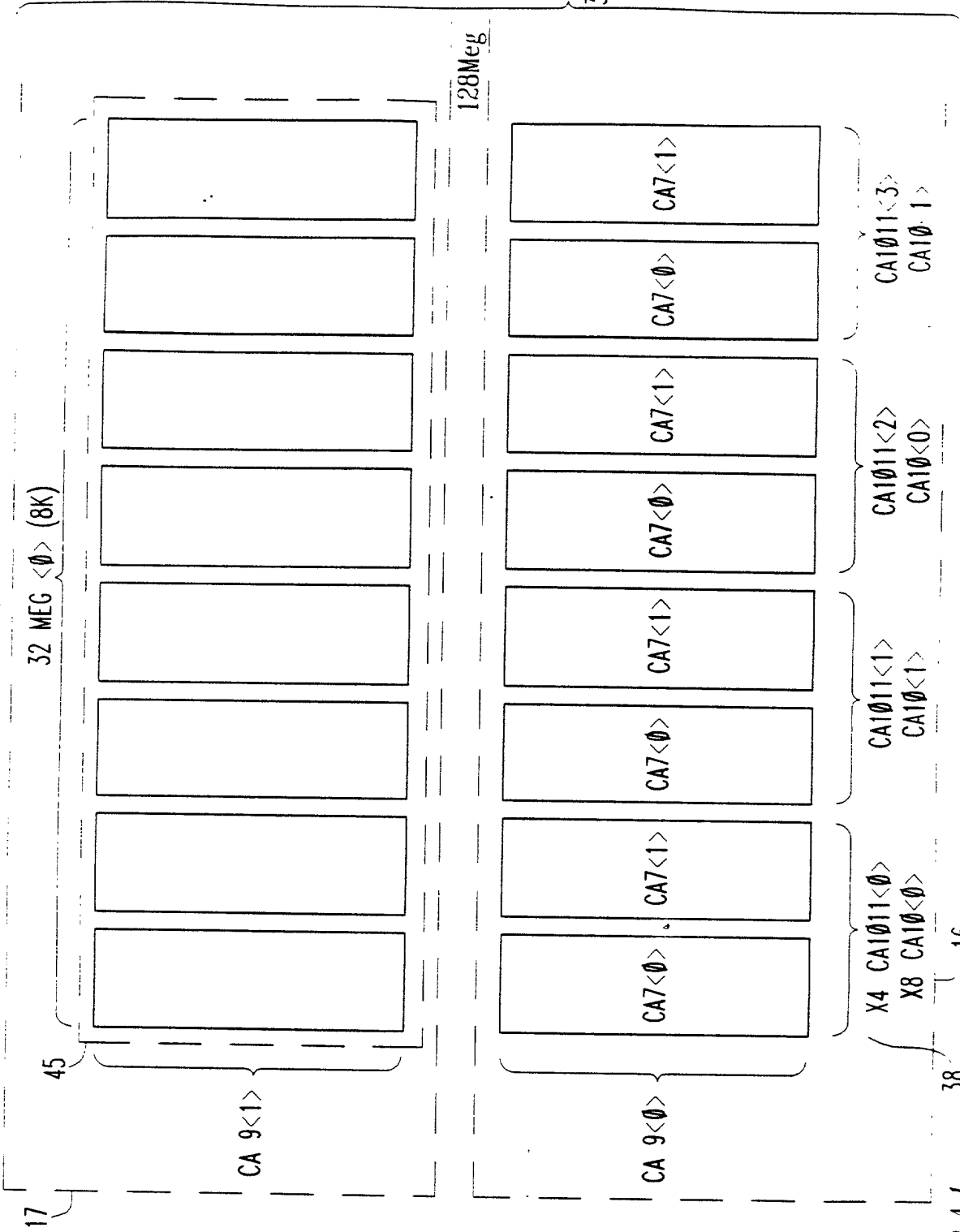


FIG. 32A1

TO
FIG.
32A3

PART TYPE	32MEG
ANY 16K	RA 13
X4 8K OR 4K	CA 12
X8 8K OR 4K	CA 11
X16 8K OR 4K	CA 10

FIG. 32A2

$\left\{ \begin{array}{l} \text{CA } 6 \langle 0:1 \rangle \text{ MSB} \\ \text{CA } 45 \langle 0:3 \rangle \\ \text{CA } 23 \langle 0:3 \rangle \\ \text{CA } 01 \langle 0:3 \rangle \\ \text{CA } 8 \langle 0:1 \rangle \text{ LSB} \end{array} \right.$

32 MEG <1> (8K)

47

FROM
FIG.
32A1

LSB → MSB

40

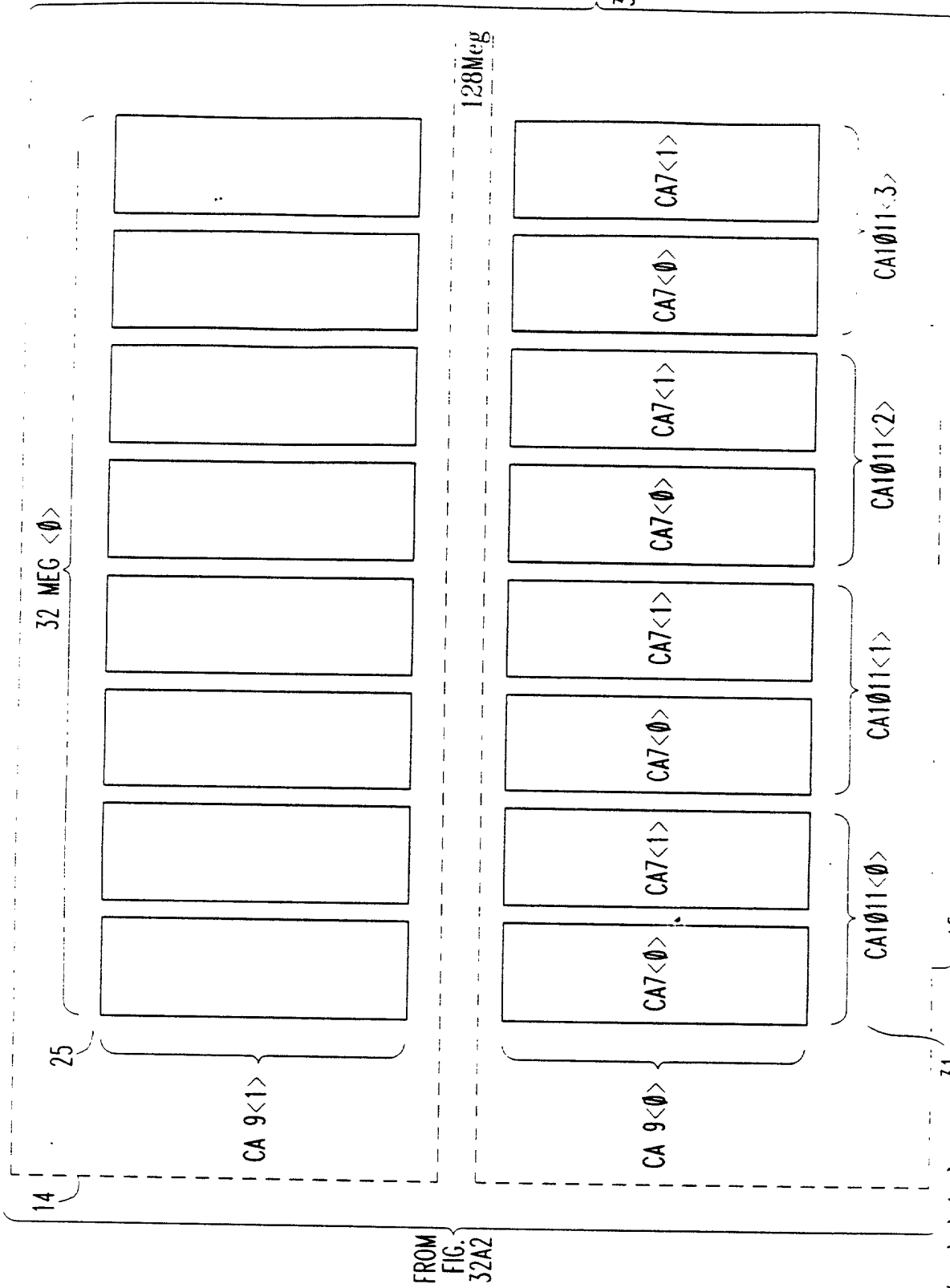
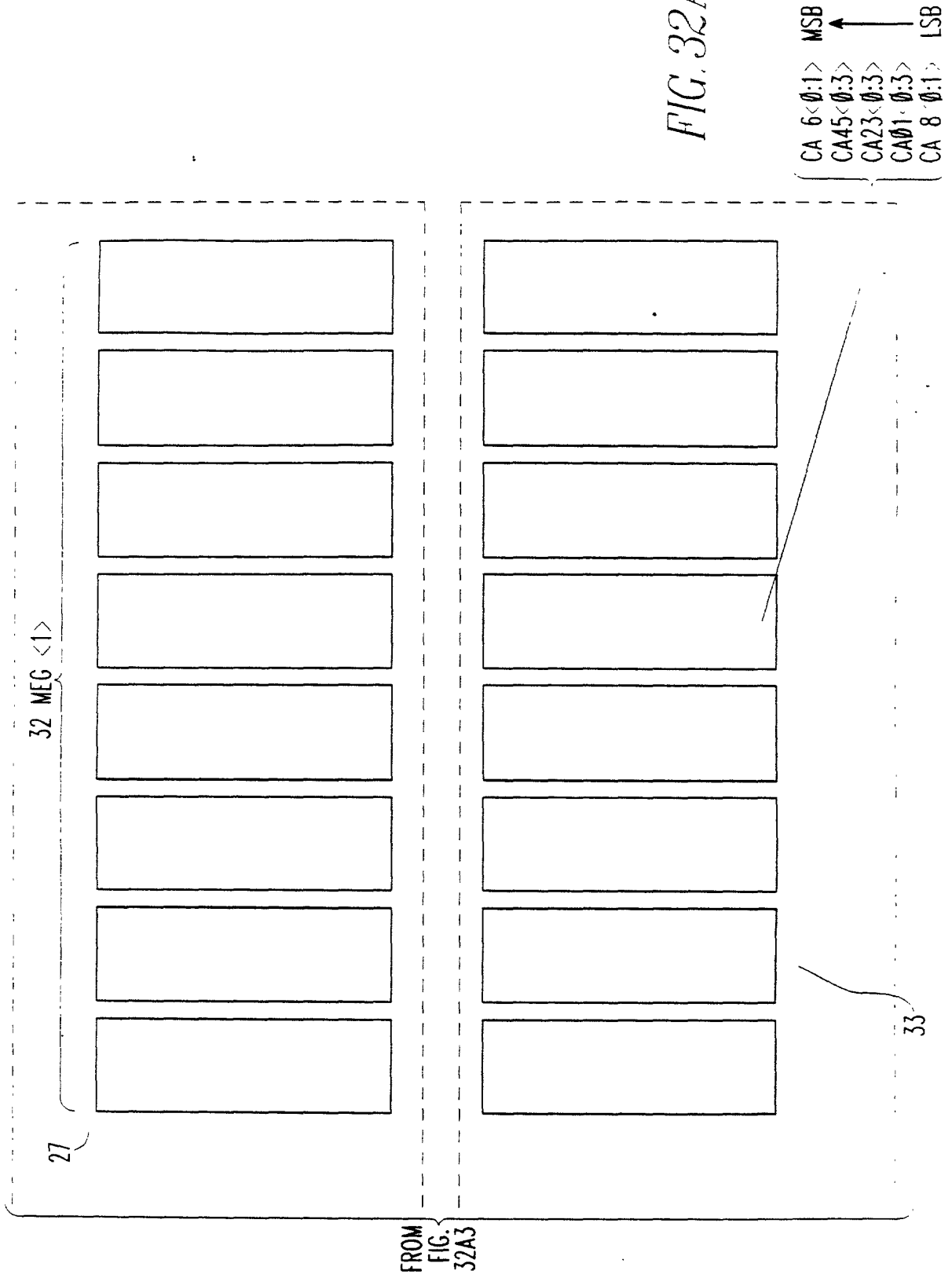


FIG. 32A4



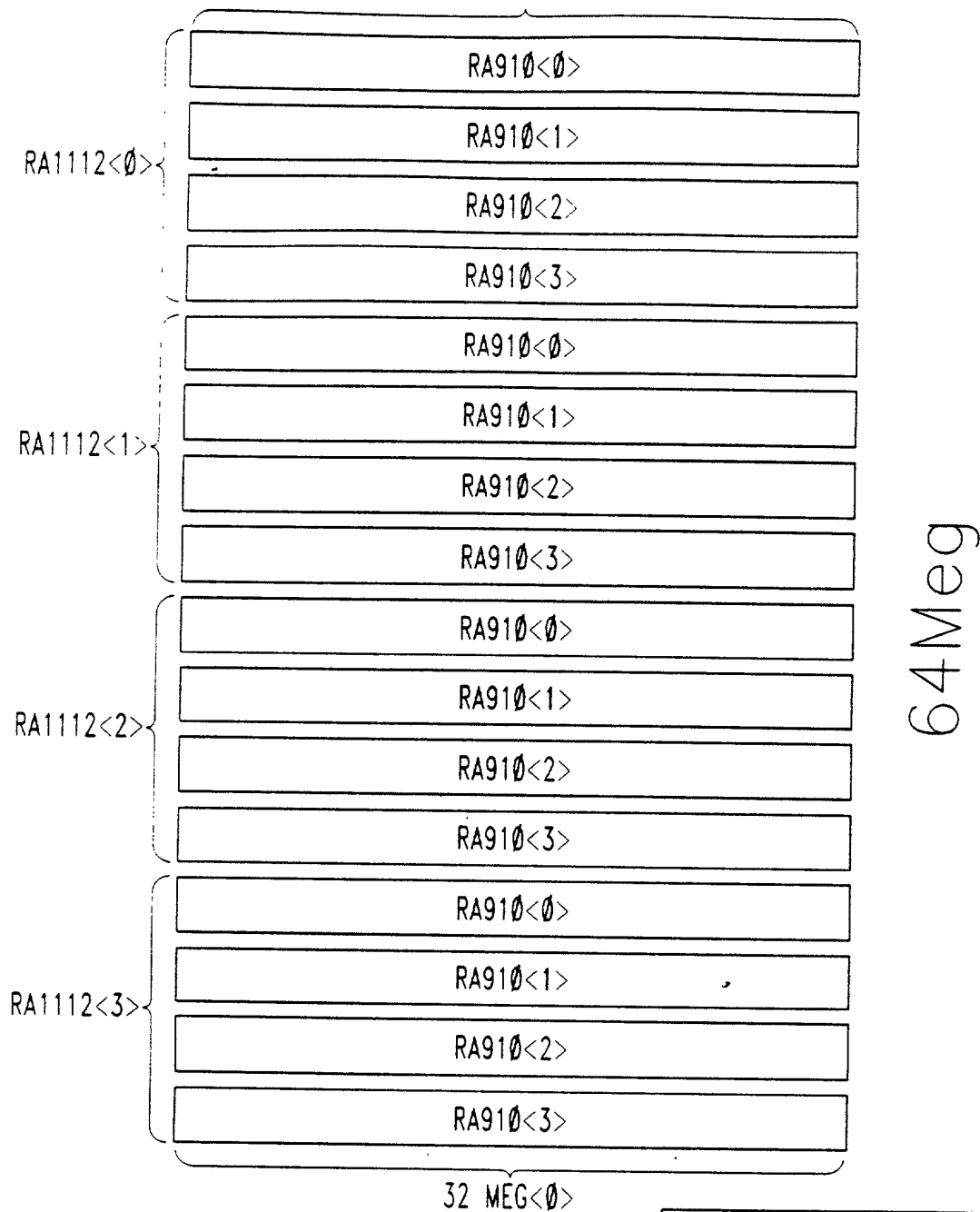


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

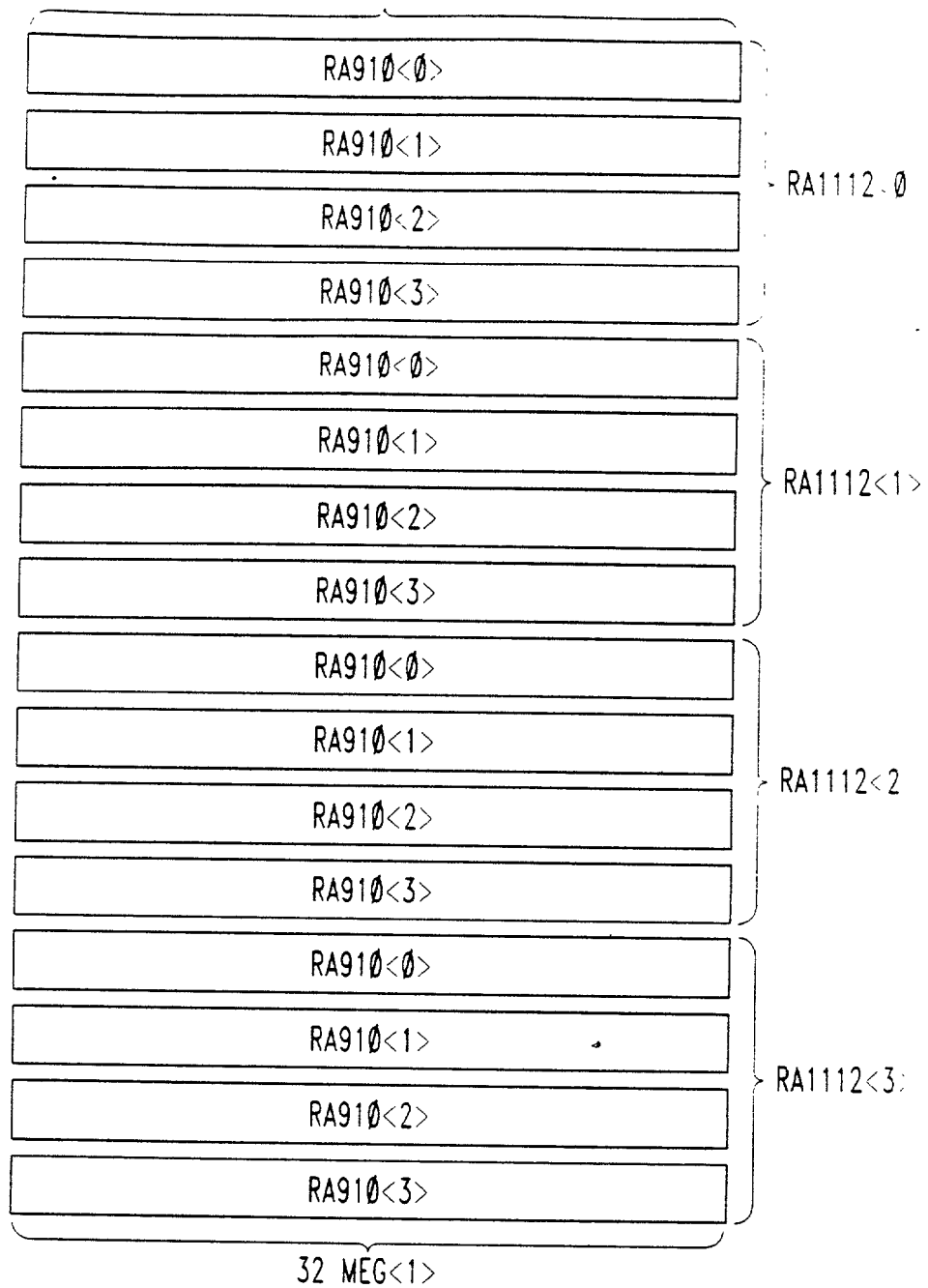
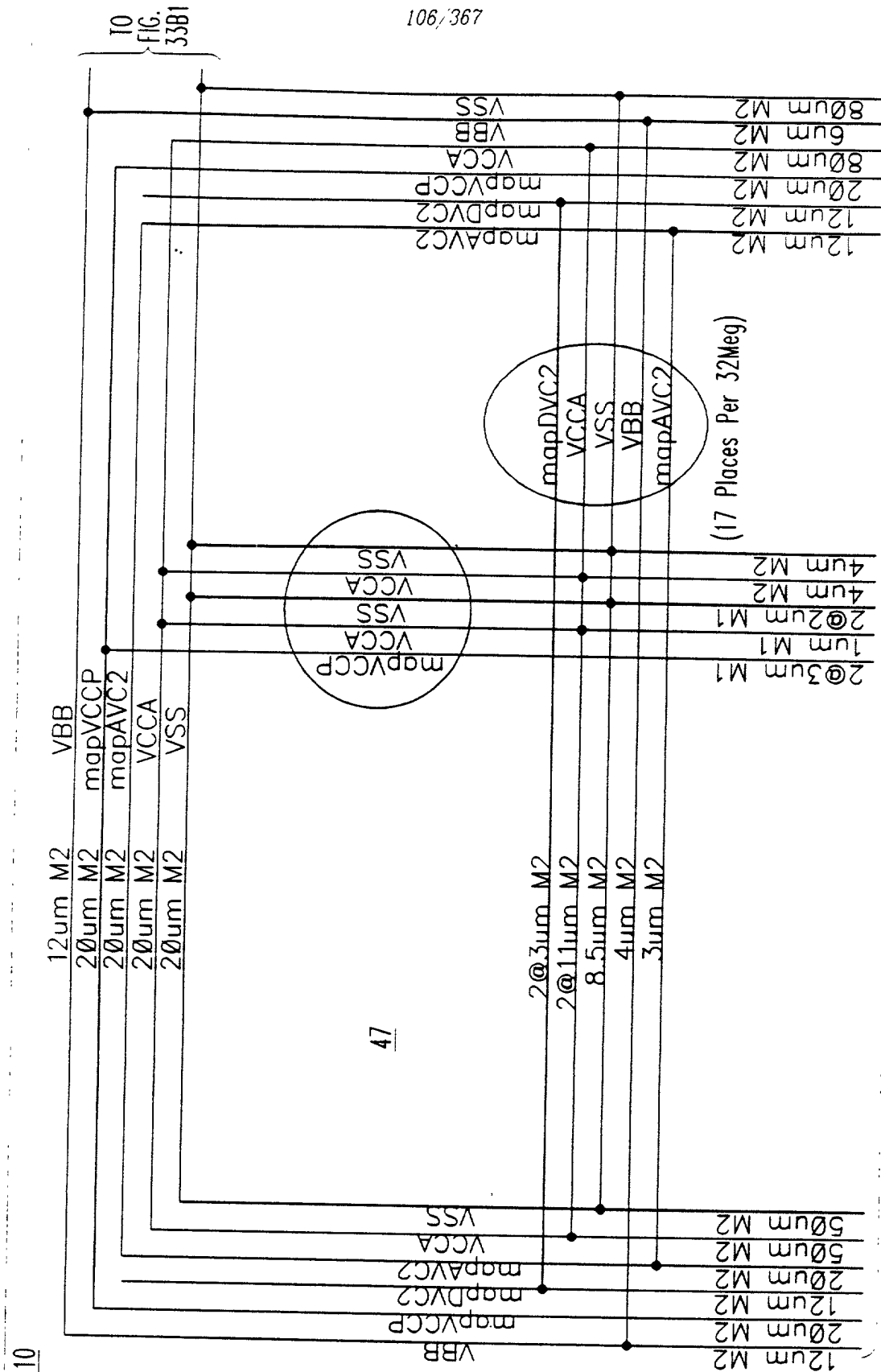


FIG. 32B2



TO FIG. 33A2

146331

FROM FIG. 33A1

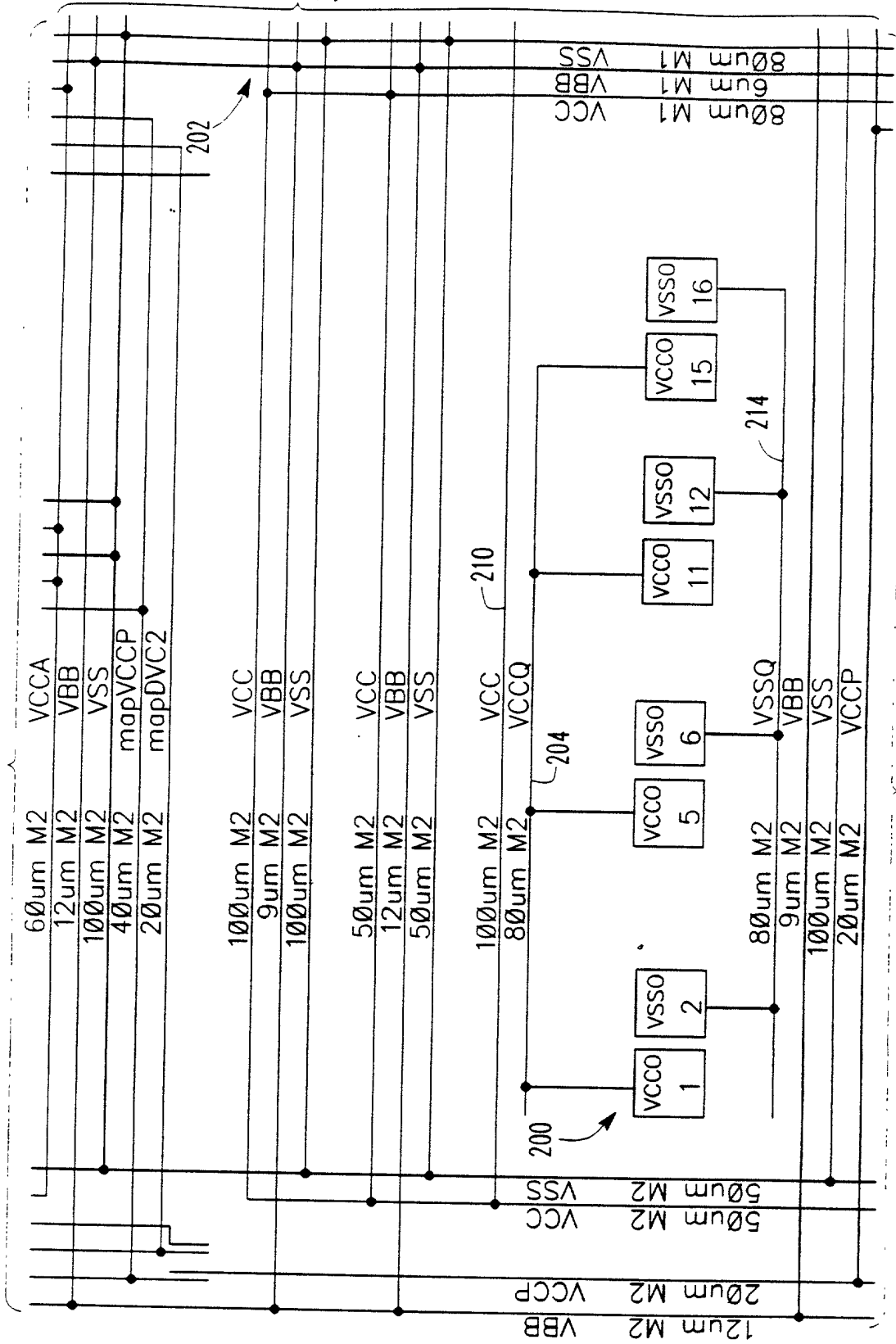
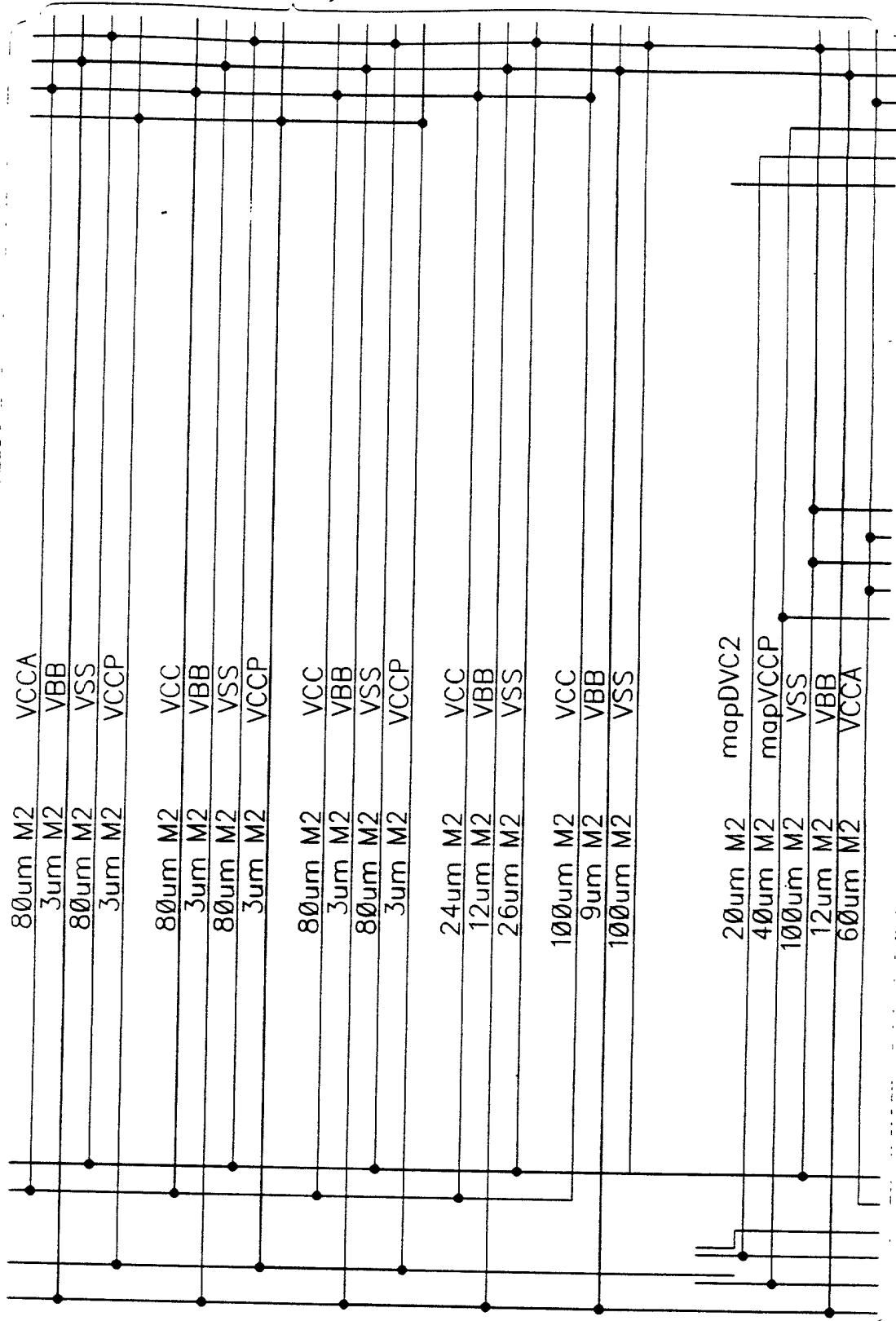


FIG. 33A3

FIG. 33A2

FROM FIG. 33A2



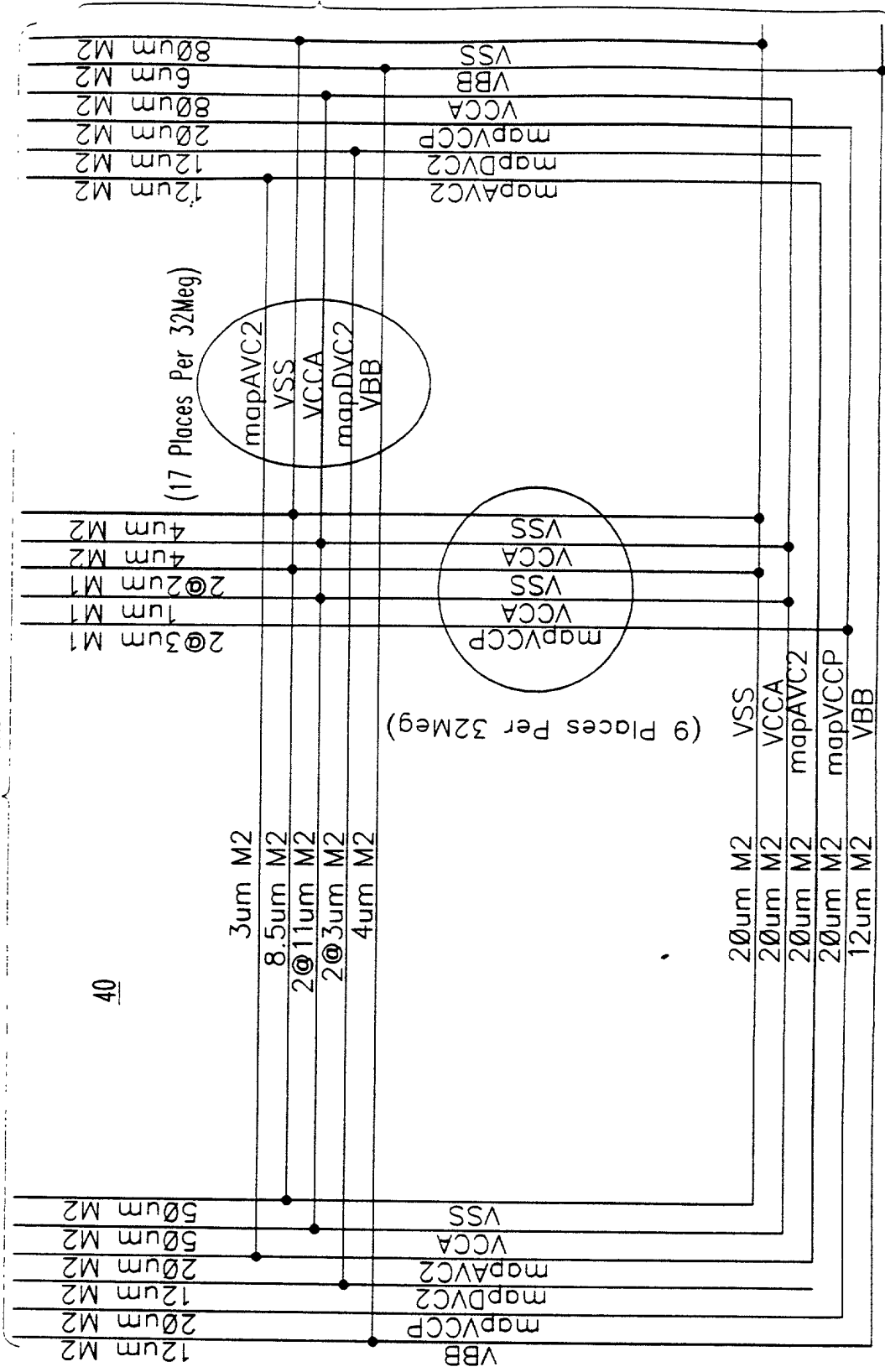
TO FIG. 33A4

FIG. 33A3

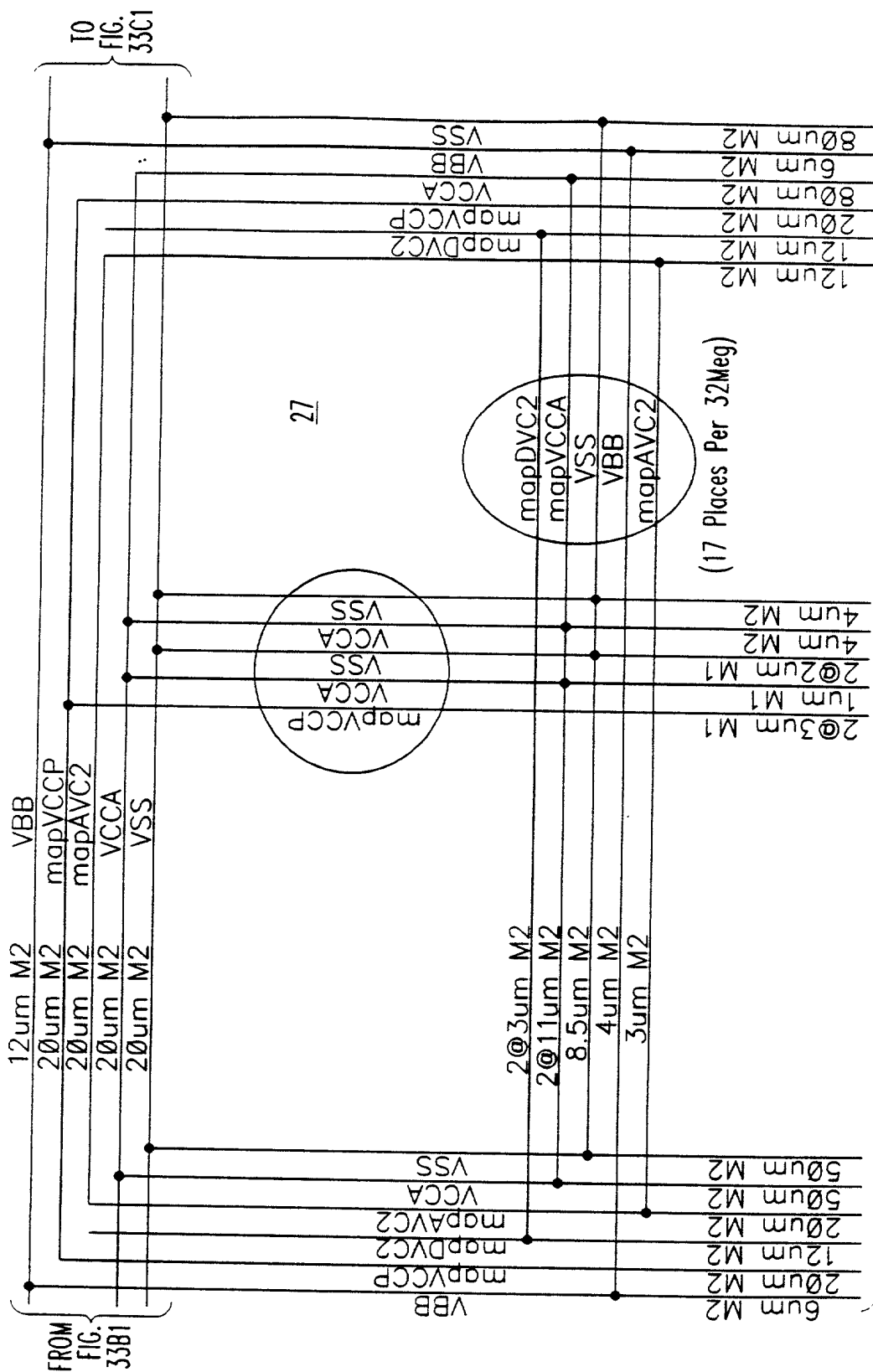
TO
FIG.
33B5

108, 367

FROM FIG. 33A3

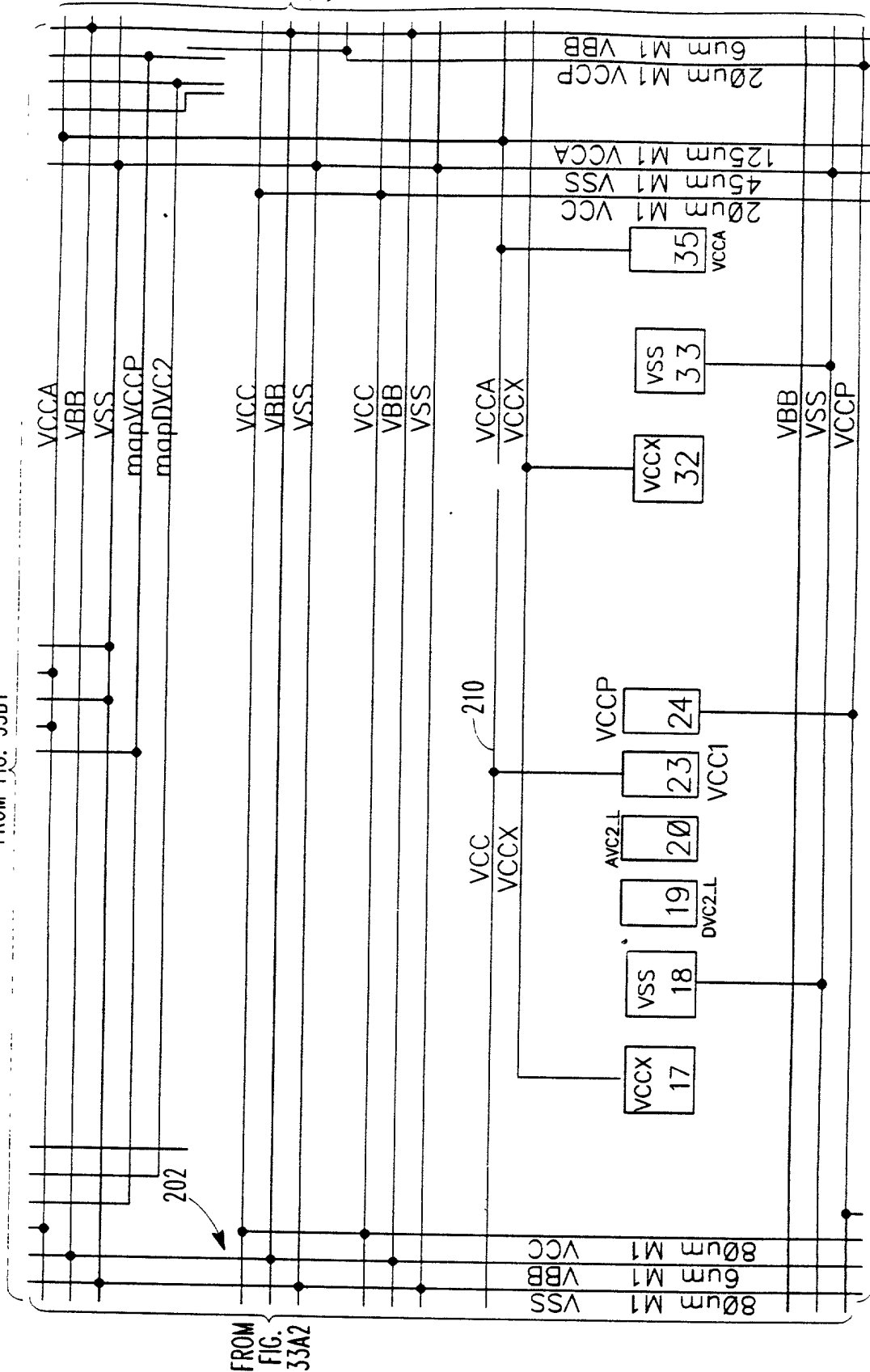


146341



TO FIG. 33B4

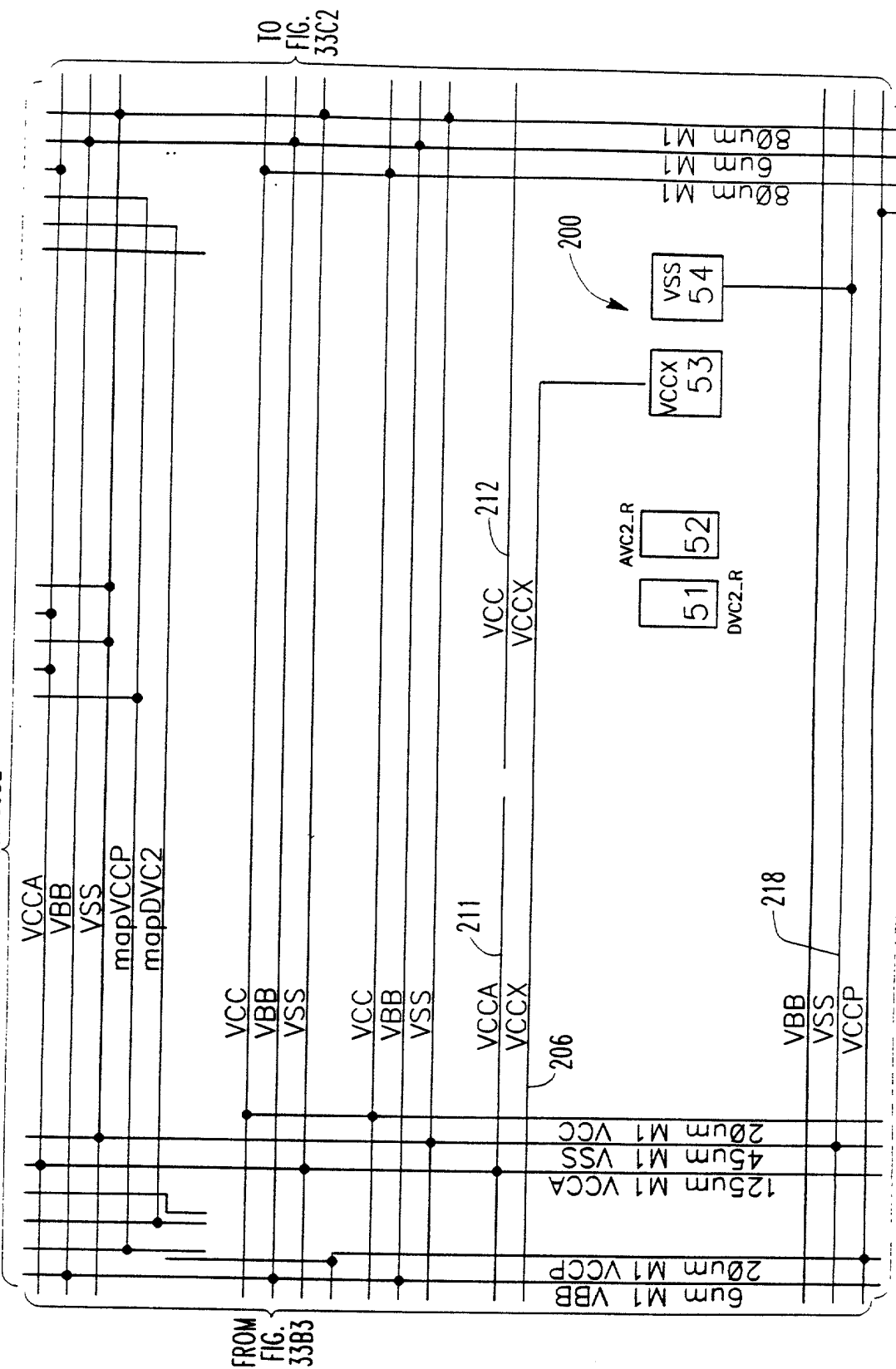
FIG. 33B)



TO FIG. 33B3

116:33/33

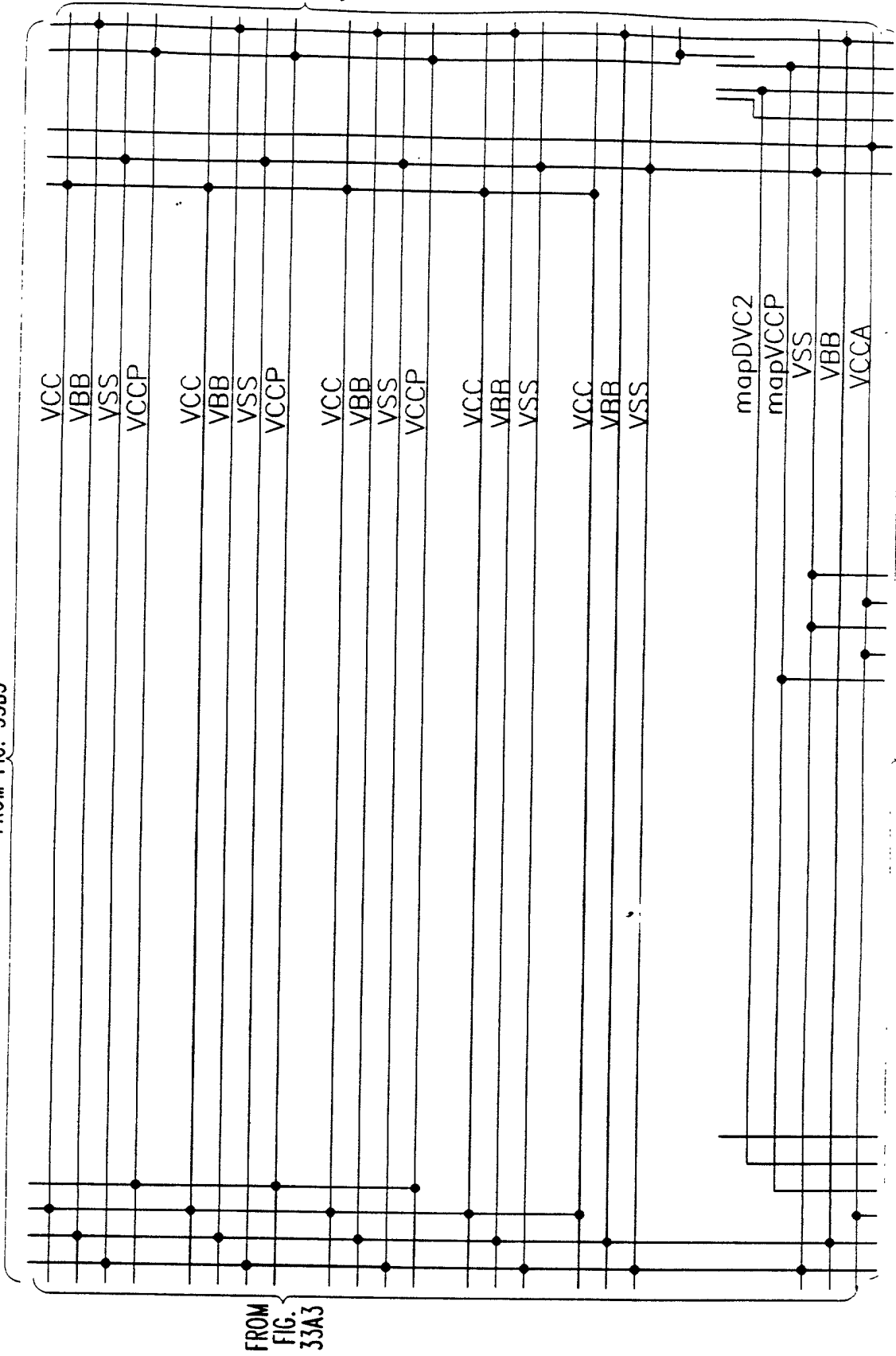
FROM FIG. 33B2



TO FIG. 33B6

FIG. 33B1

FROM FIG. 33B3



FROM
FIG.
33A3

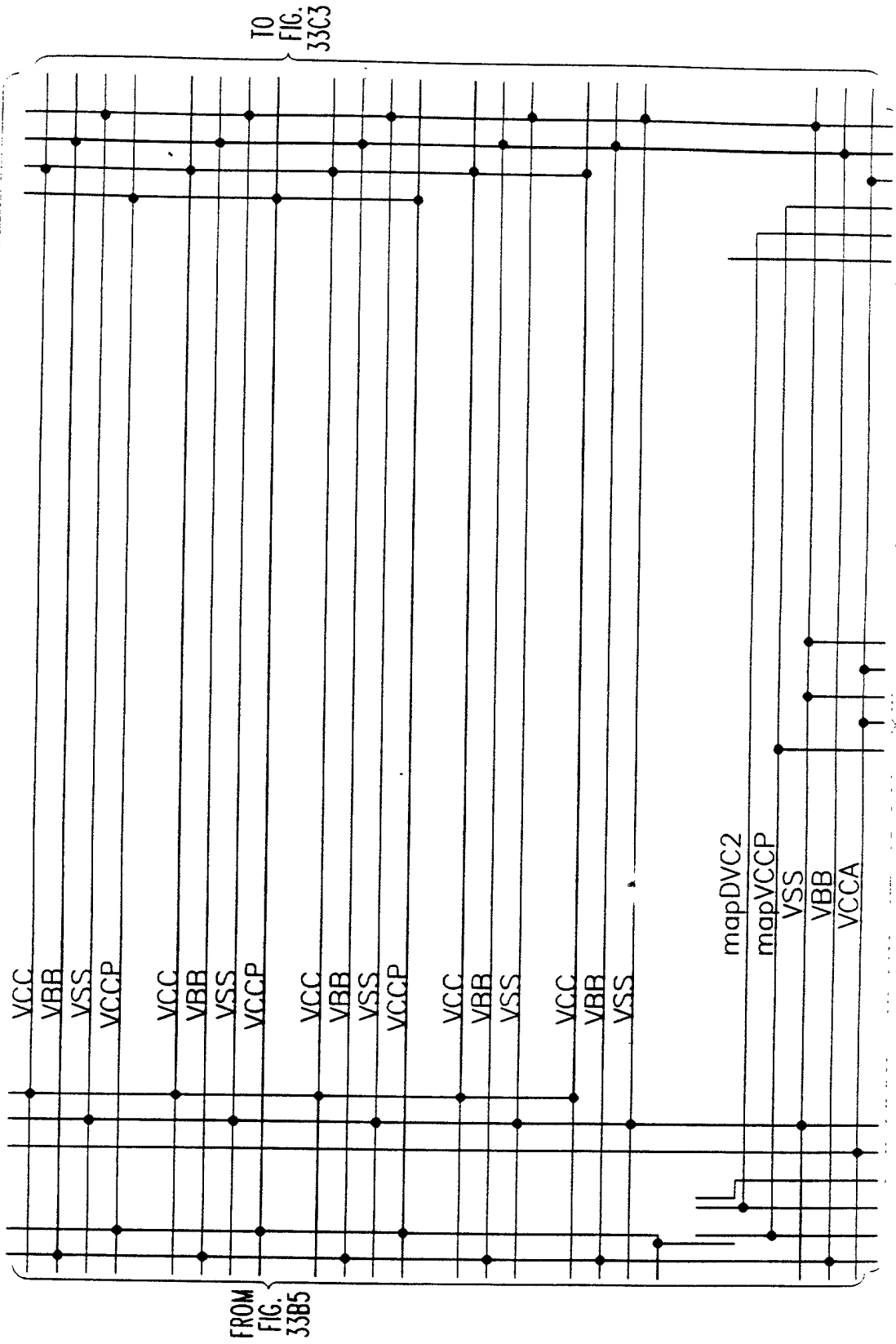
TO
FIG.
33B6

114/367

TO FIG. 33B7

FIG. 33B5

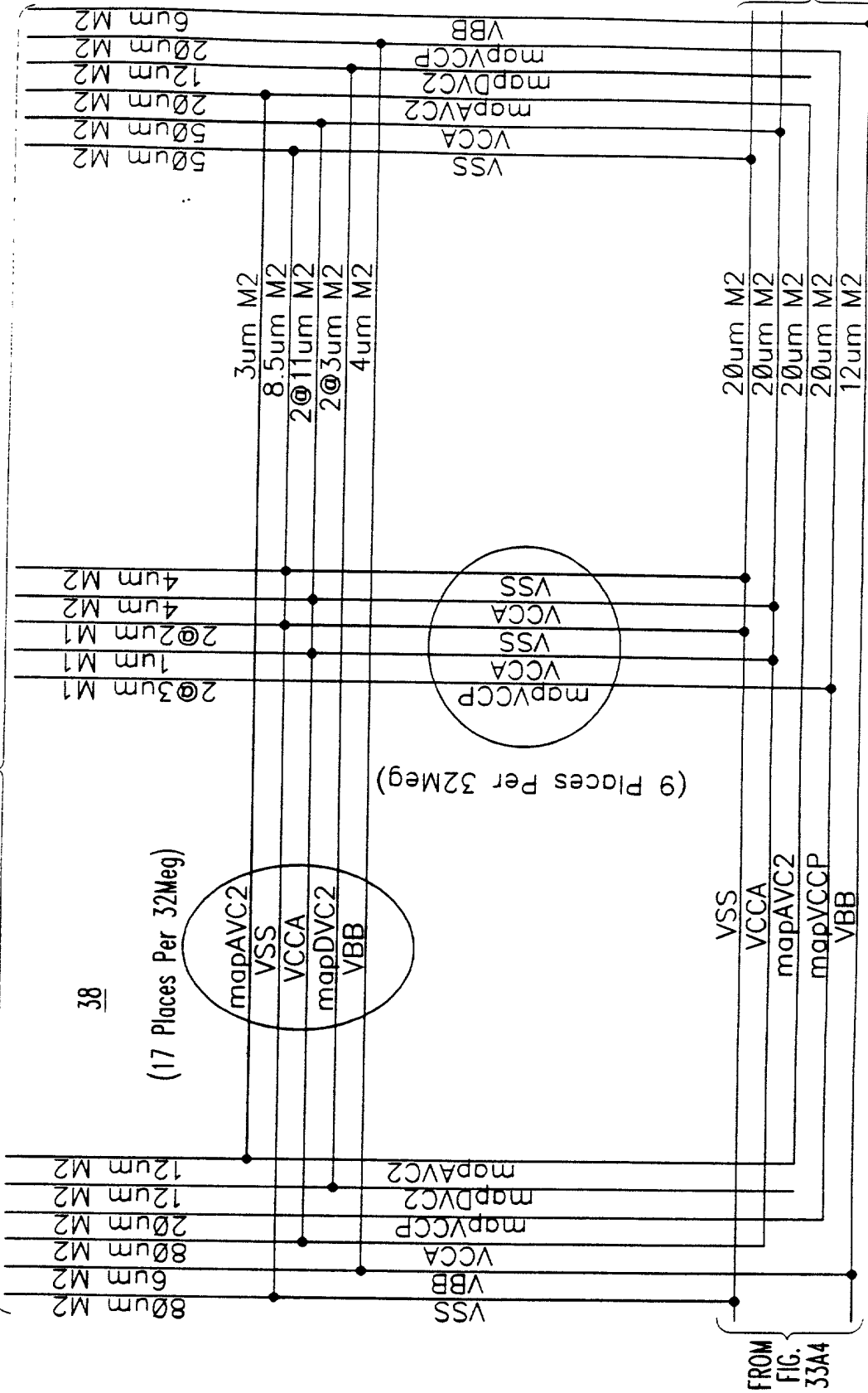
FROM FIG. 33B4



TO FIG. 33B8

FIG. 33B6

FROM FIG. 33B5



116. 367

FIG. 33B8

FIG. 33B7

FROM FIG. 33B6

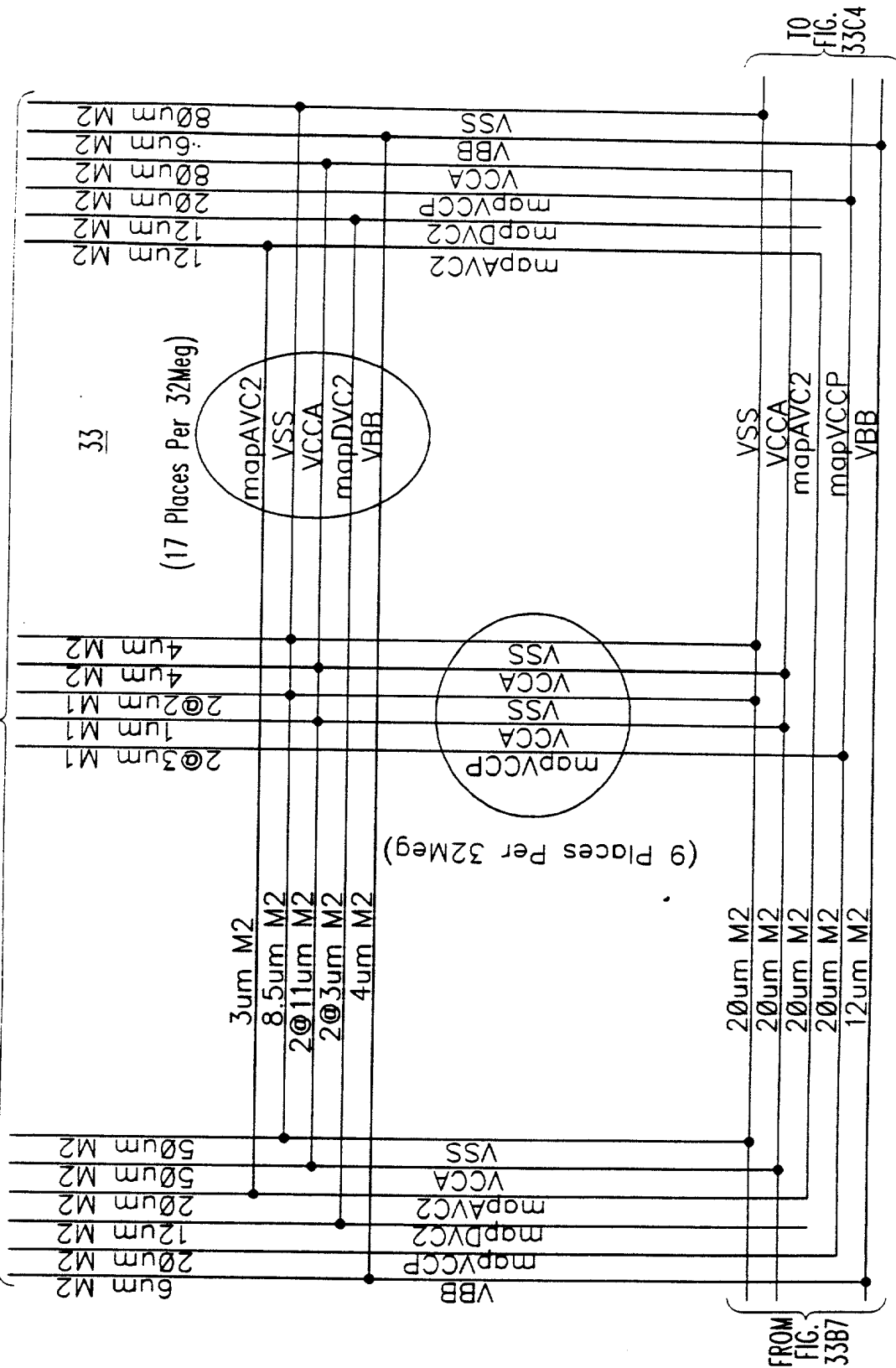
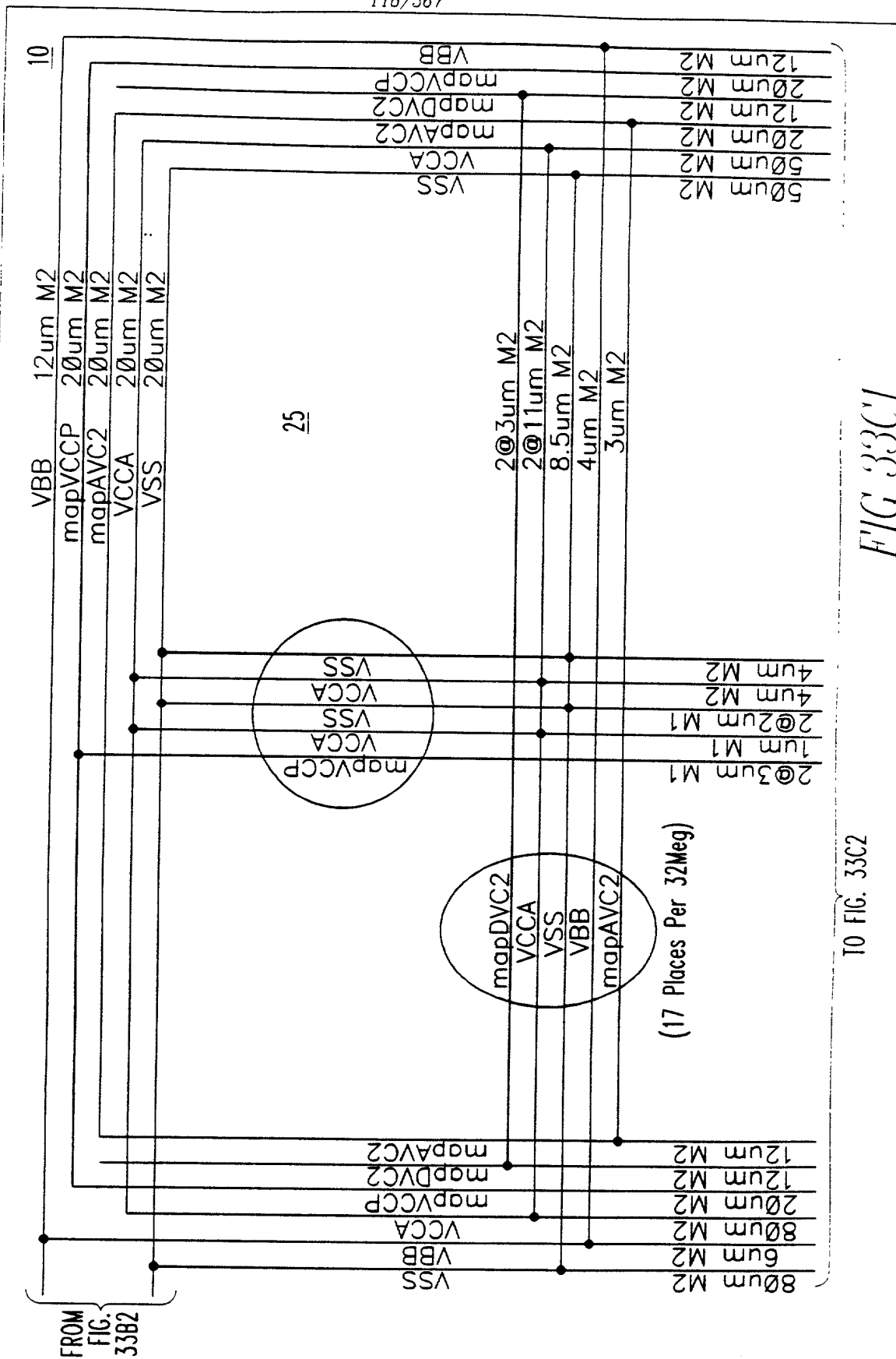
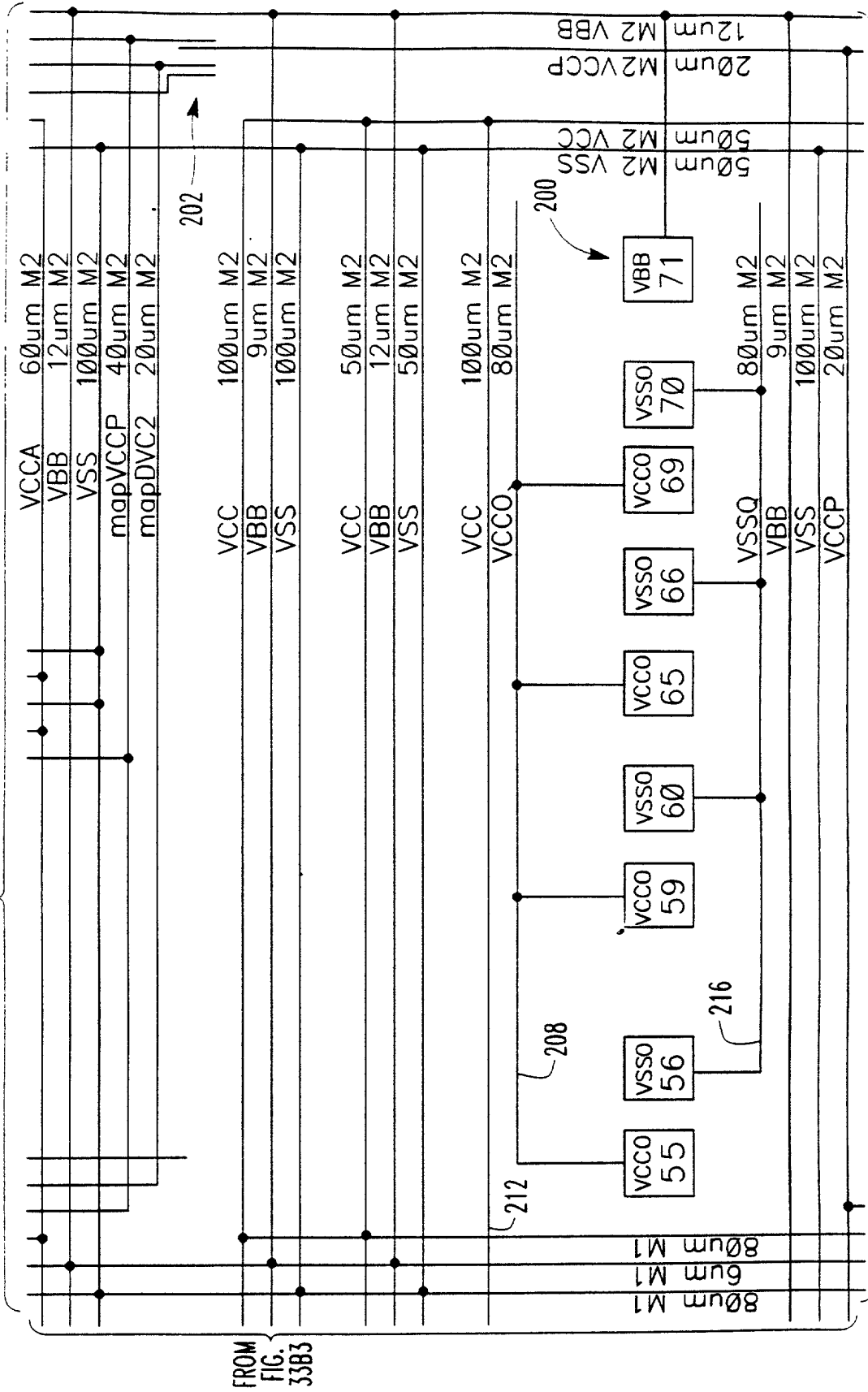


FIG. 33B8



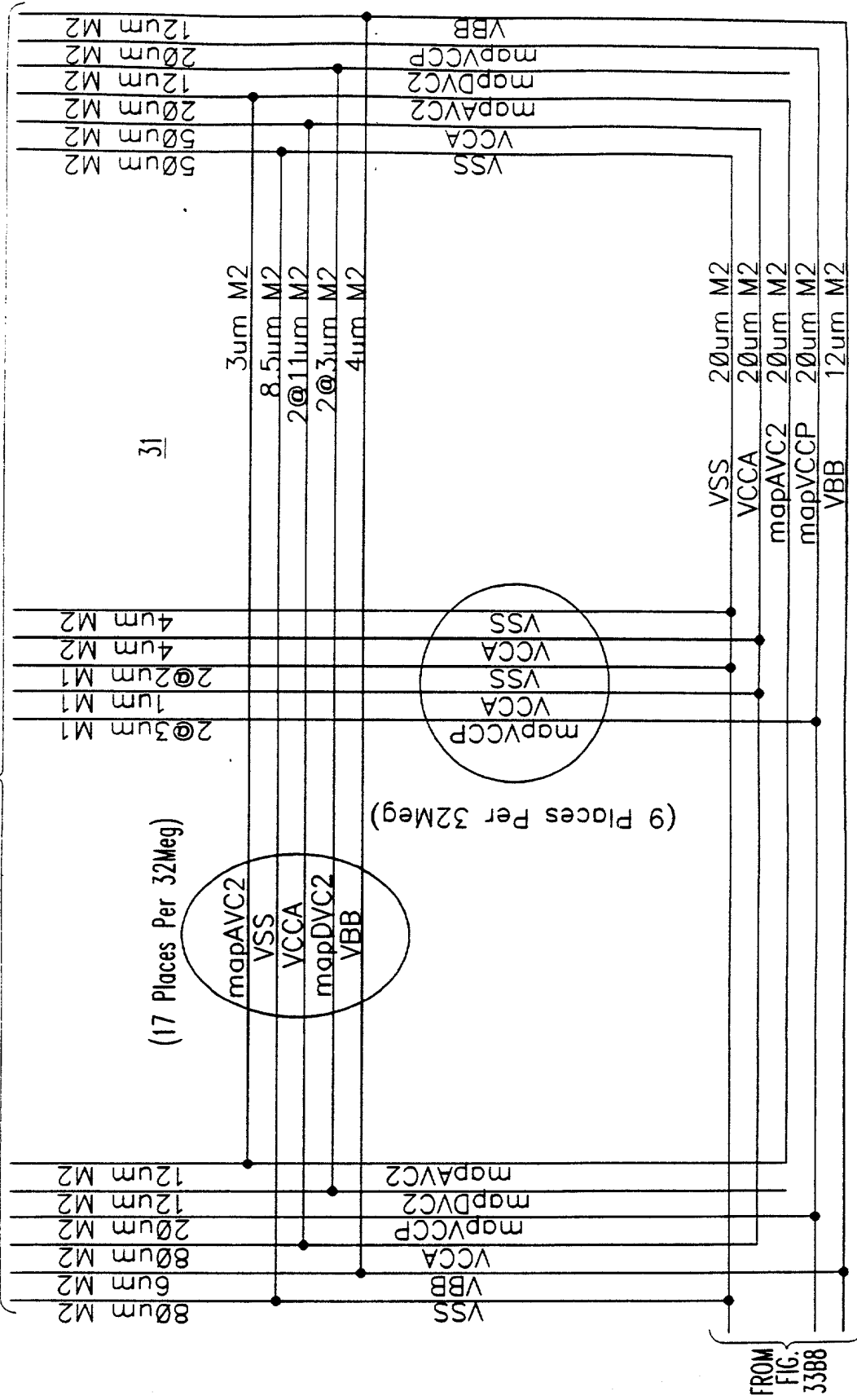
FROM FIG. 33C1



FROM
FIG. 33B6



1763

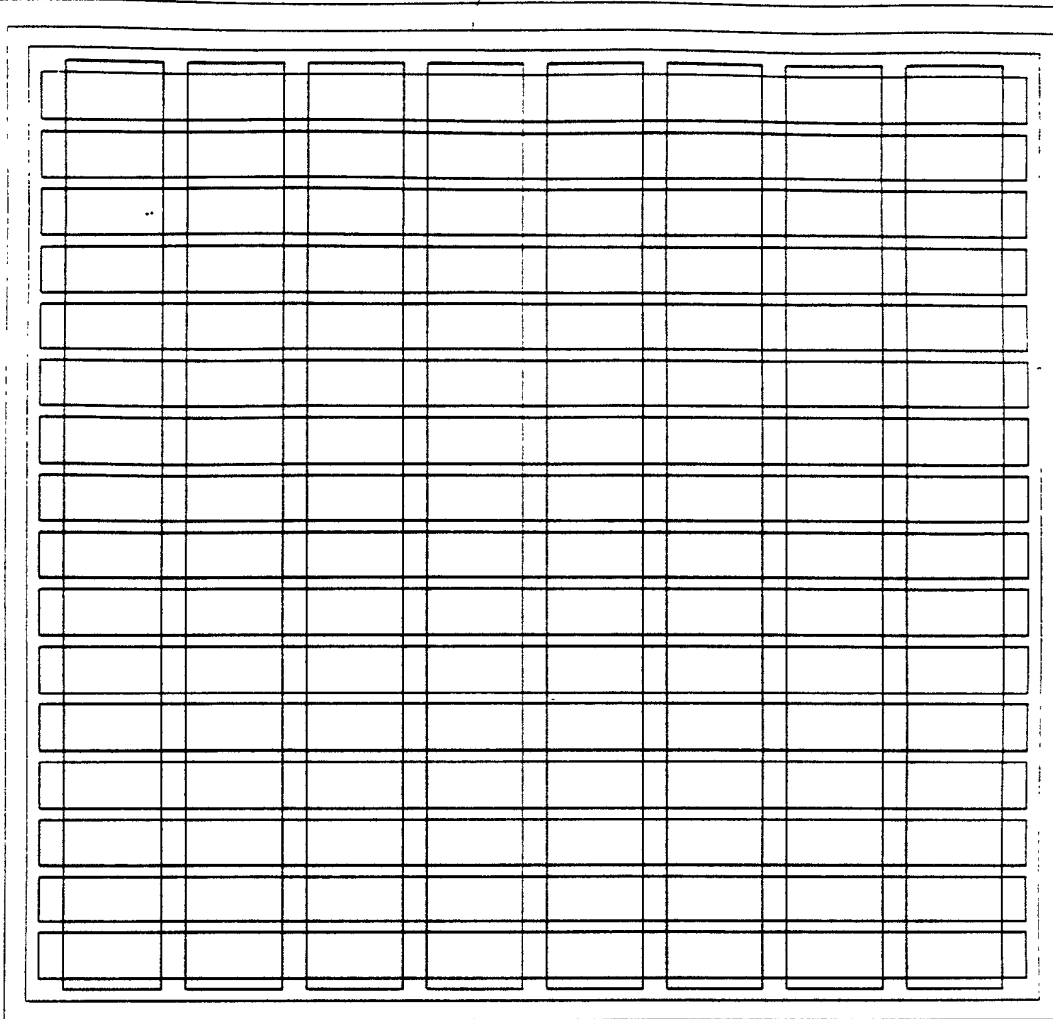


1833

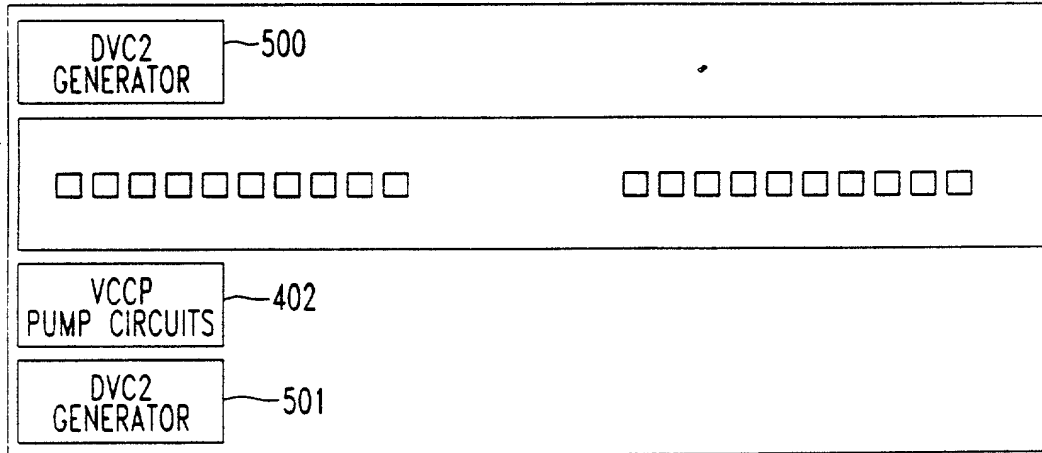
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10

45



200



TO
FIG.
33D3

TO FIG. 33D2

FIG. 33D1

TO FIG. 33D1

47

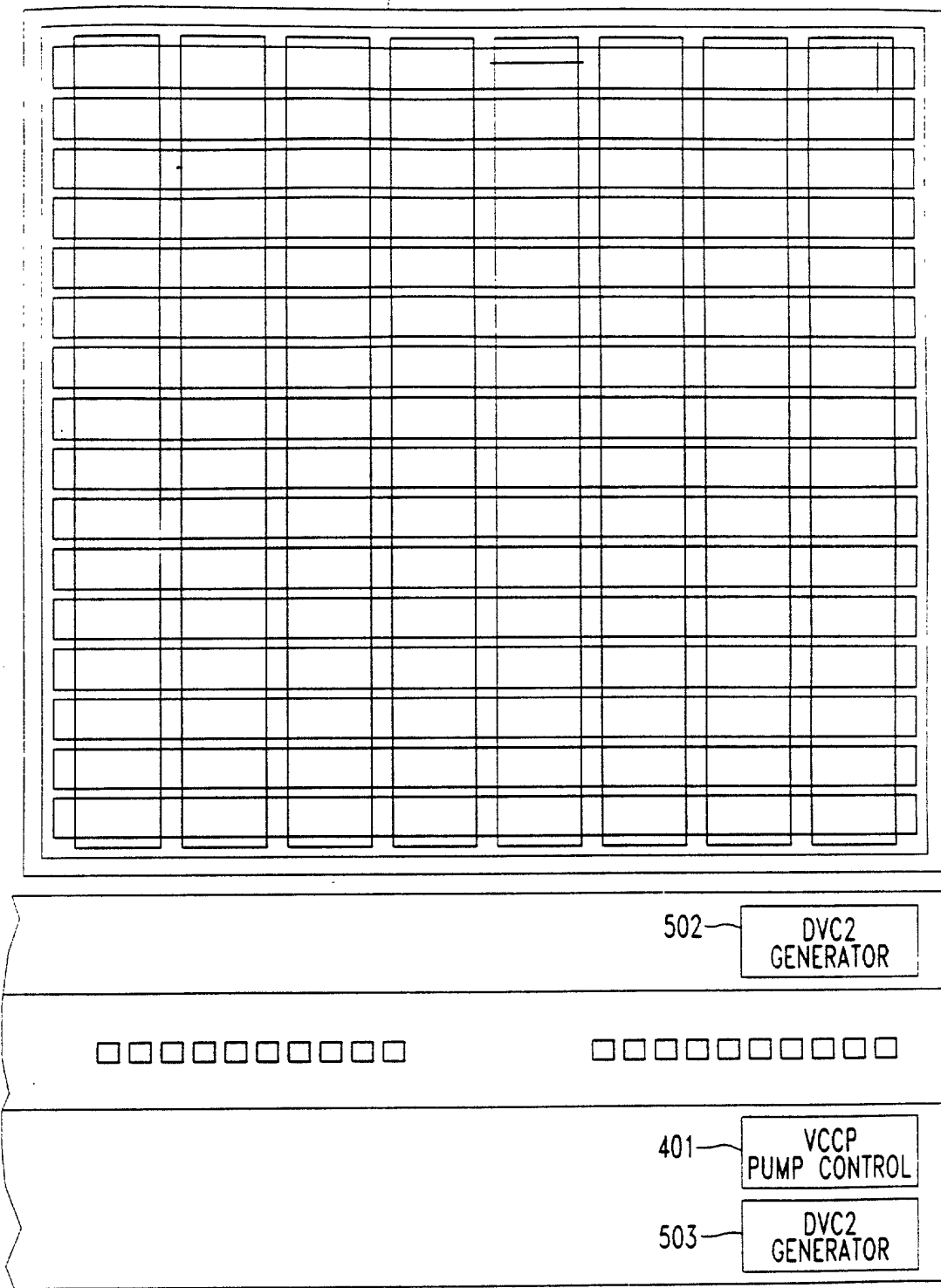
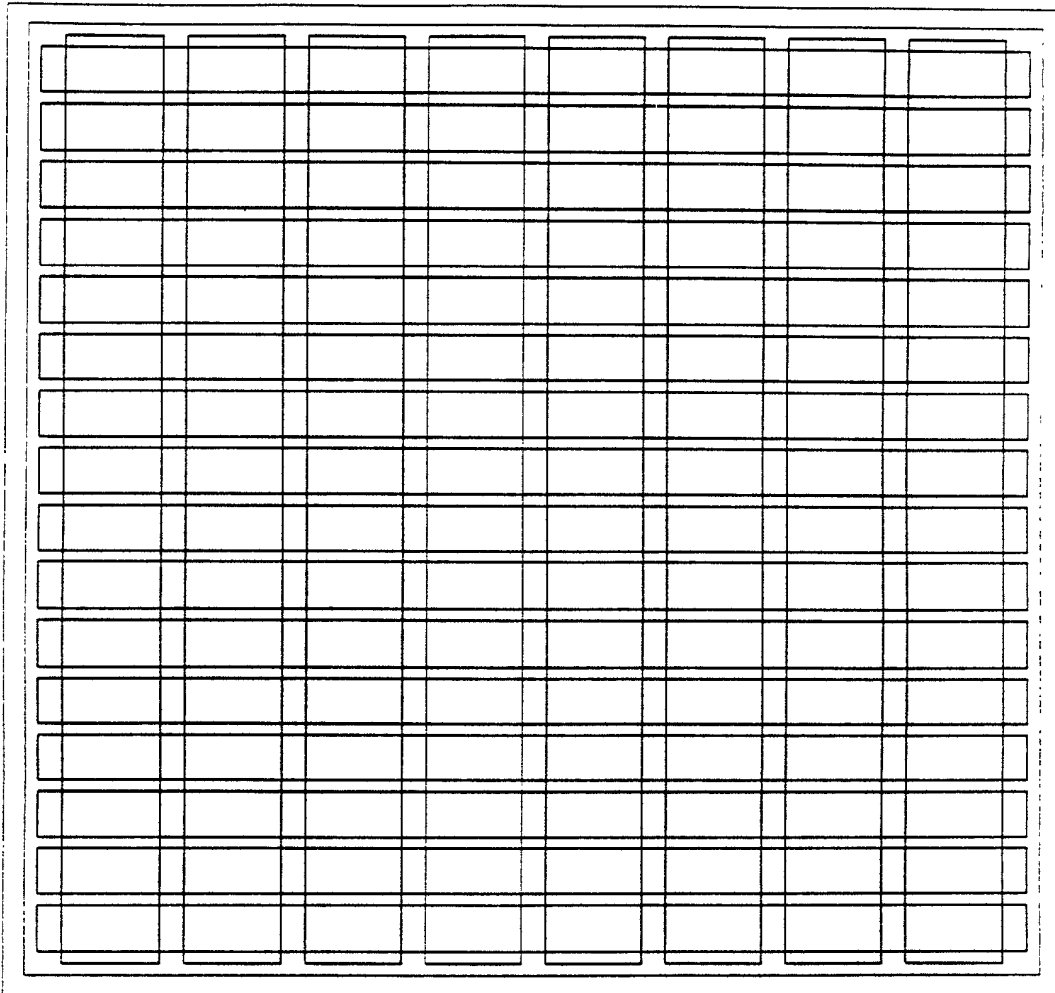


FIG. 33D2

TO
FIG.
33D4

TO
FIG.
33D1

(SEE FIG. 33E1)



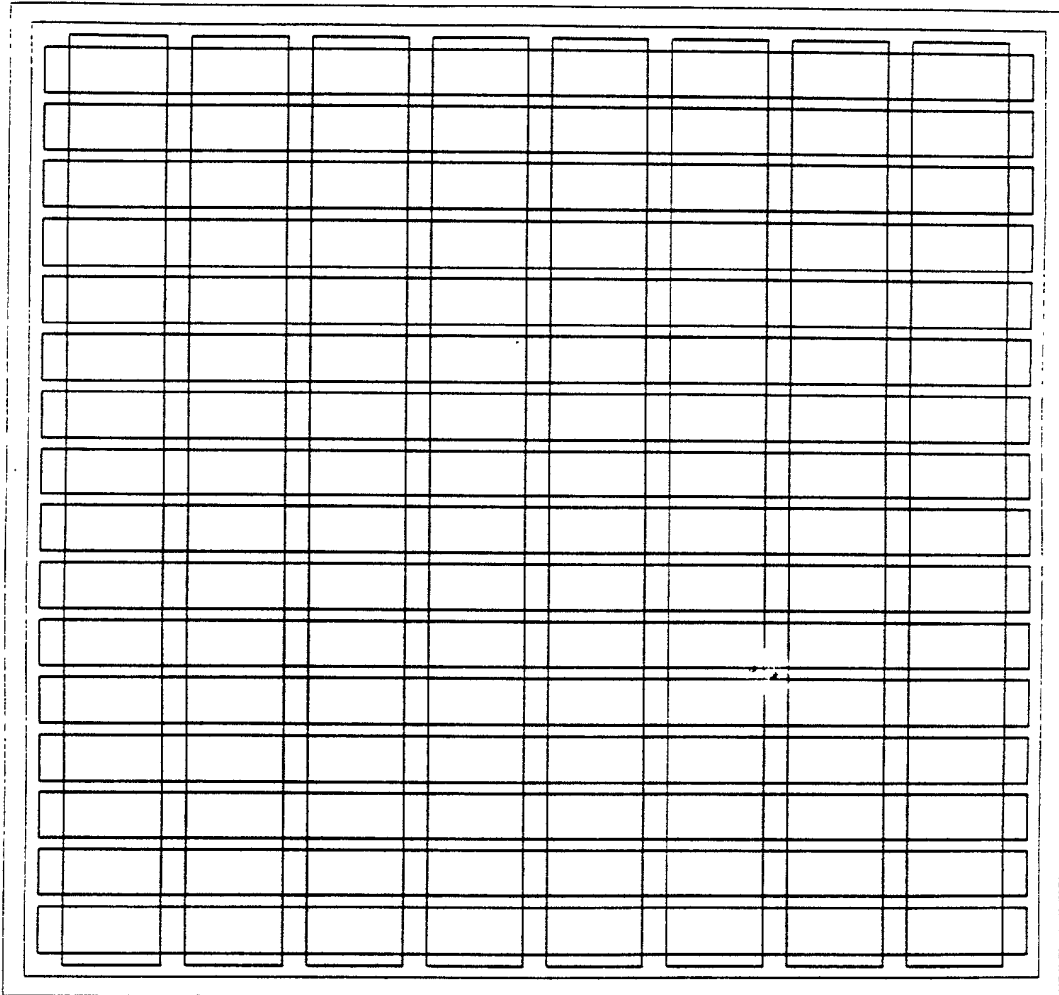
38

TO FIG. 33D4

FIG. 33D3

125, 367

TO
FIG.
33D2



40

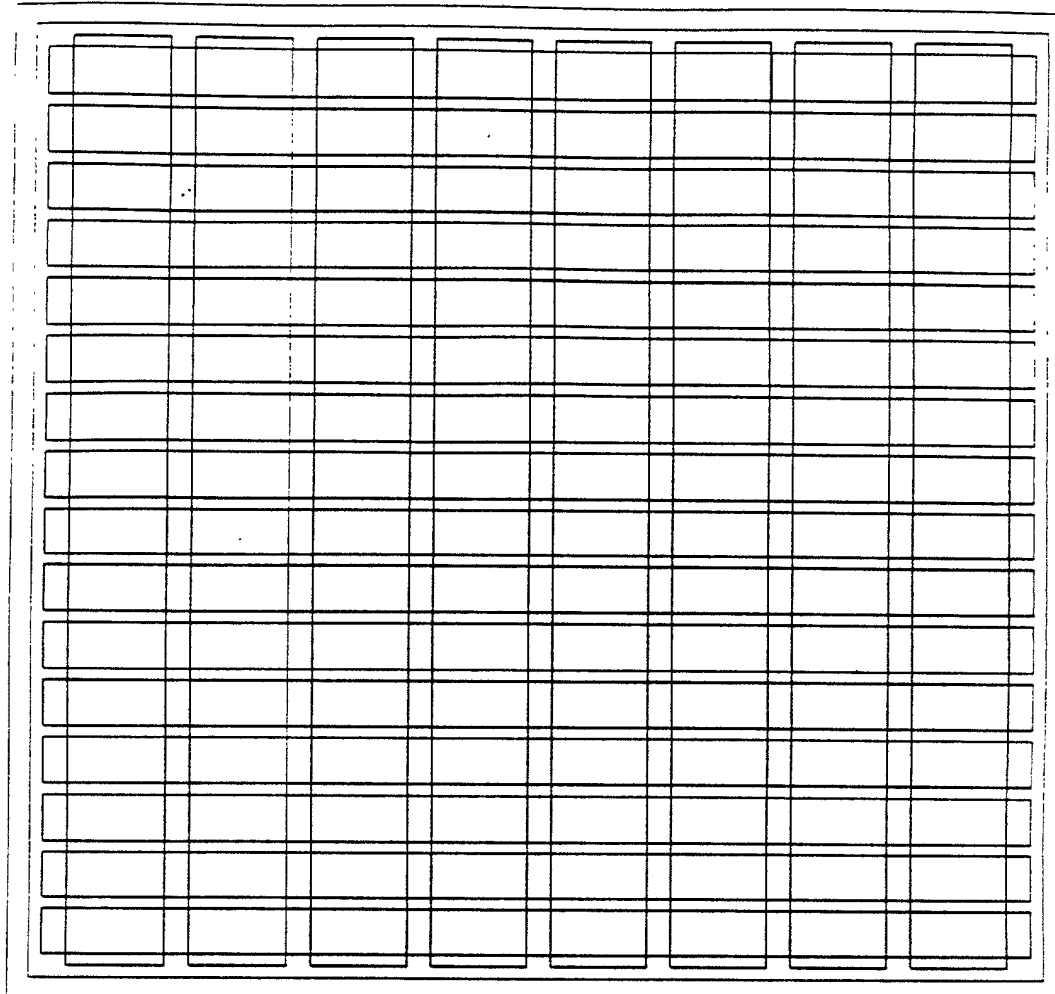
TO FIG. 33D3

FIG. 33D4

(SEE FIG. 33D2)

25

TO FIG. 33E2

DVC2
GENERATOR 504

□ □ □ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □ □ □

VCCP
REGULATOR 220DVC2
GENERATOR 505TO
FIG. 33E3

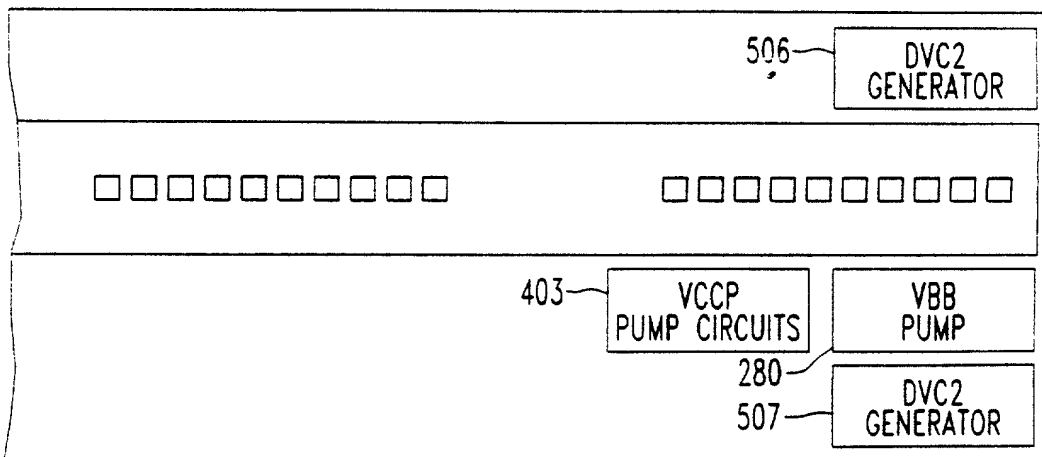
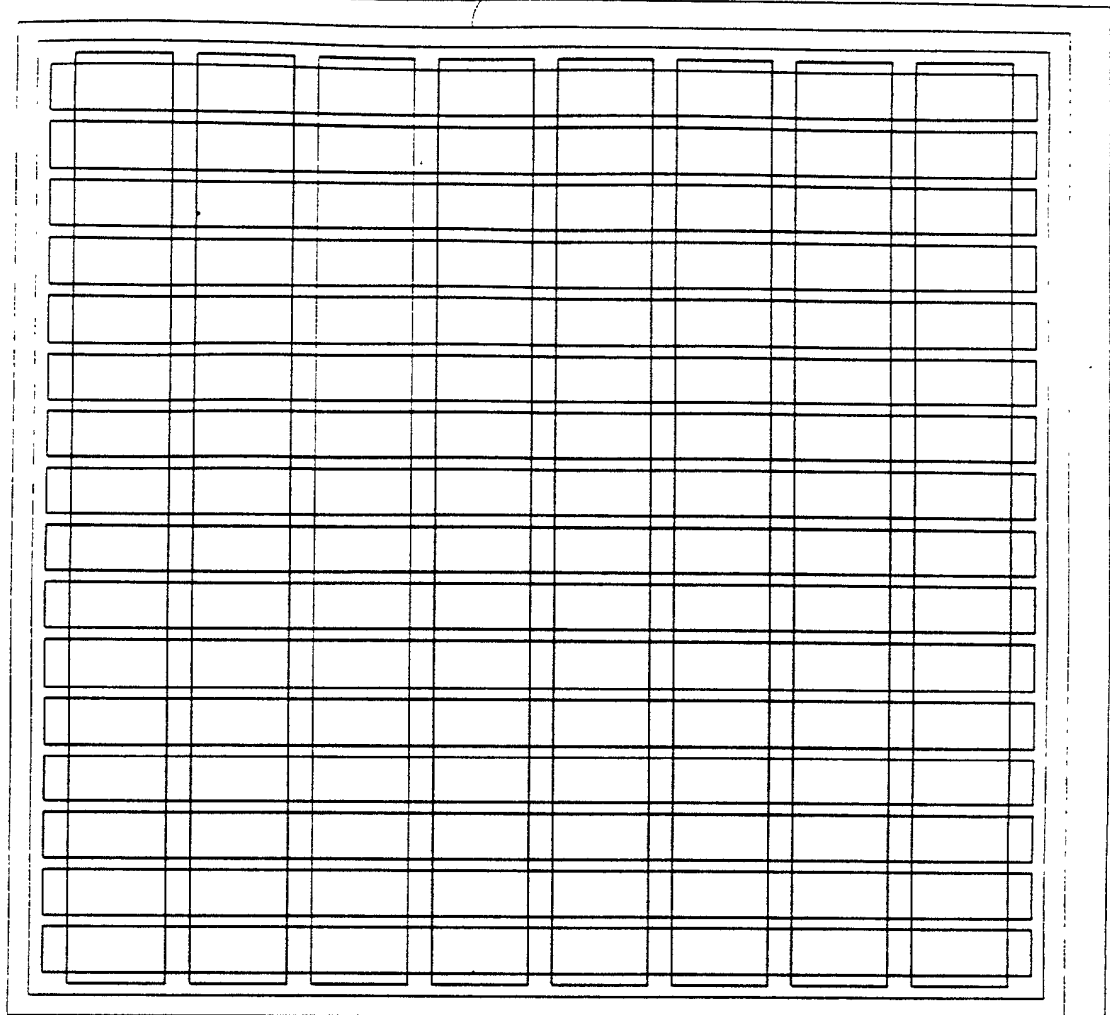
FIG. 33E1

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TO FIG. 33E1

27

10

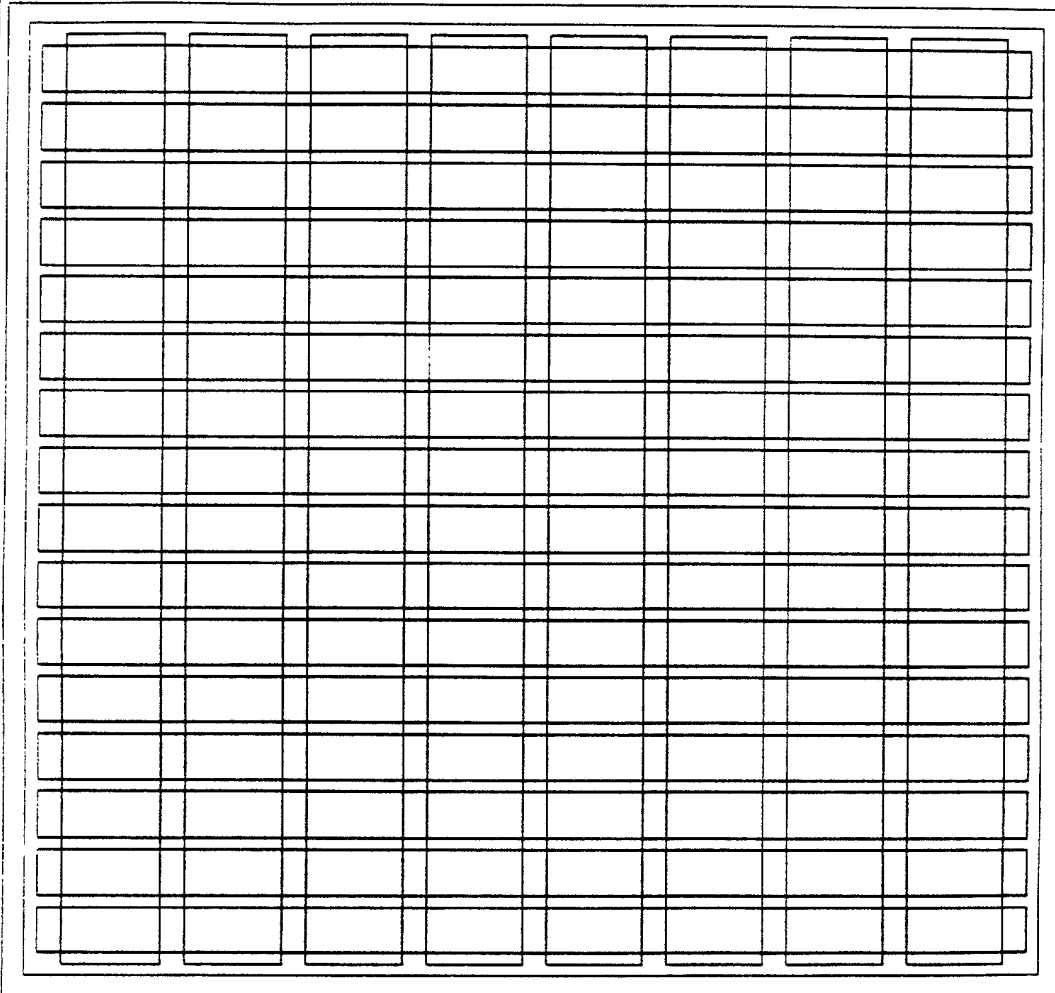


200

FIG. 33E2

TO FIG. 33E4

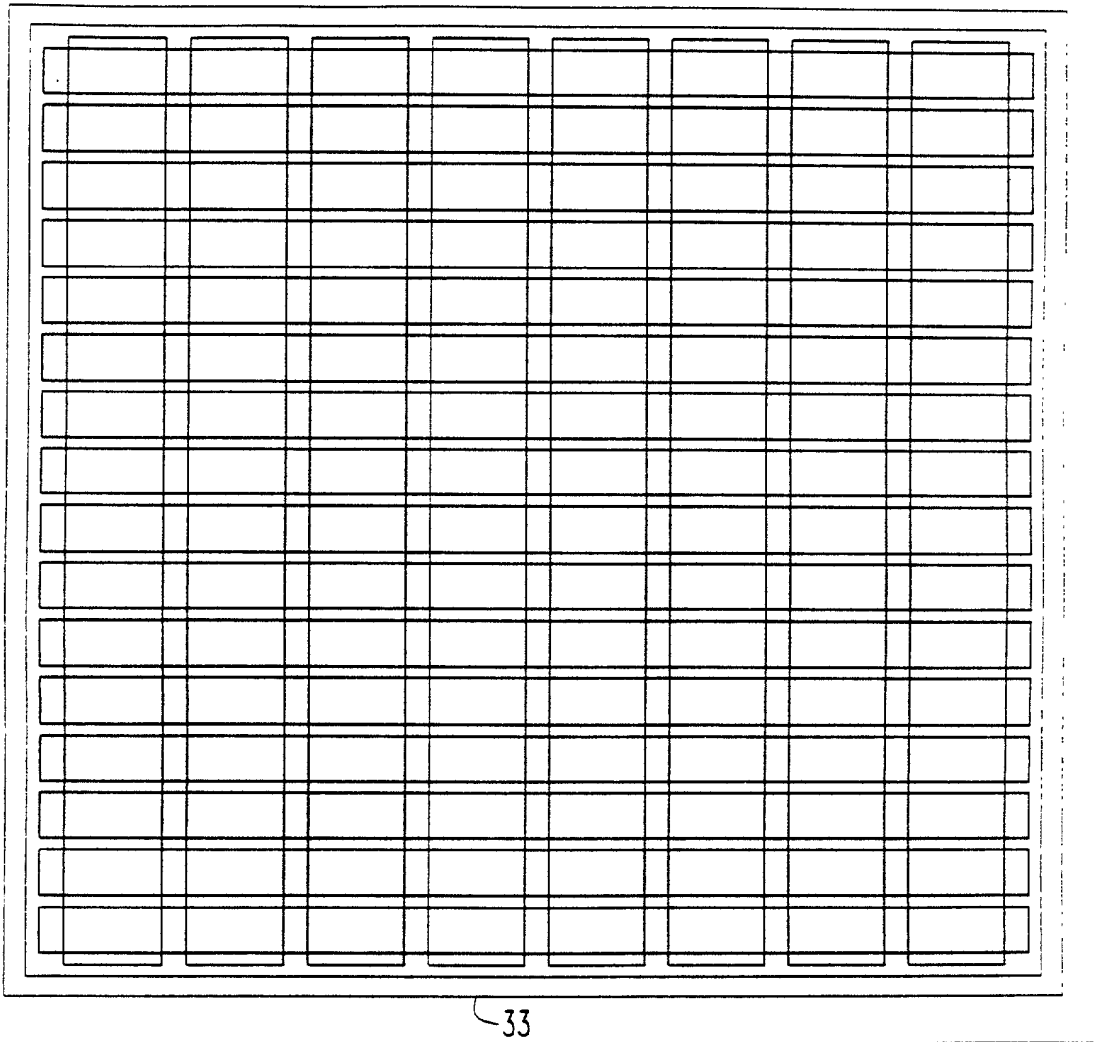
TO
FIG.
33E1



31

TO FIG. 33E4

FIG. 33E3

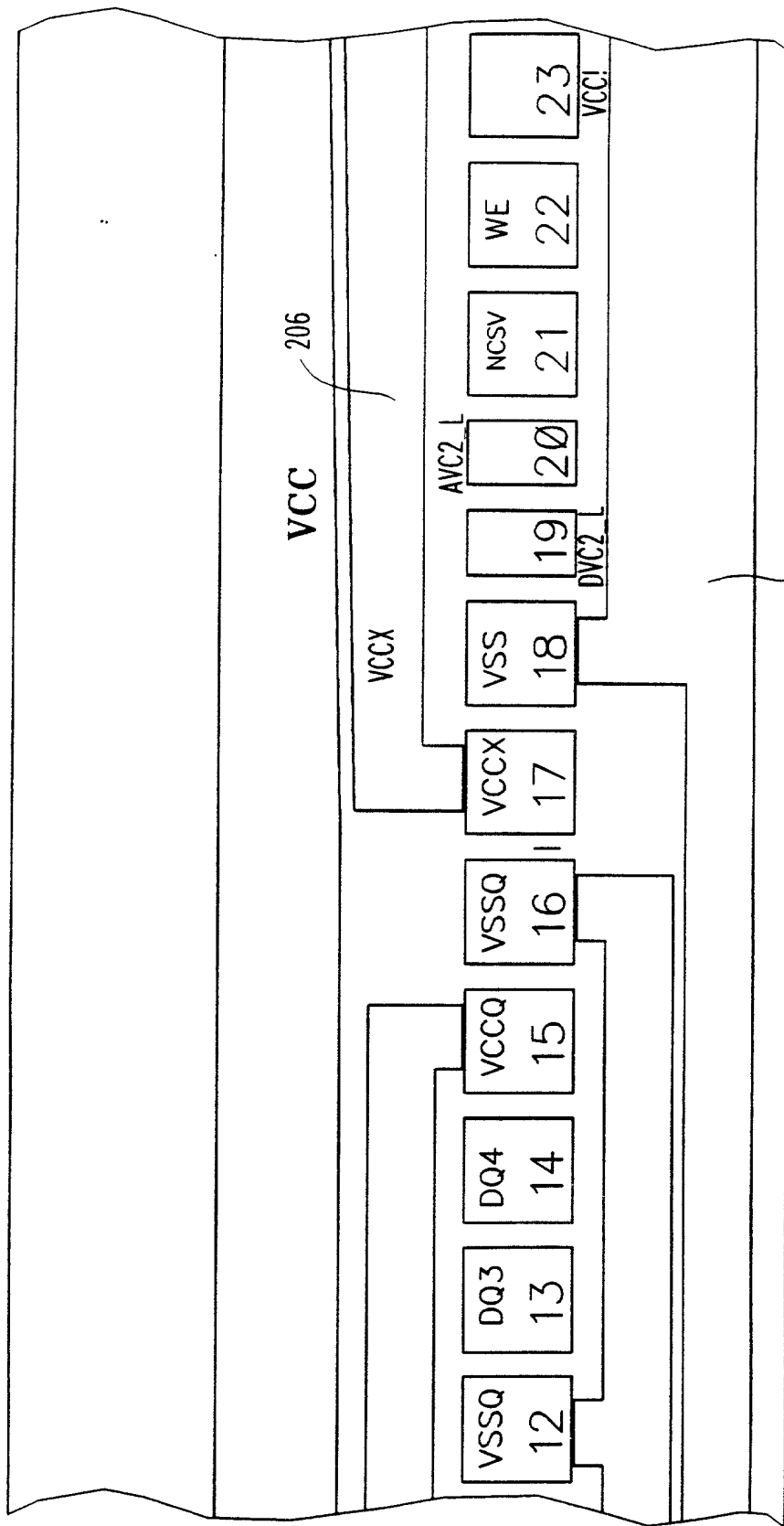


TO
FIG.
33E2

TO FIG. 33E3

FIG. 33E4

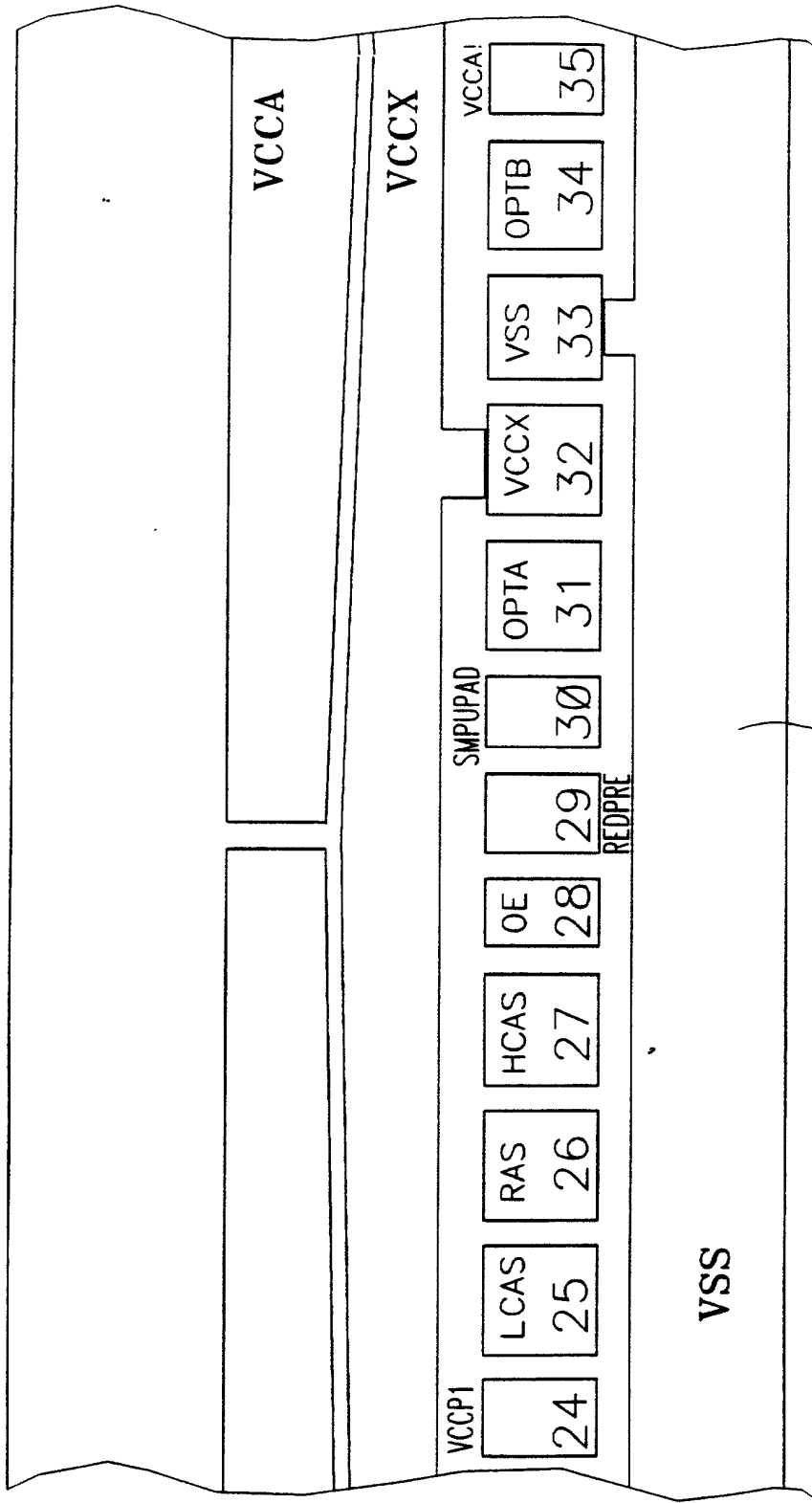
TO FIG. 34A1



TO FIG. 34B1

FIG. 34A2

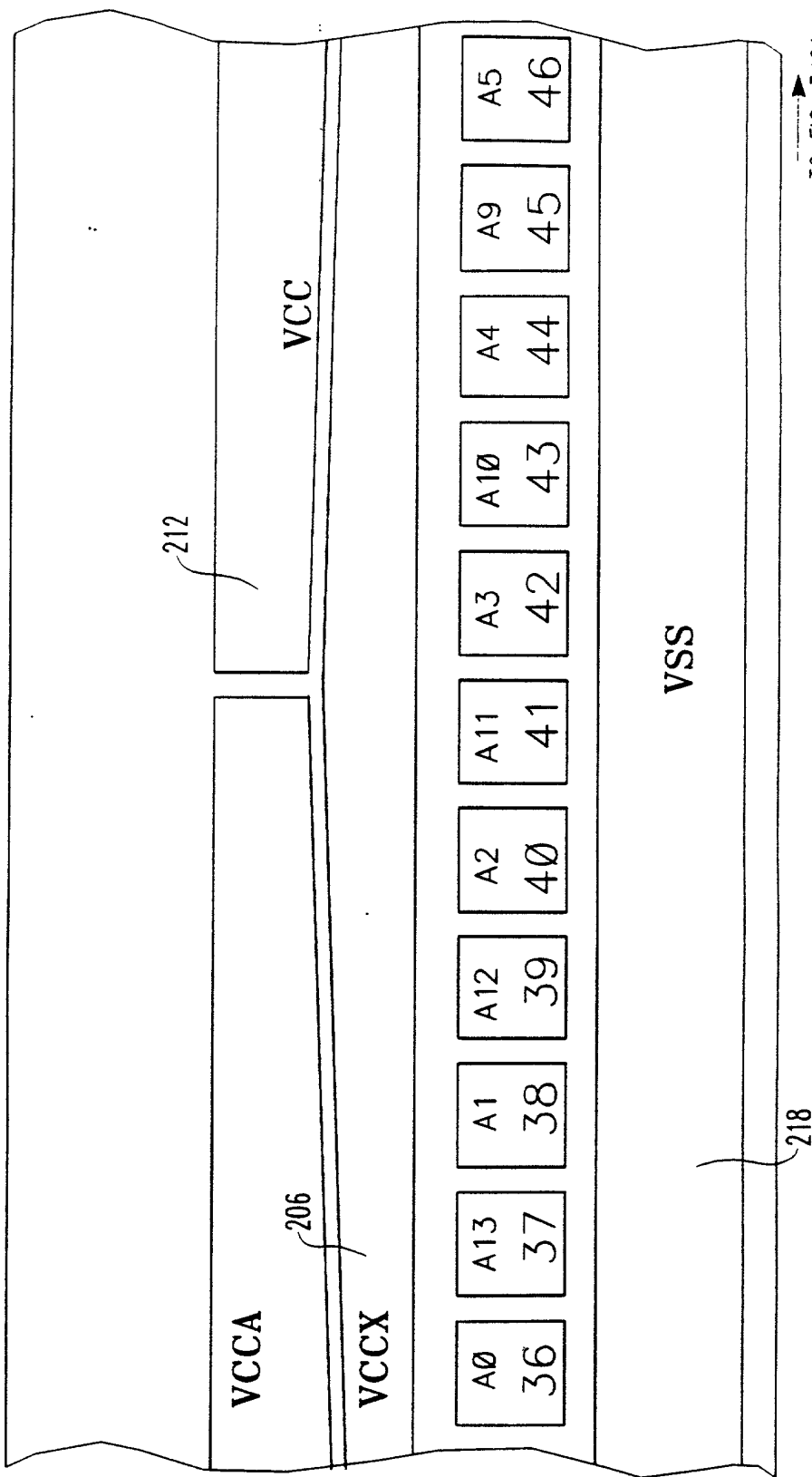
TO FIG. 34A2



TO FIG. 34B2

FIG. 34B1

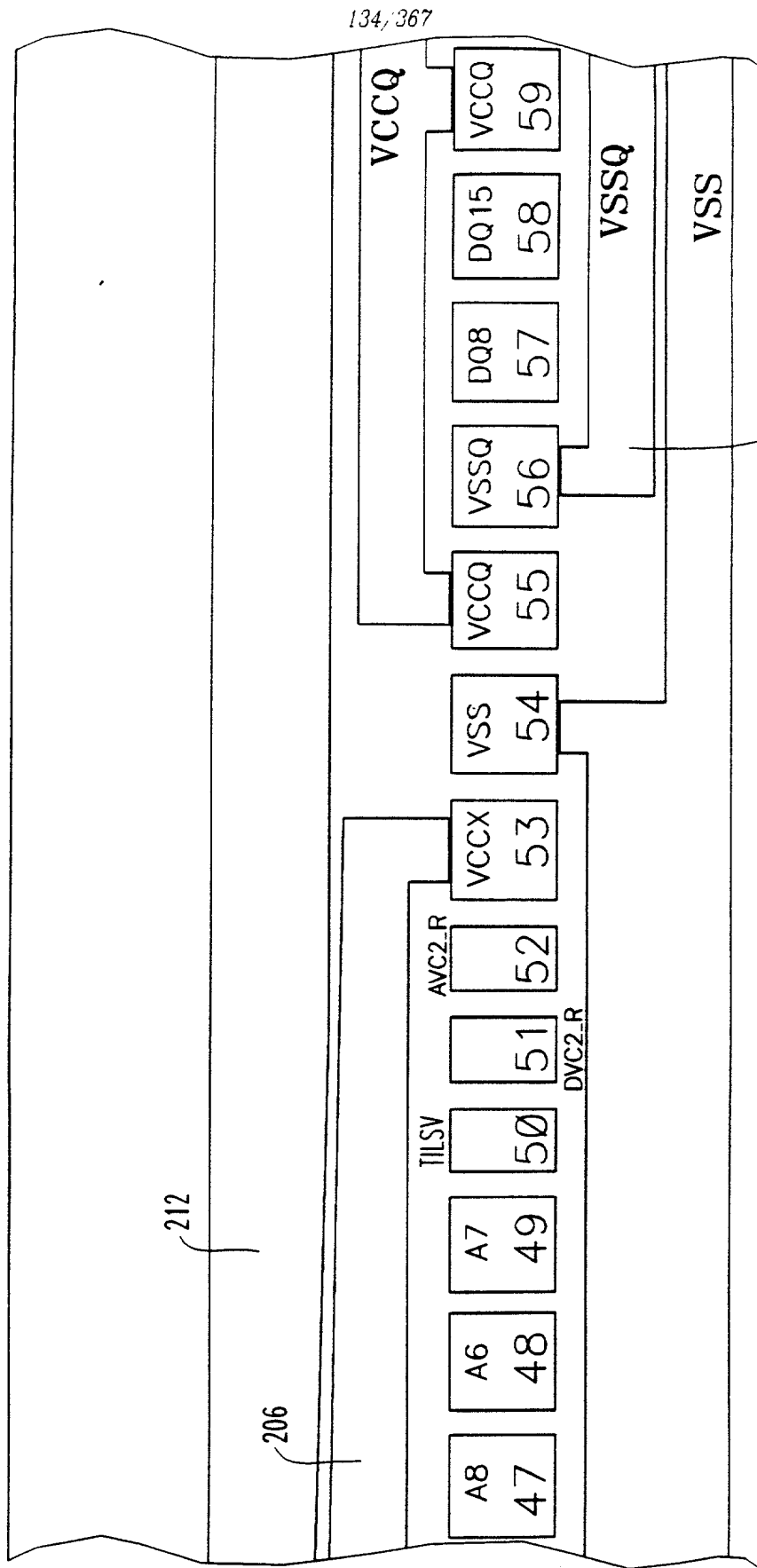
TO FIG. 34B1



TO FIG. 34C1

FIG. 34B2

TO FIG. 34B2



134, 367

TO FIG. 34C2

FIG. 34C1

FIG. 34C1

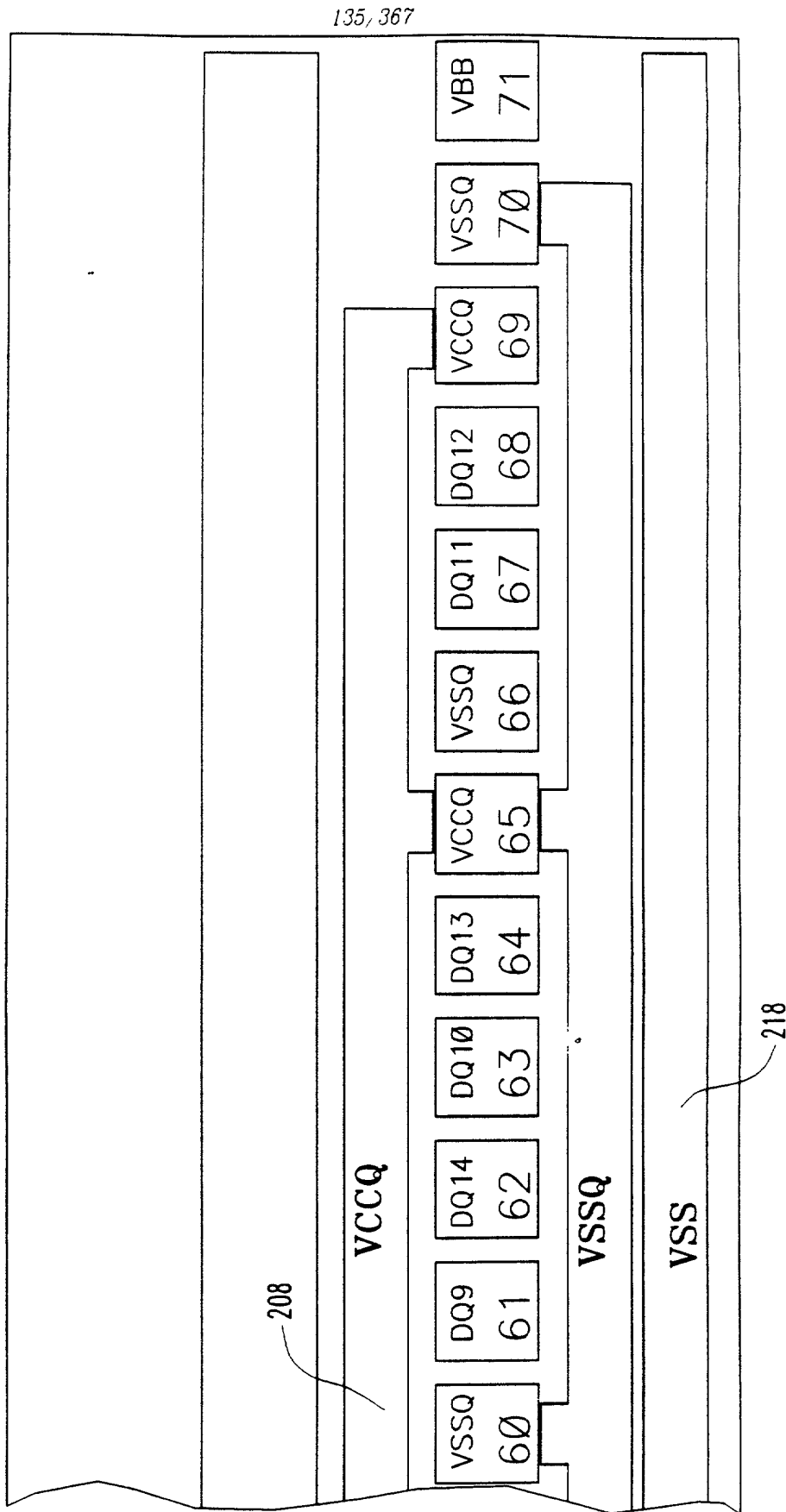


FIG. 34C2

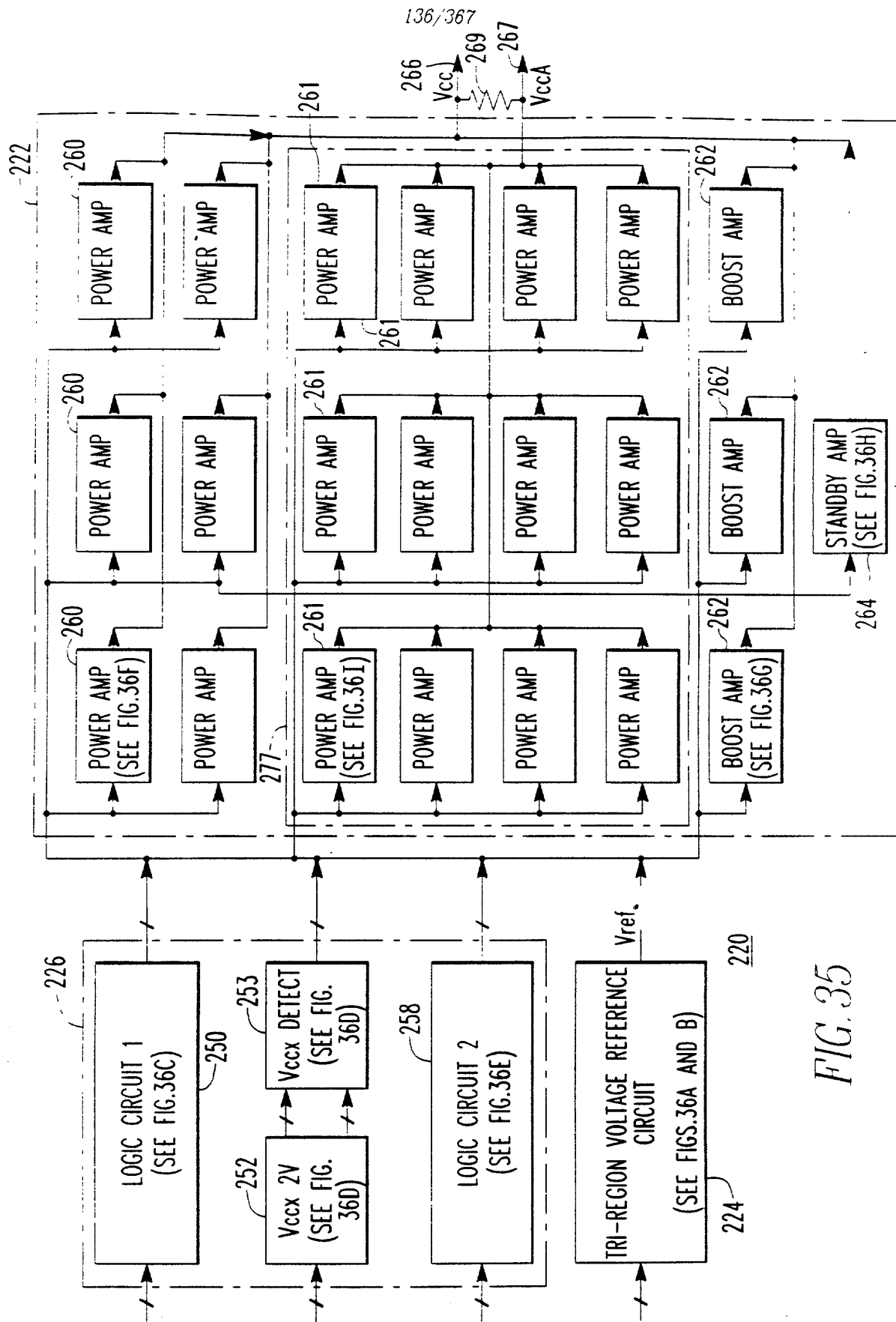


FIG. 35

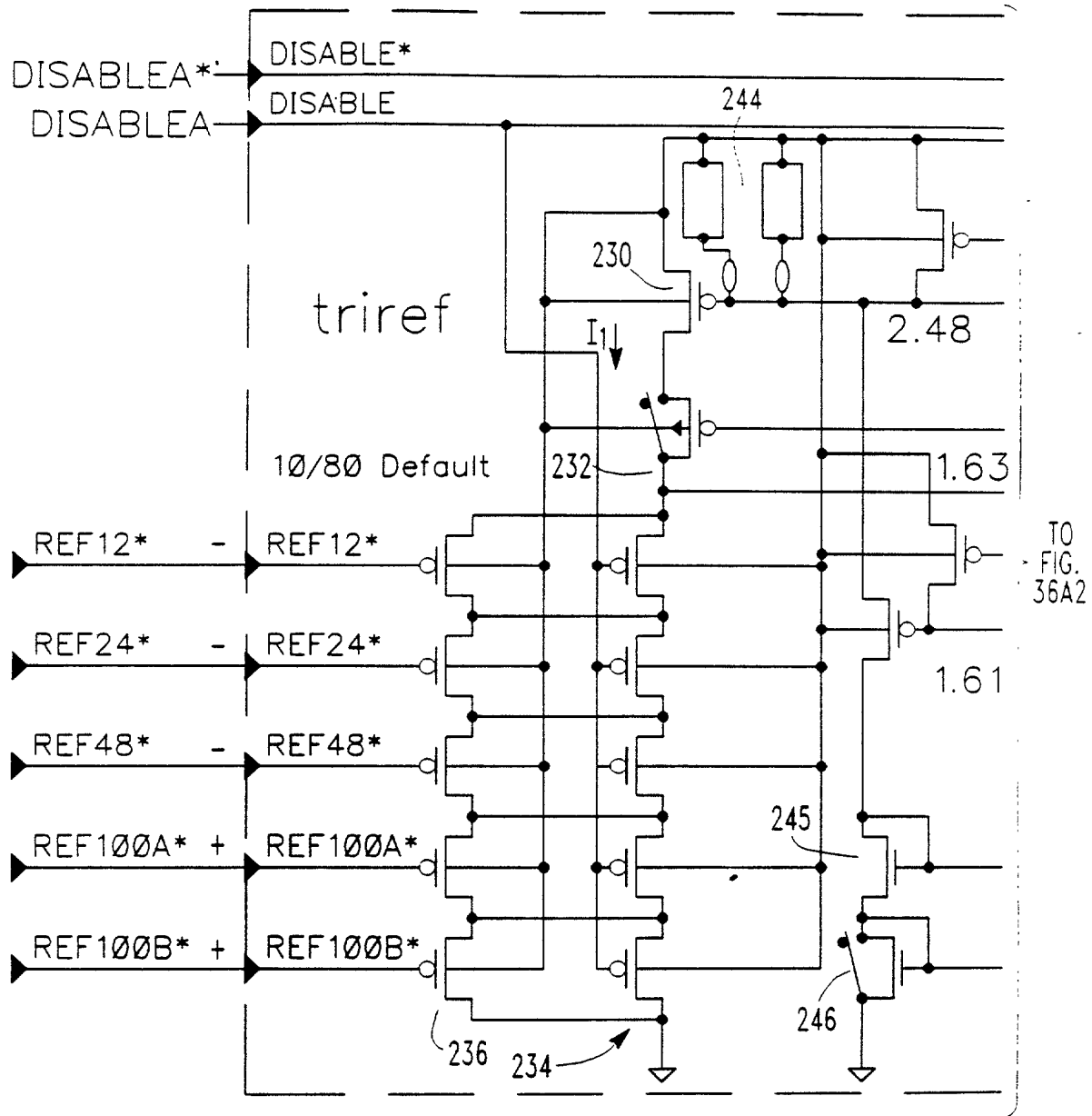


FIG. 36A1

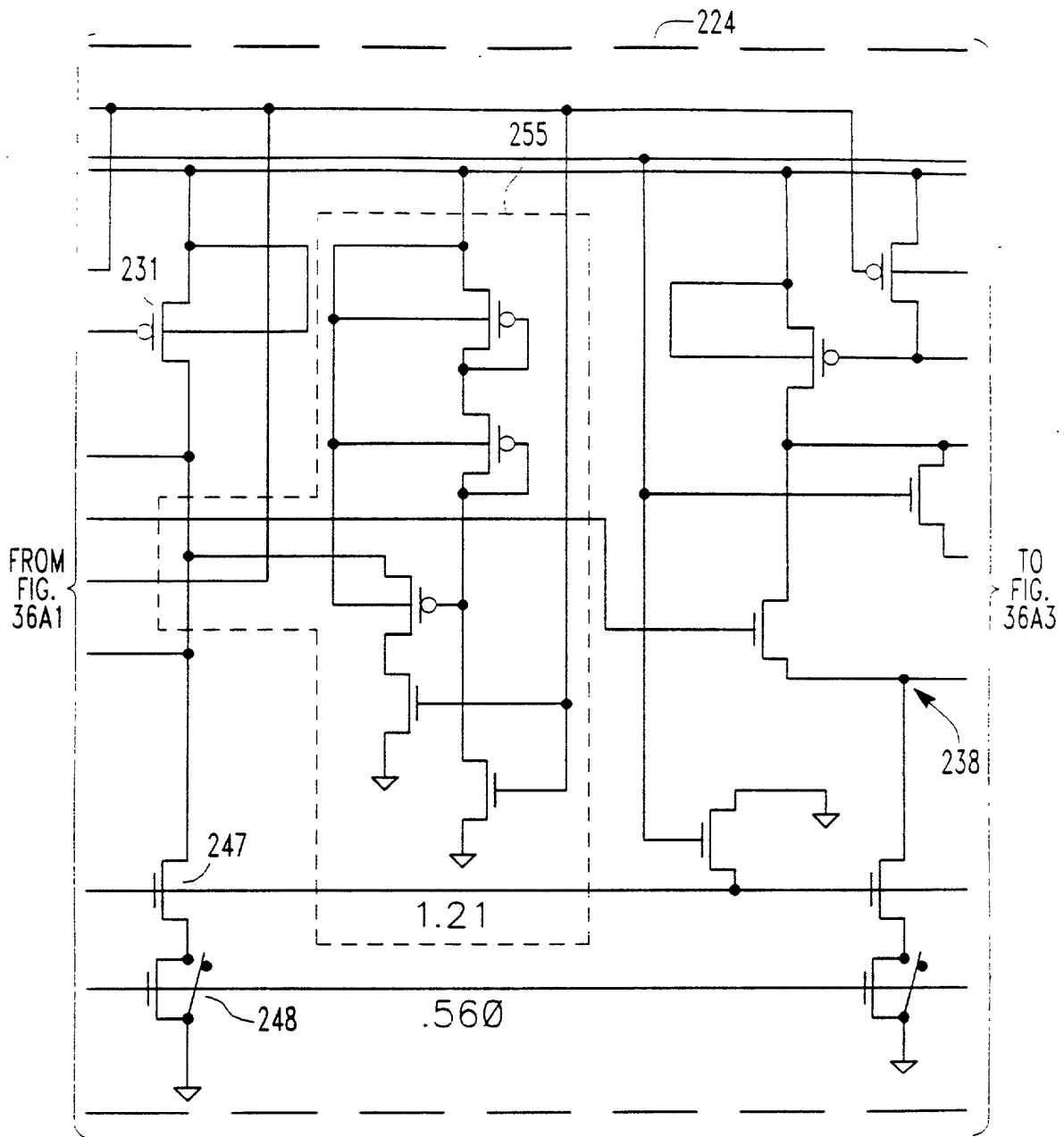


FIG. 36A2

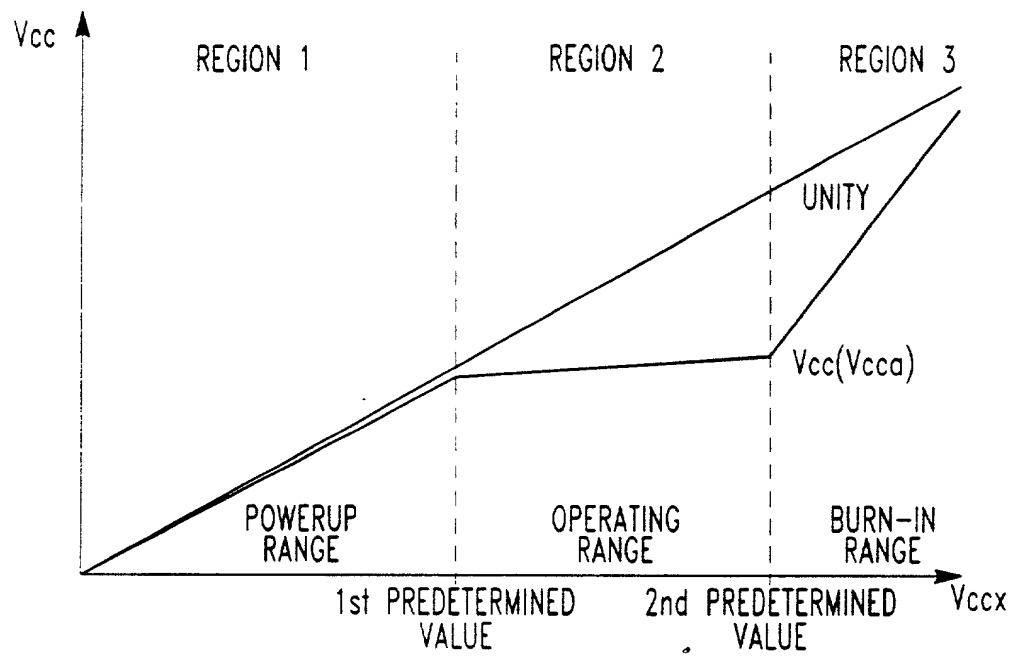


FIG. 36B

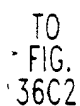


FIG. 36C1

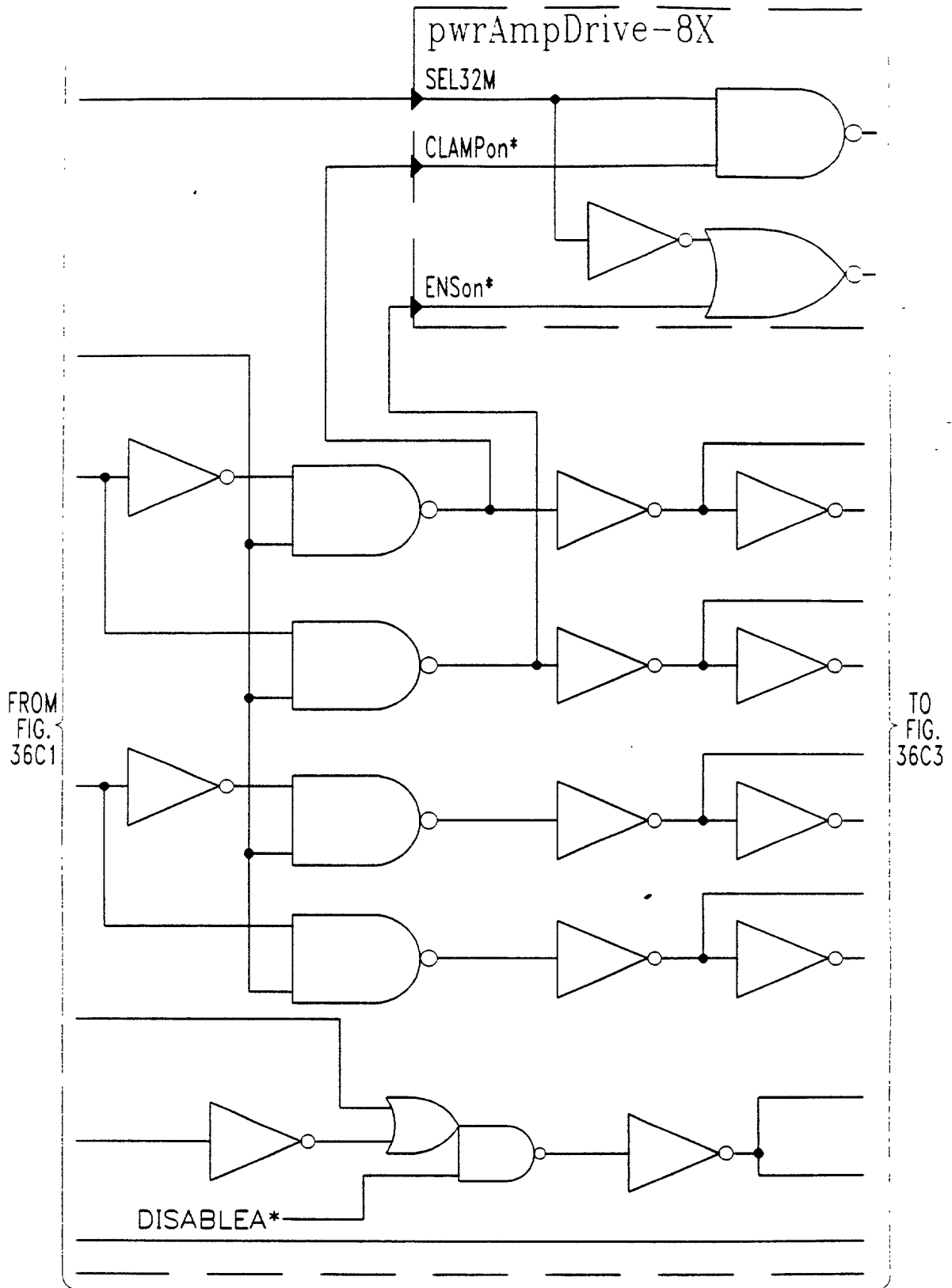


FIG. 36C2

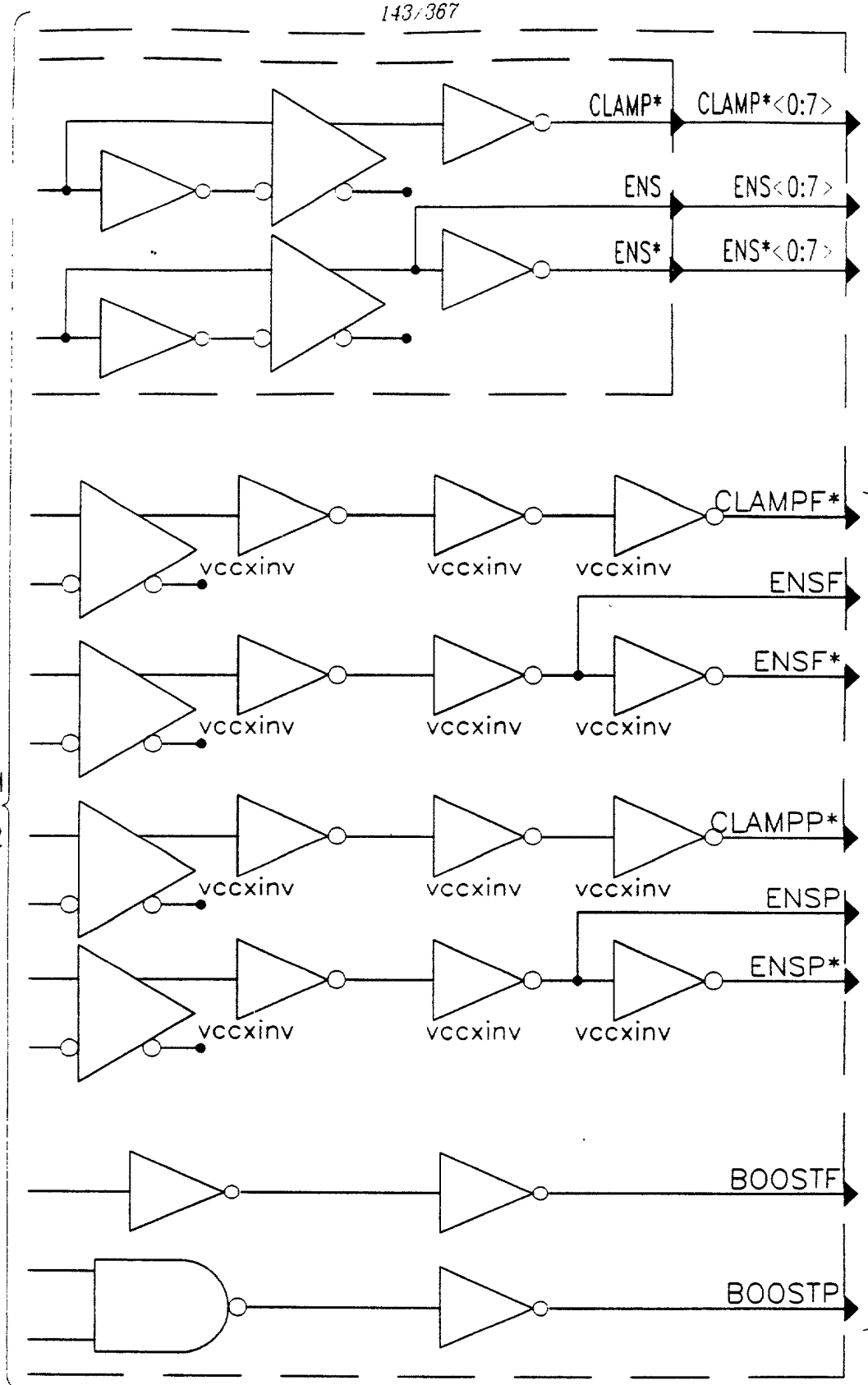
FROM
FIG.
36C2TO
FIG.
36F

FIG. 36C3

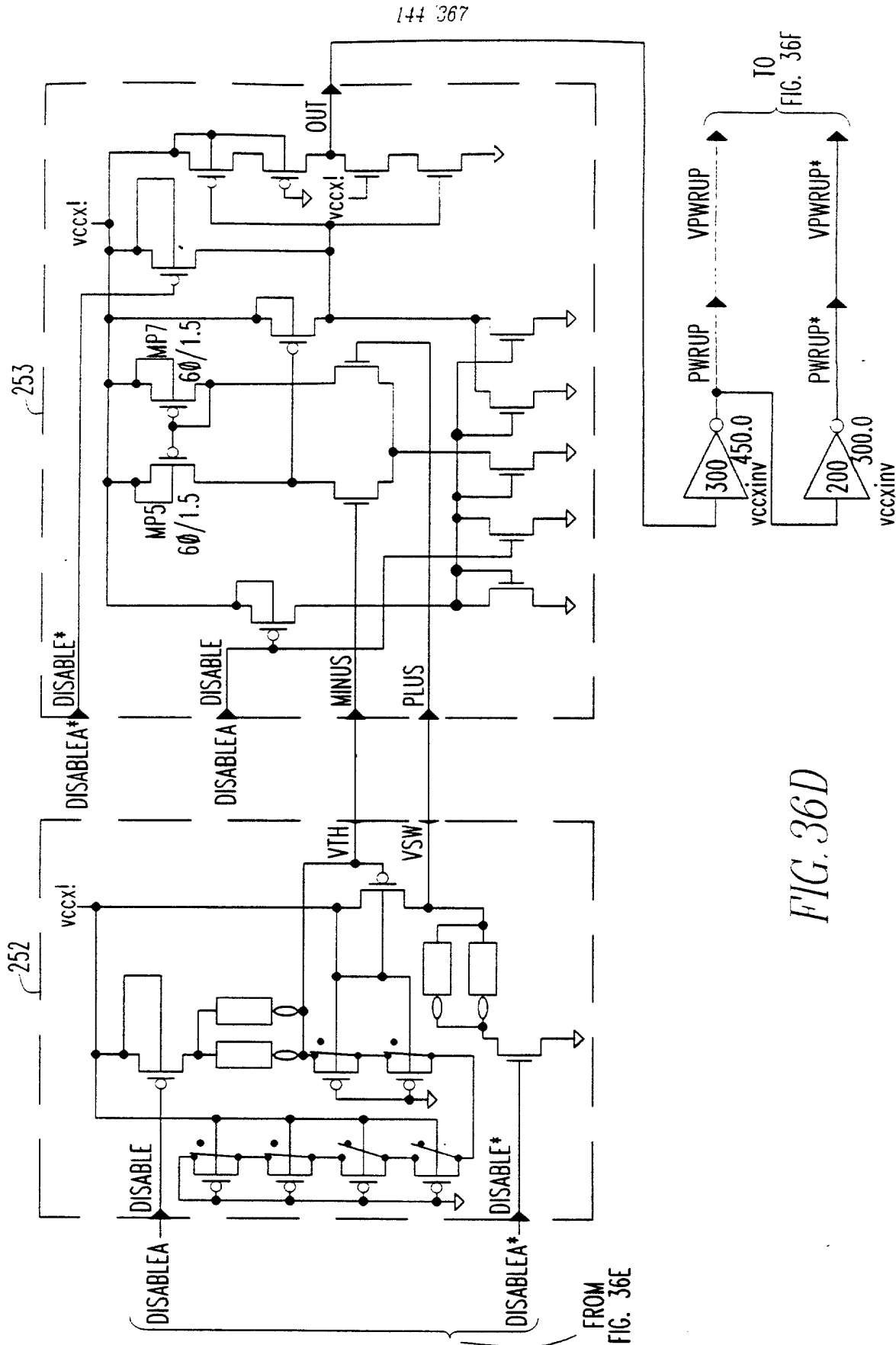


FIG. 36D

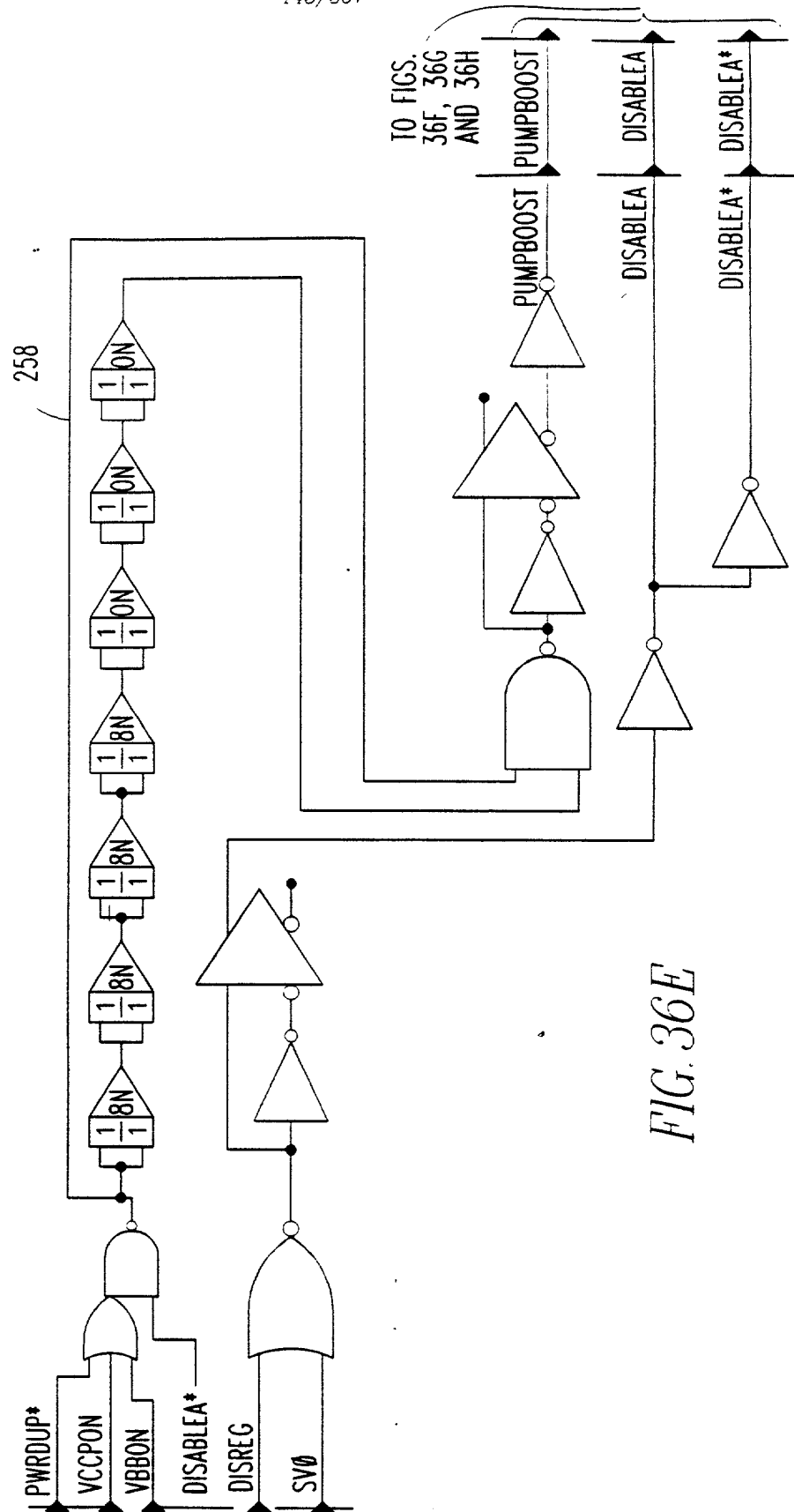
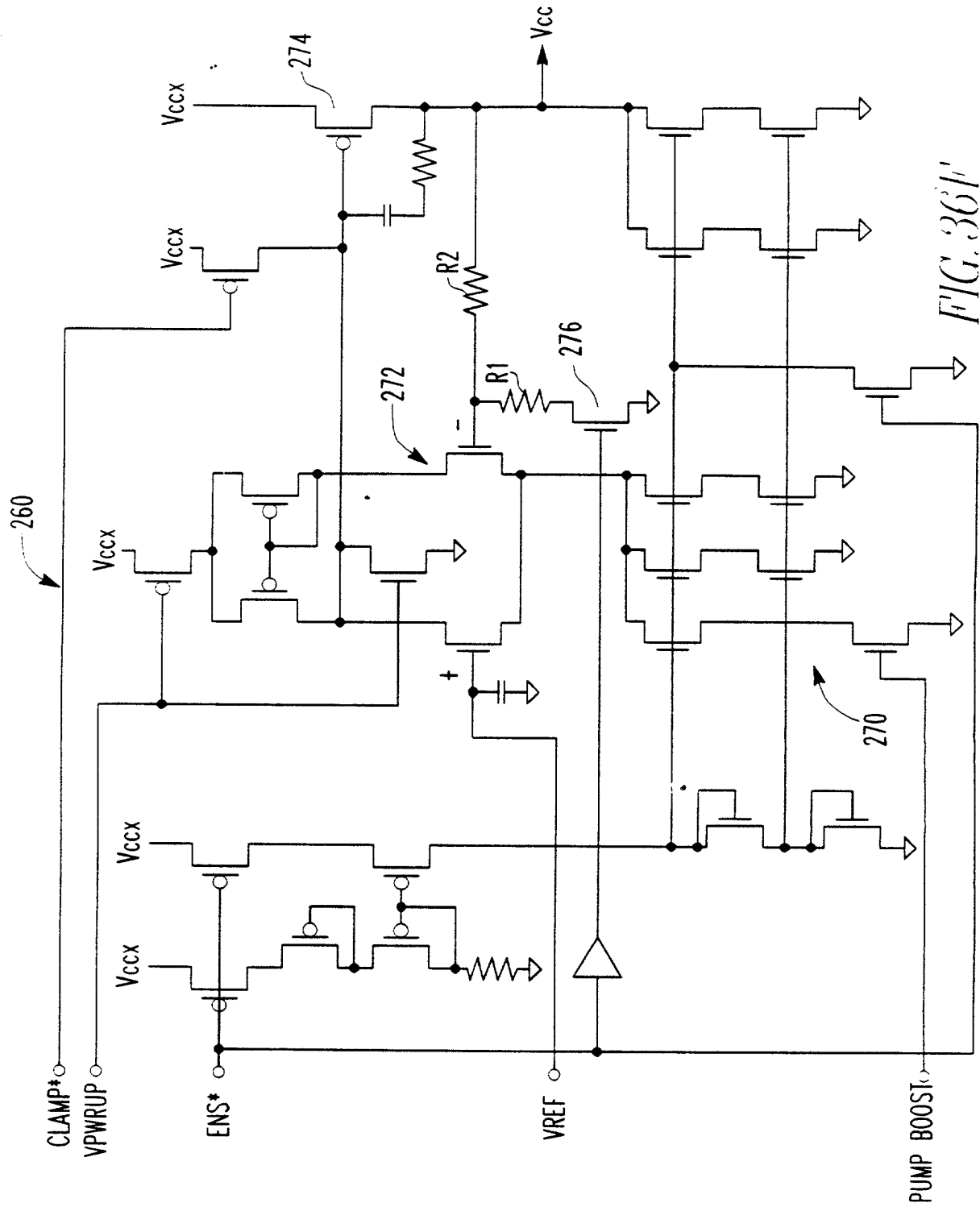


FIG. 36E



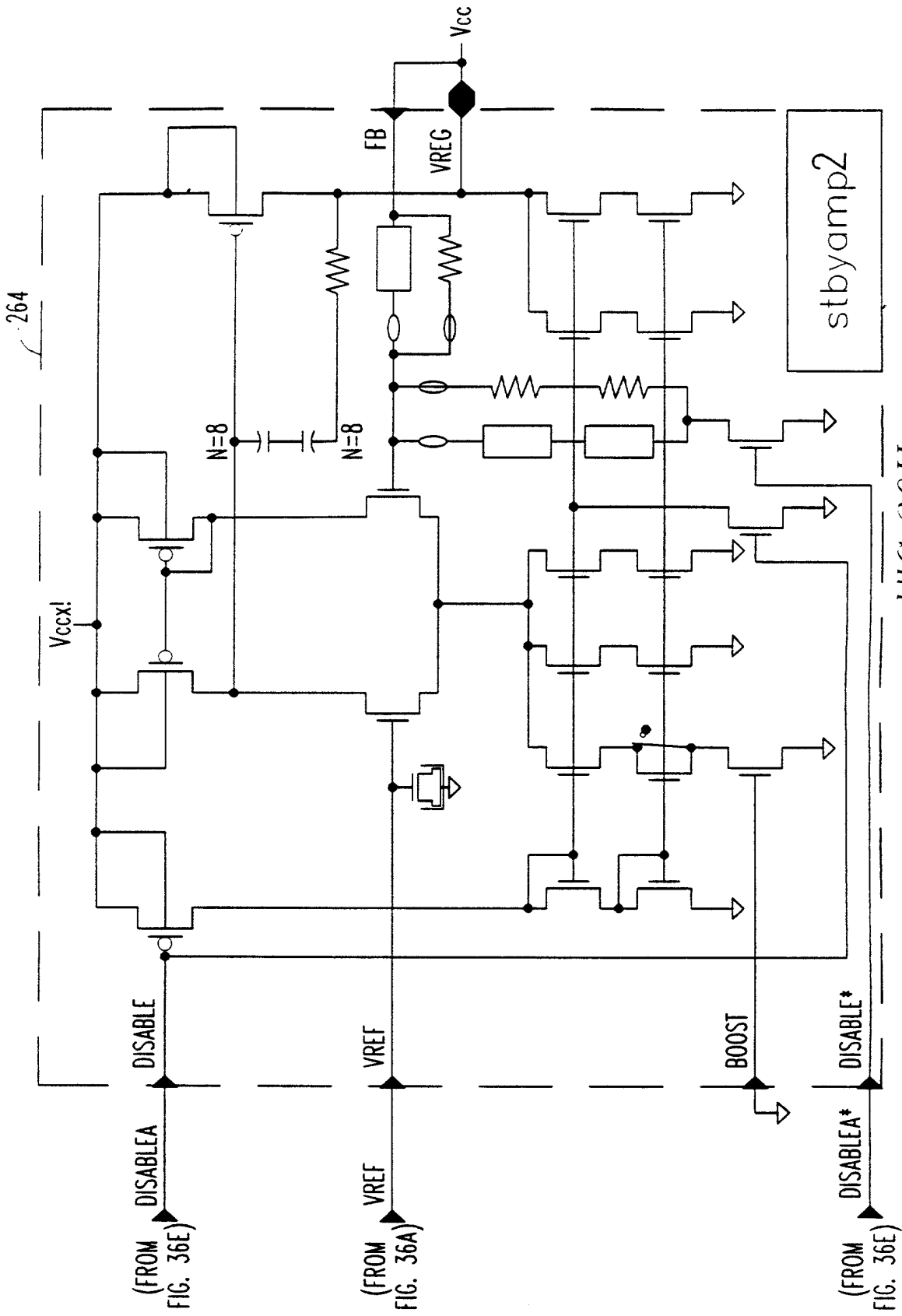


FIG. 36H

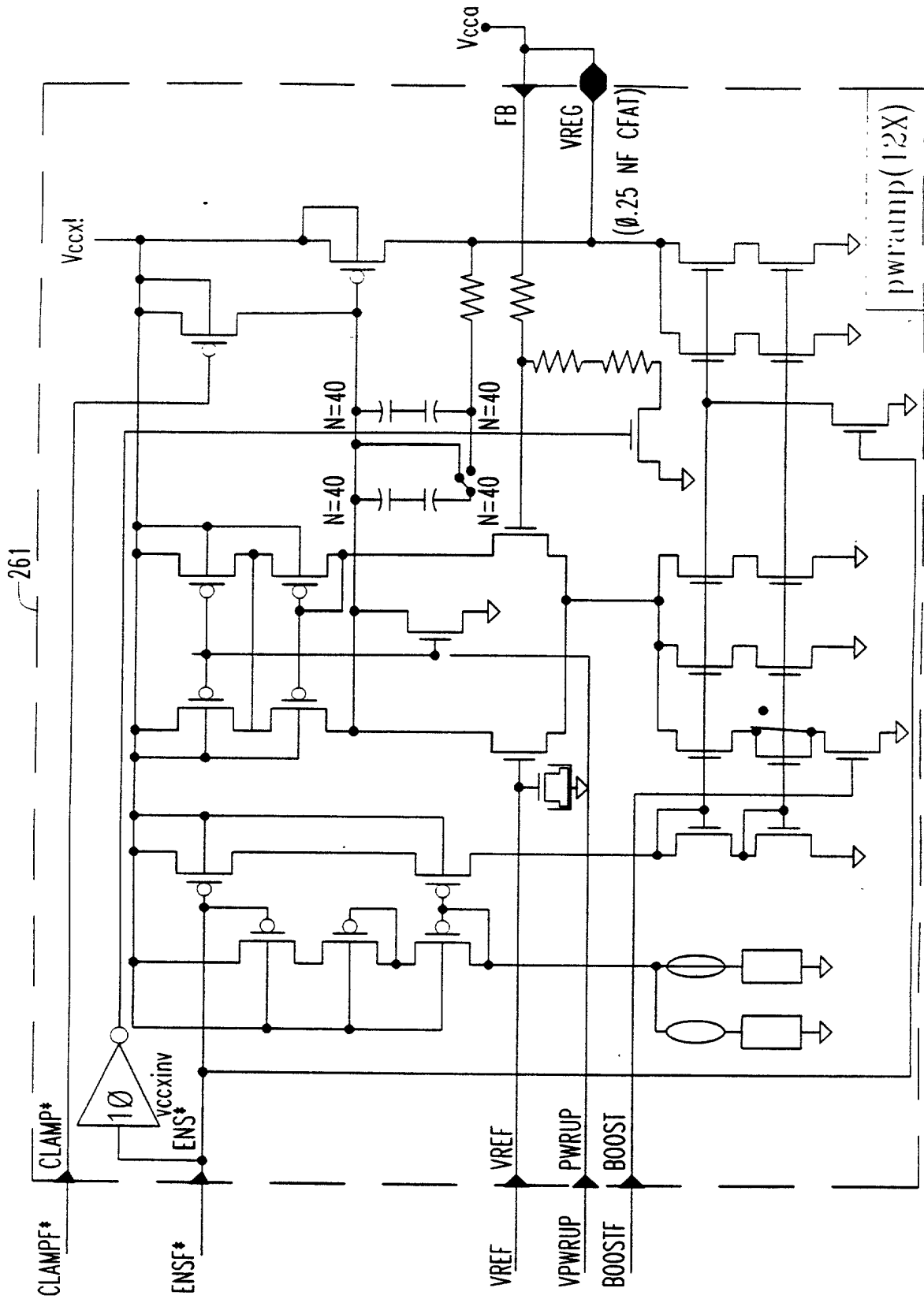


FIG. 361

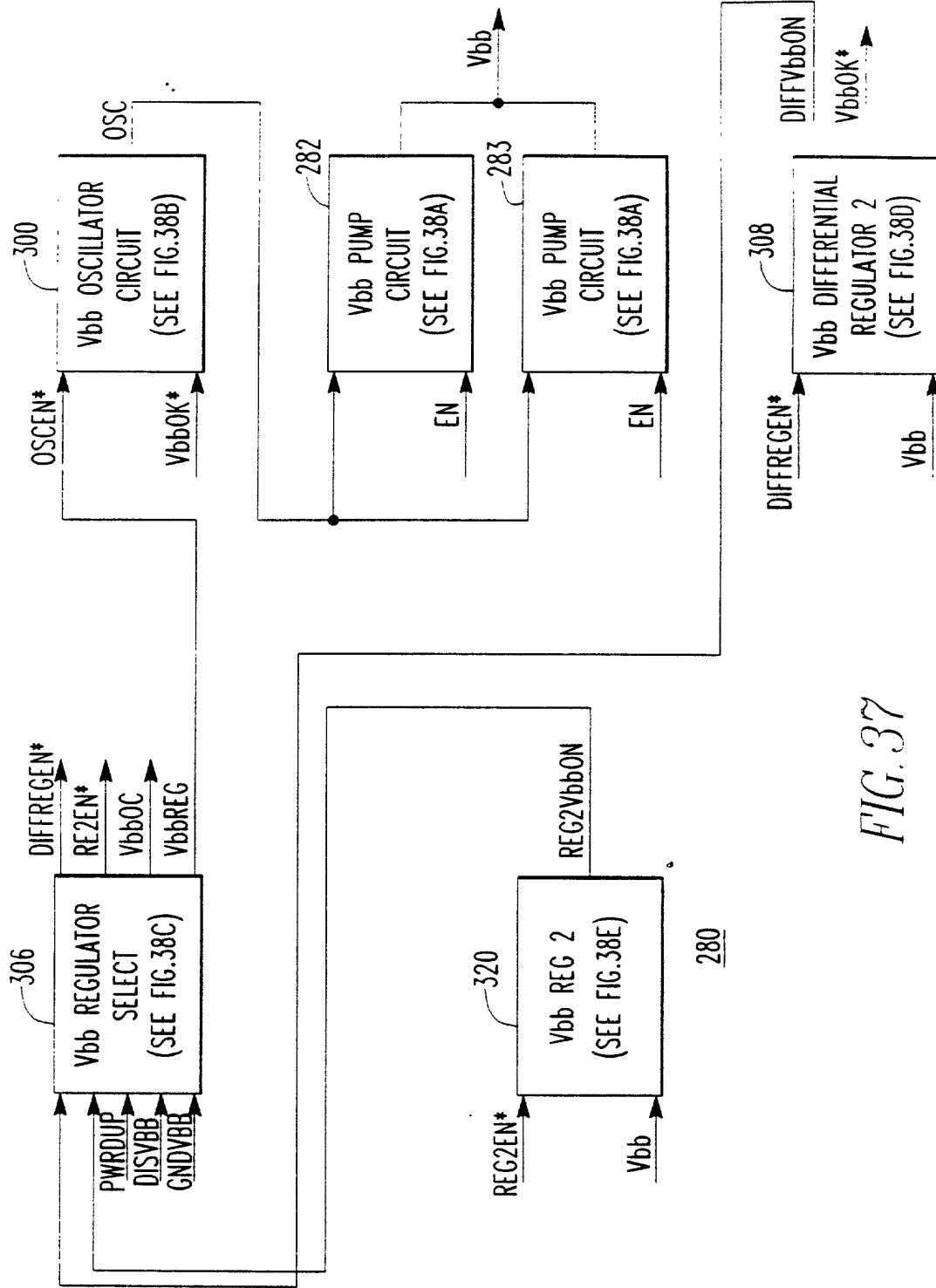


FIG. 37

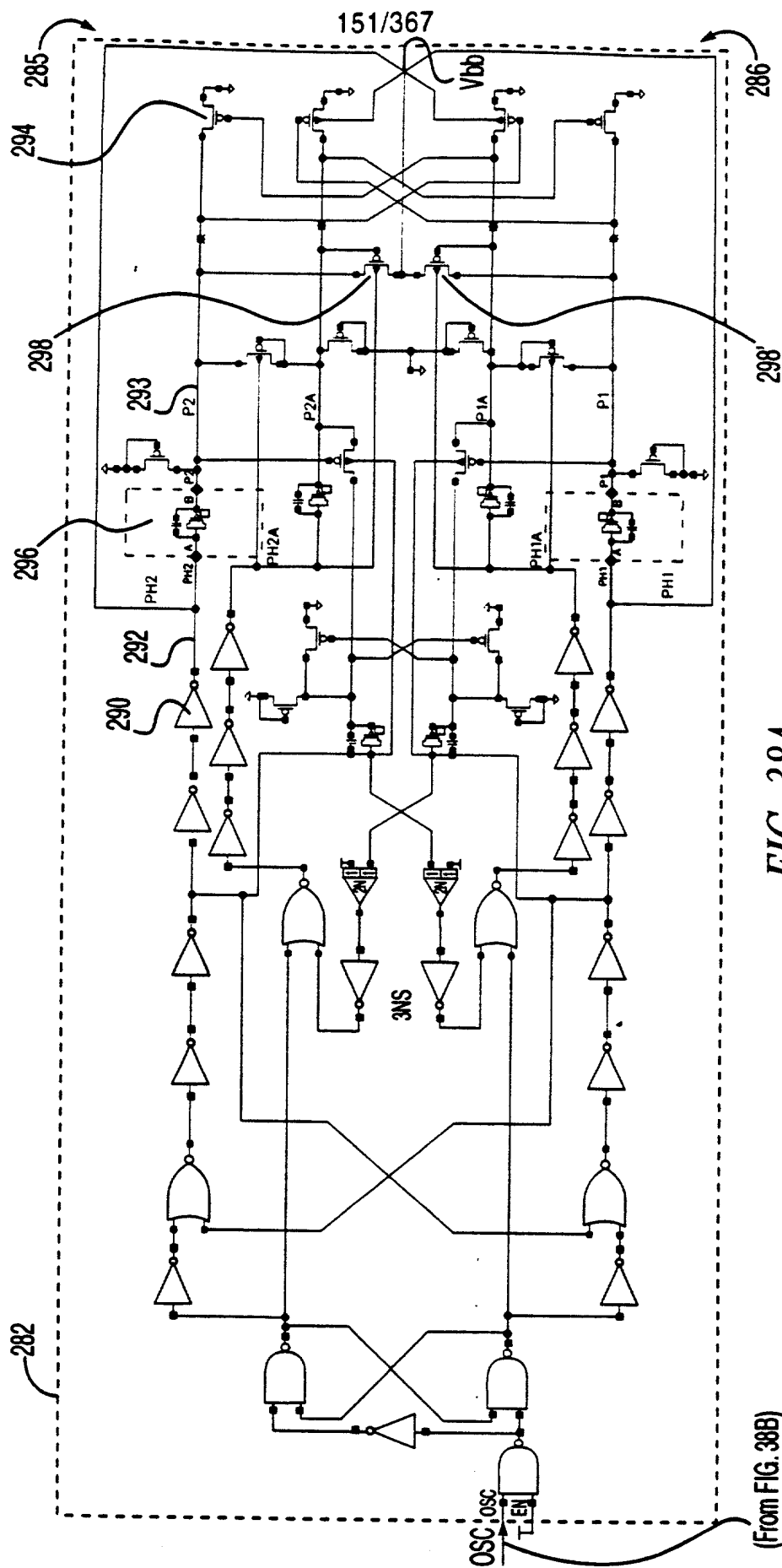
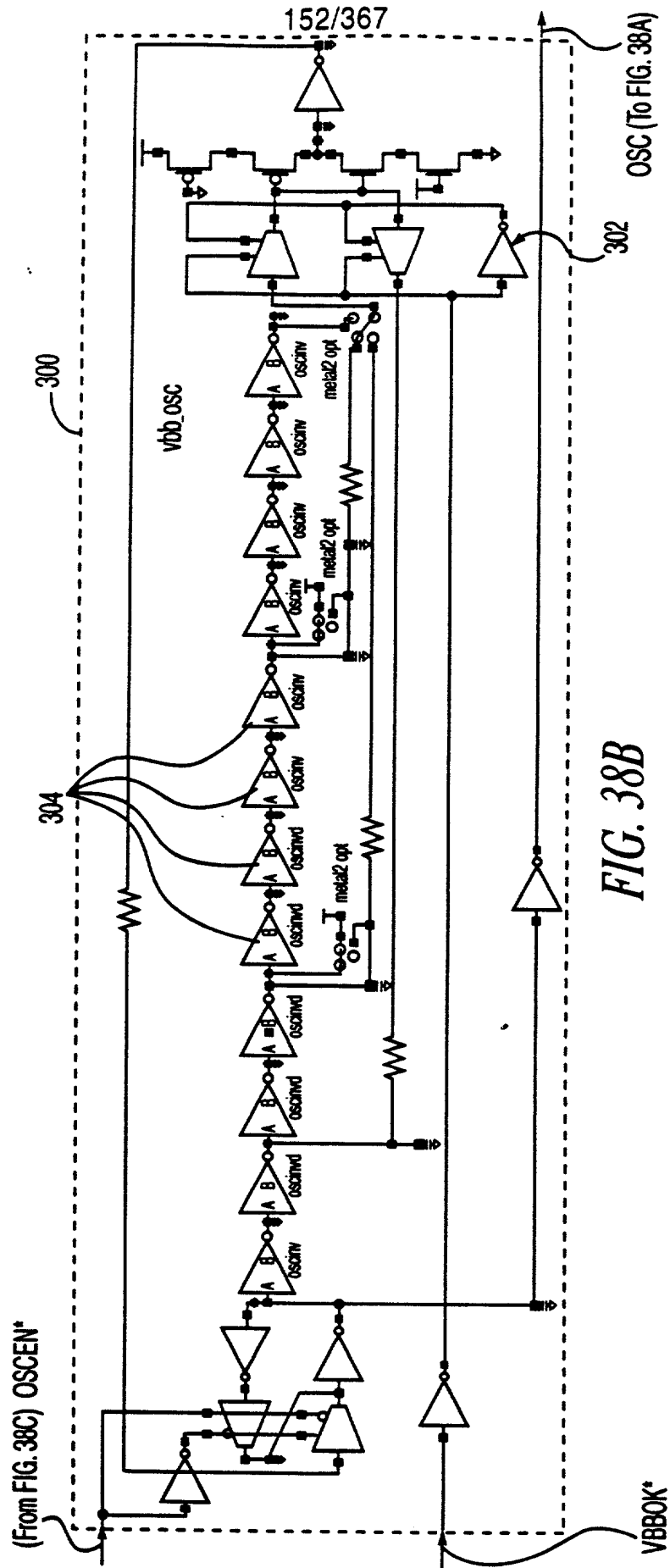


FIG. 38A

(From FIG. 38B)



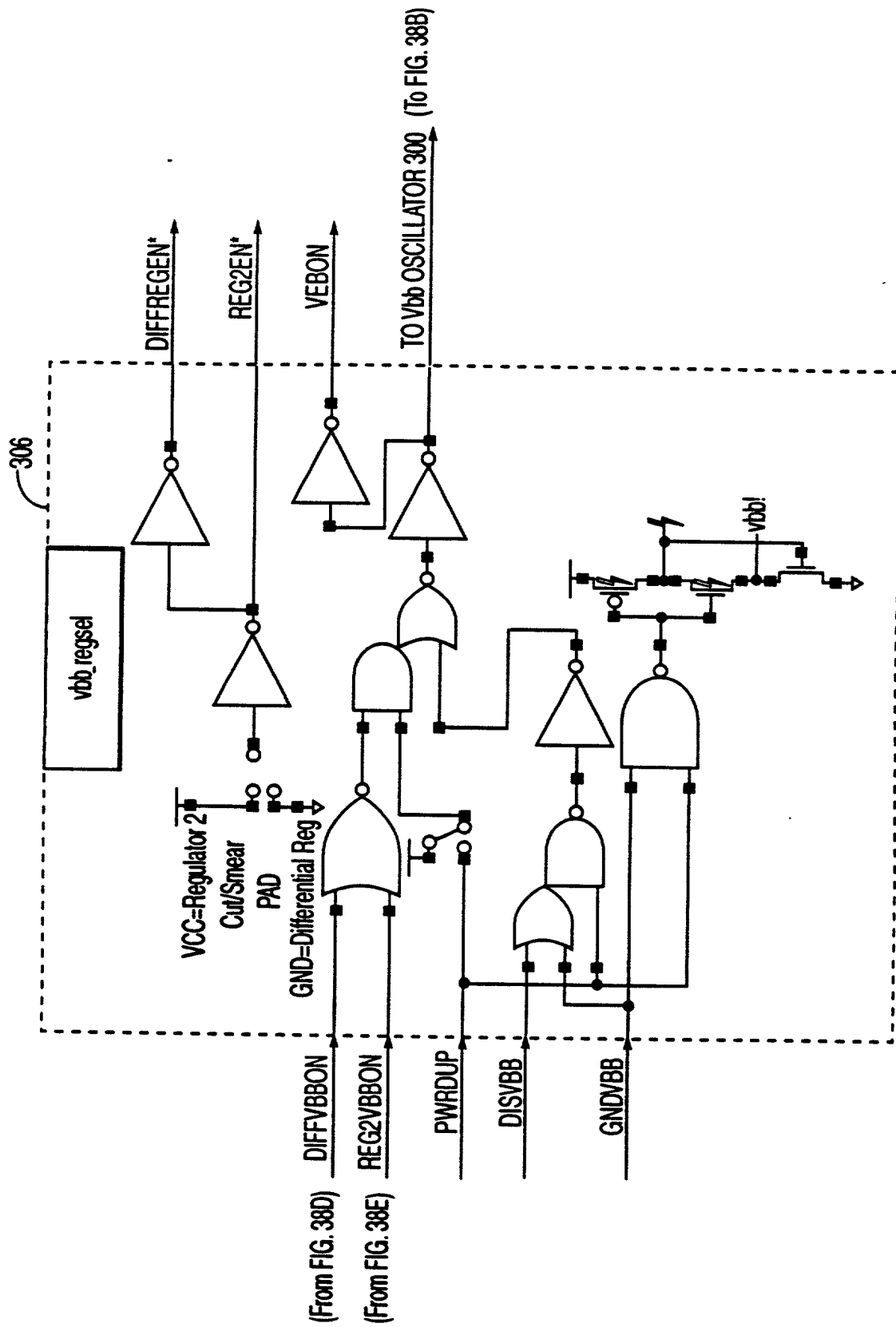


FIG. 38C

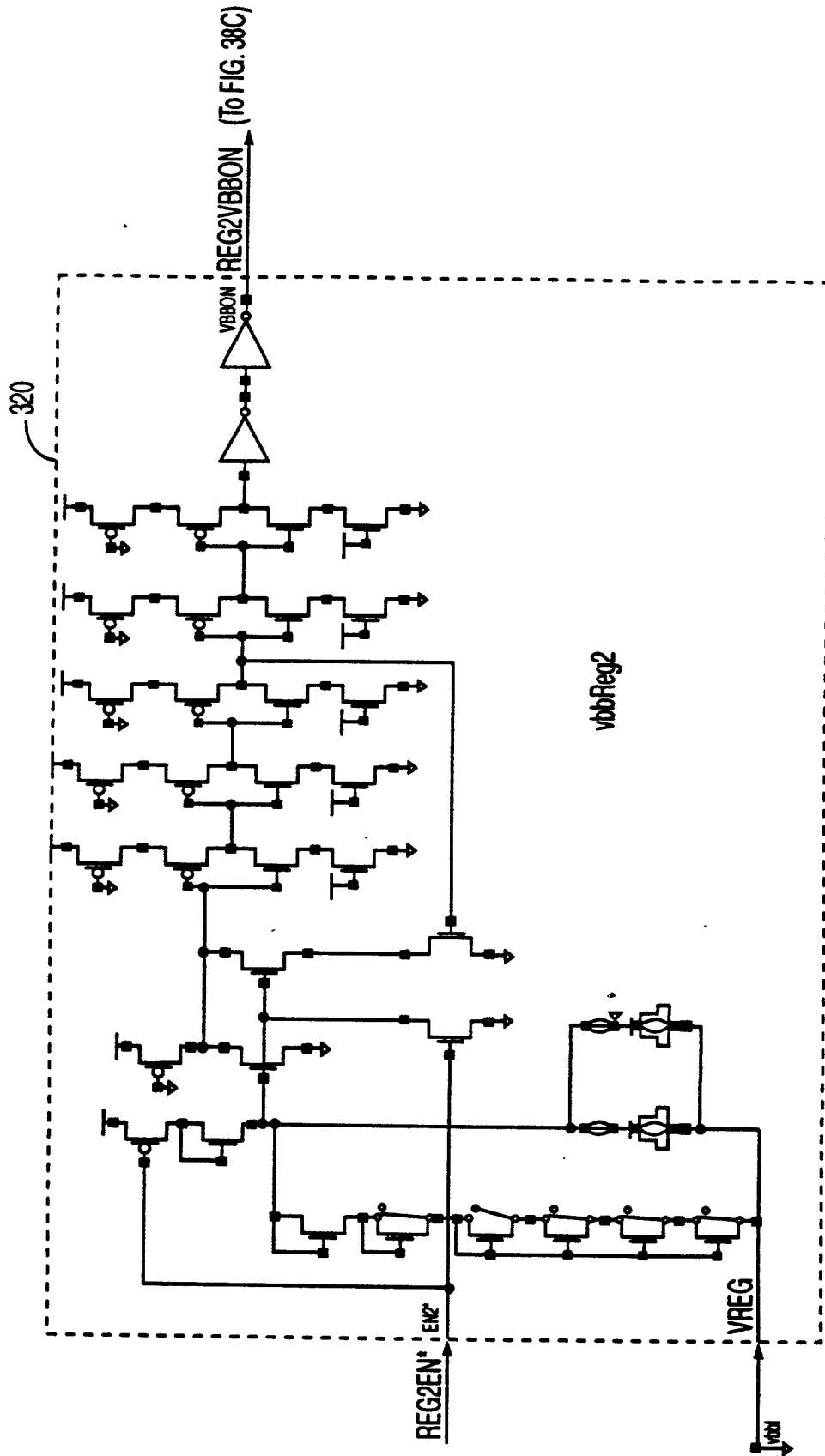


FIG. 38E

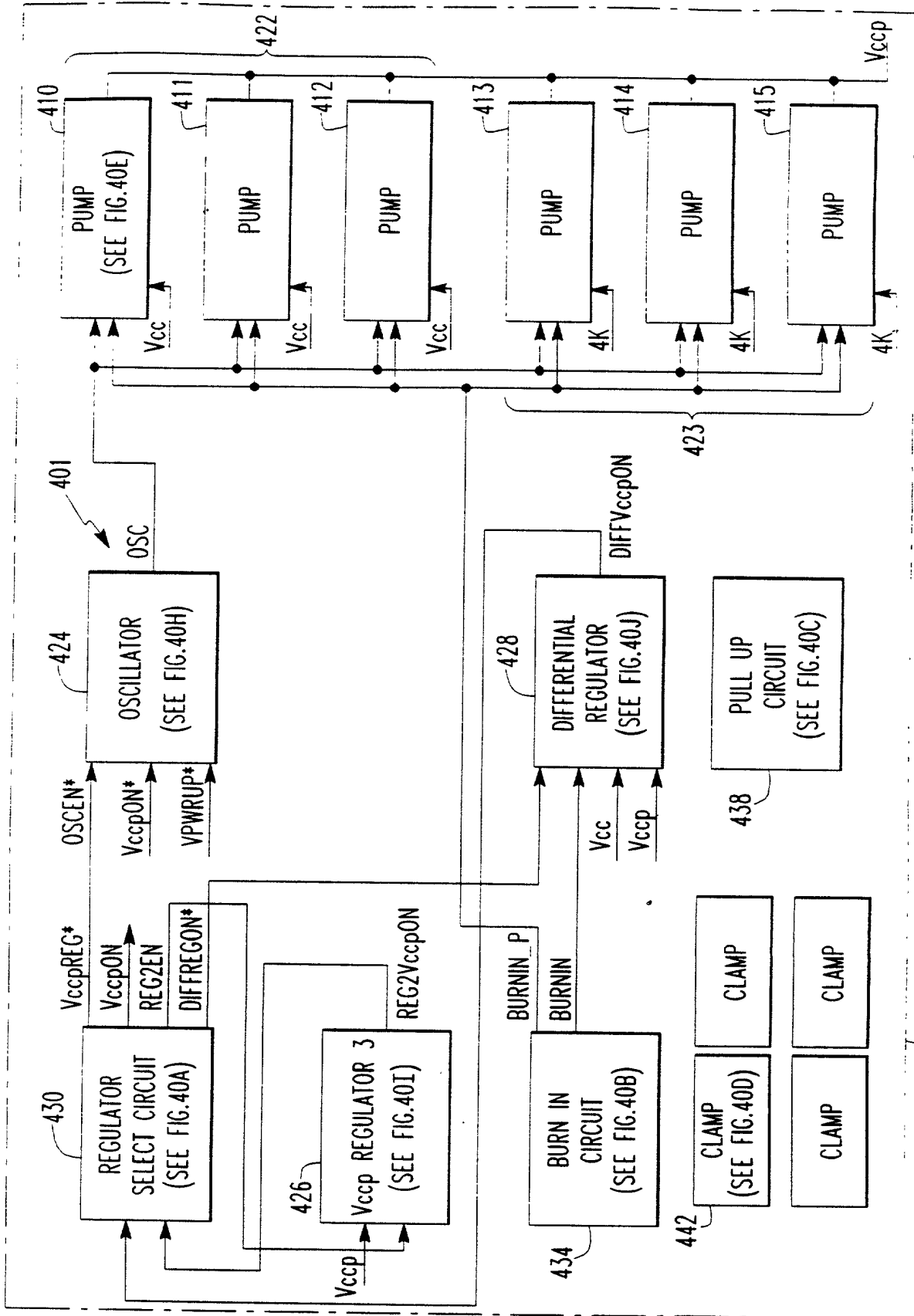


FIG. 39

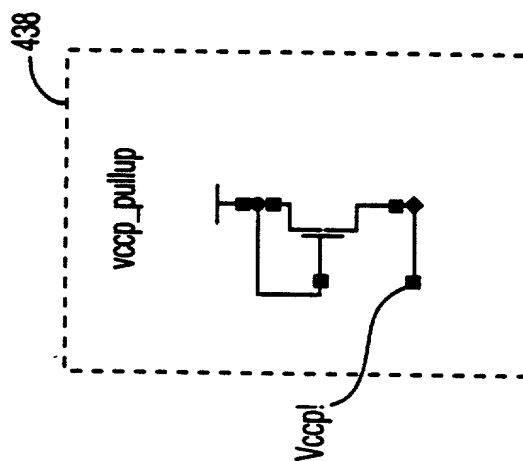


FIG. 40C

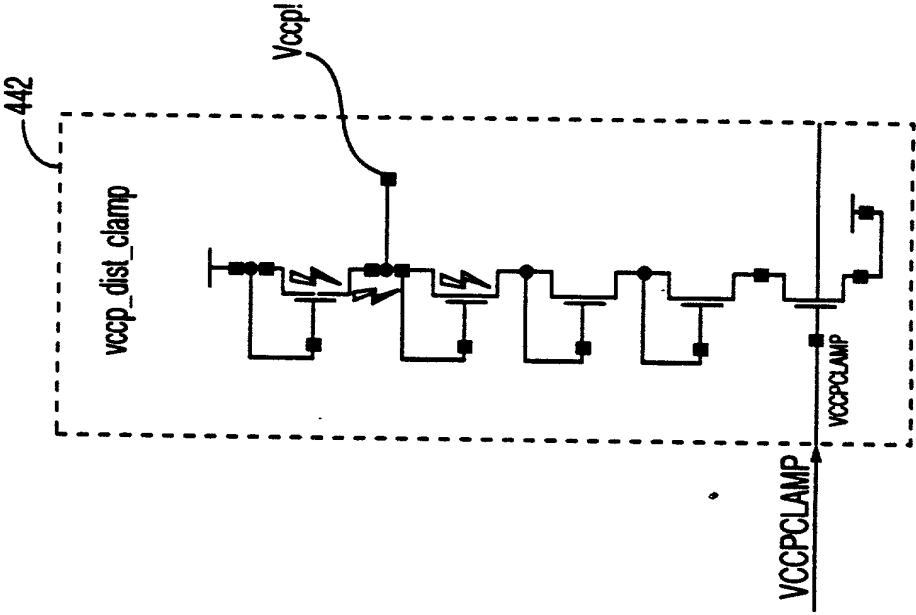


FIG. 40D



(From FIG. 40H) VCCPOSC

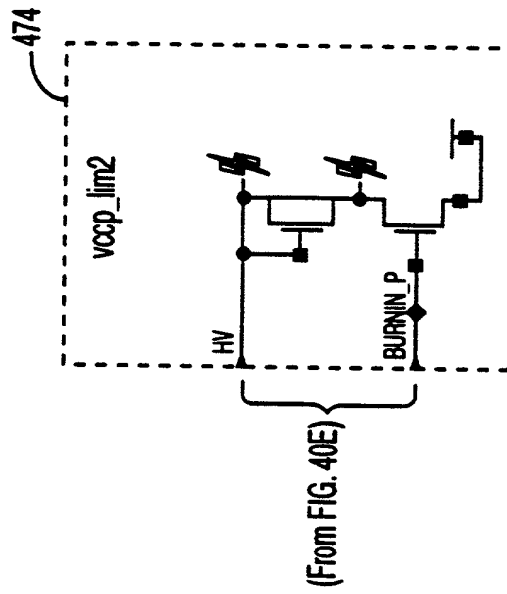


FIG. 40F

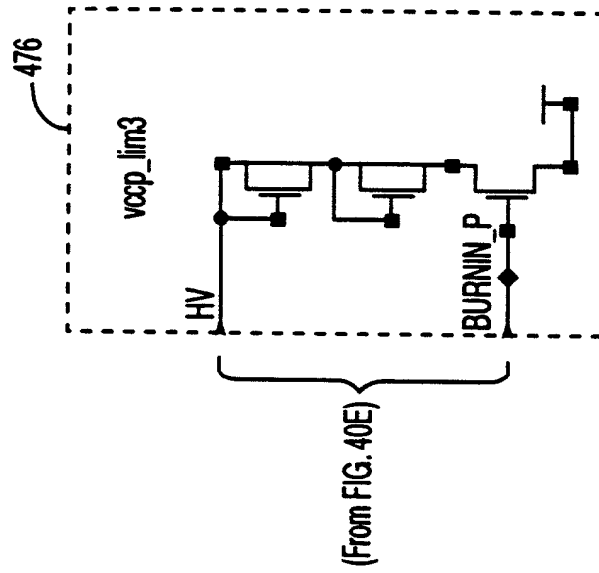


FIG. 40G



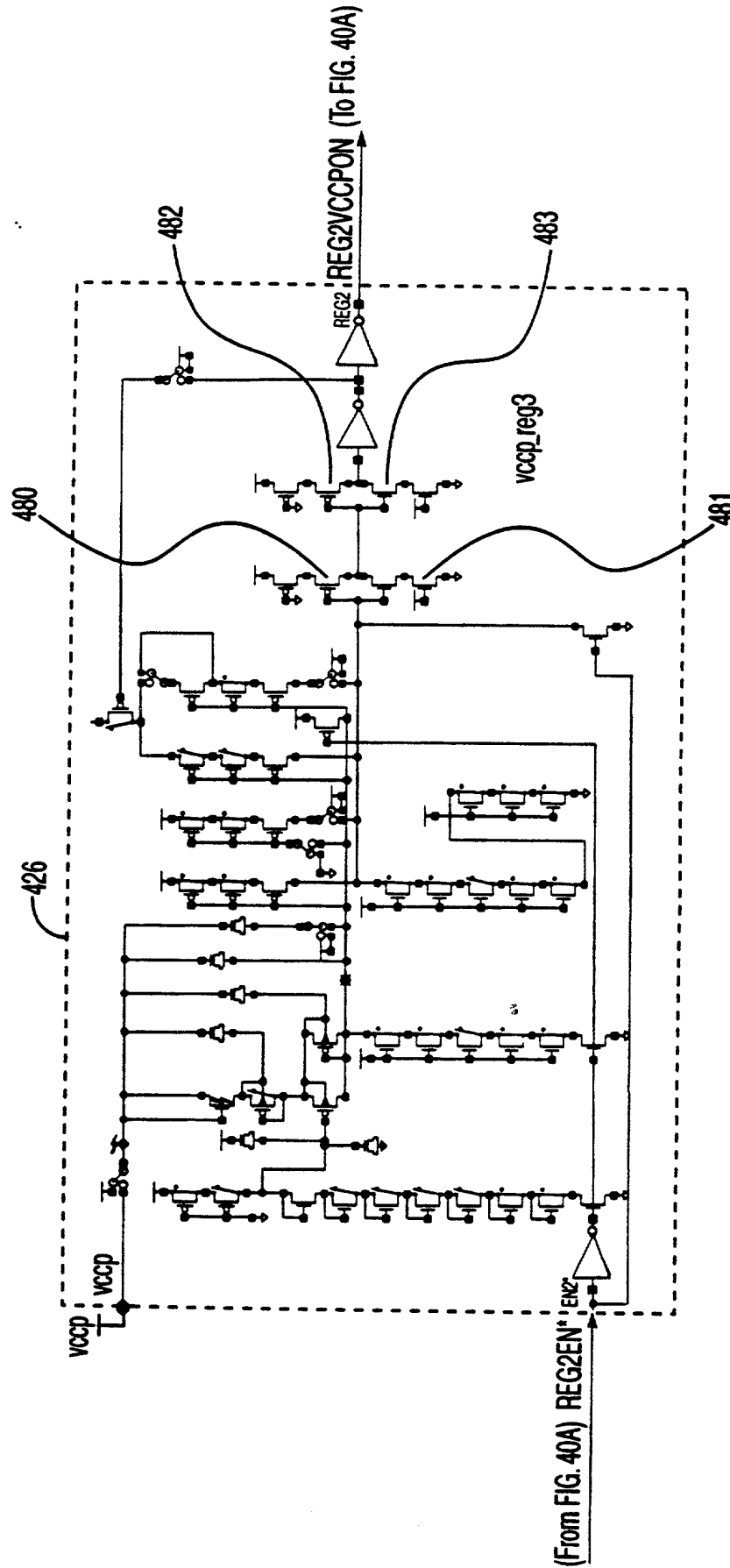


FIG. 40I

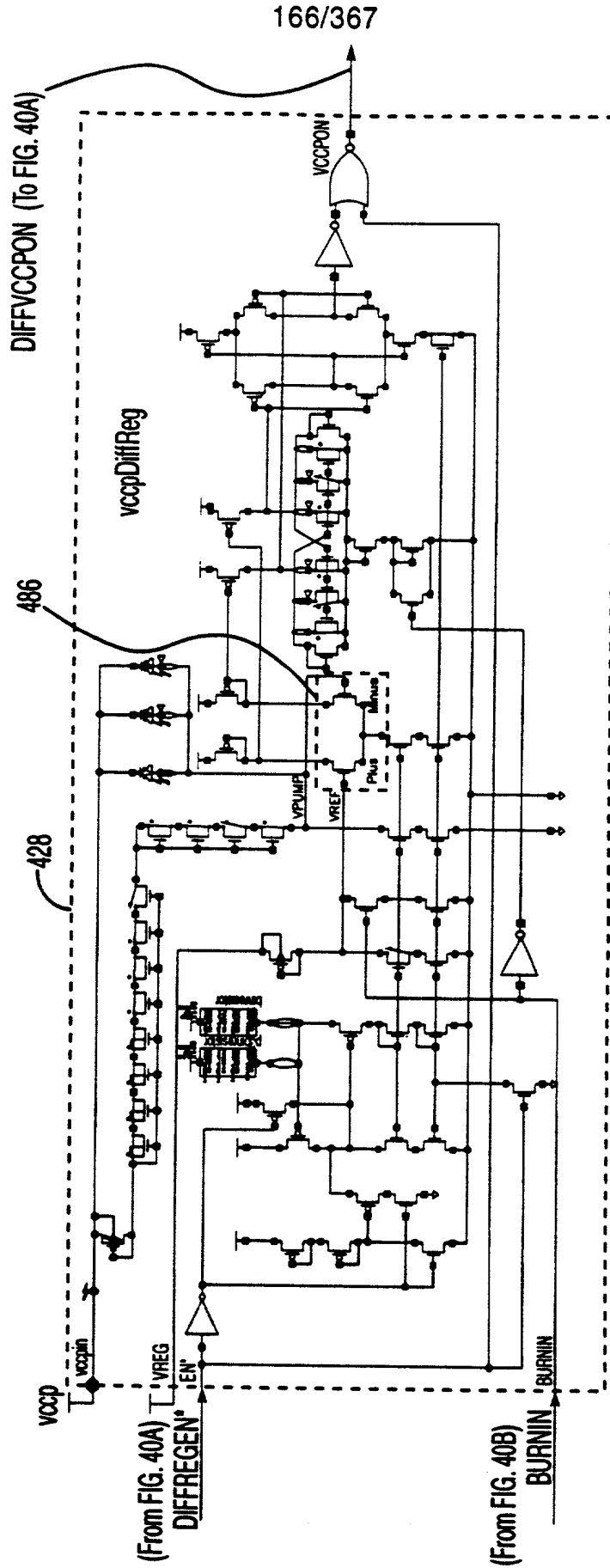
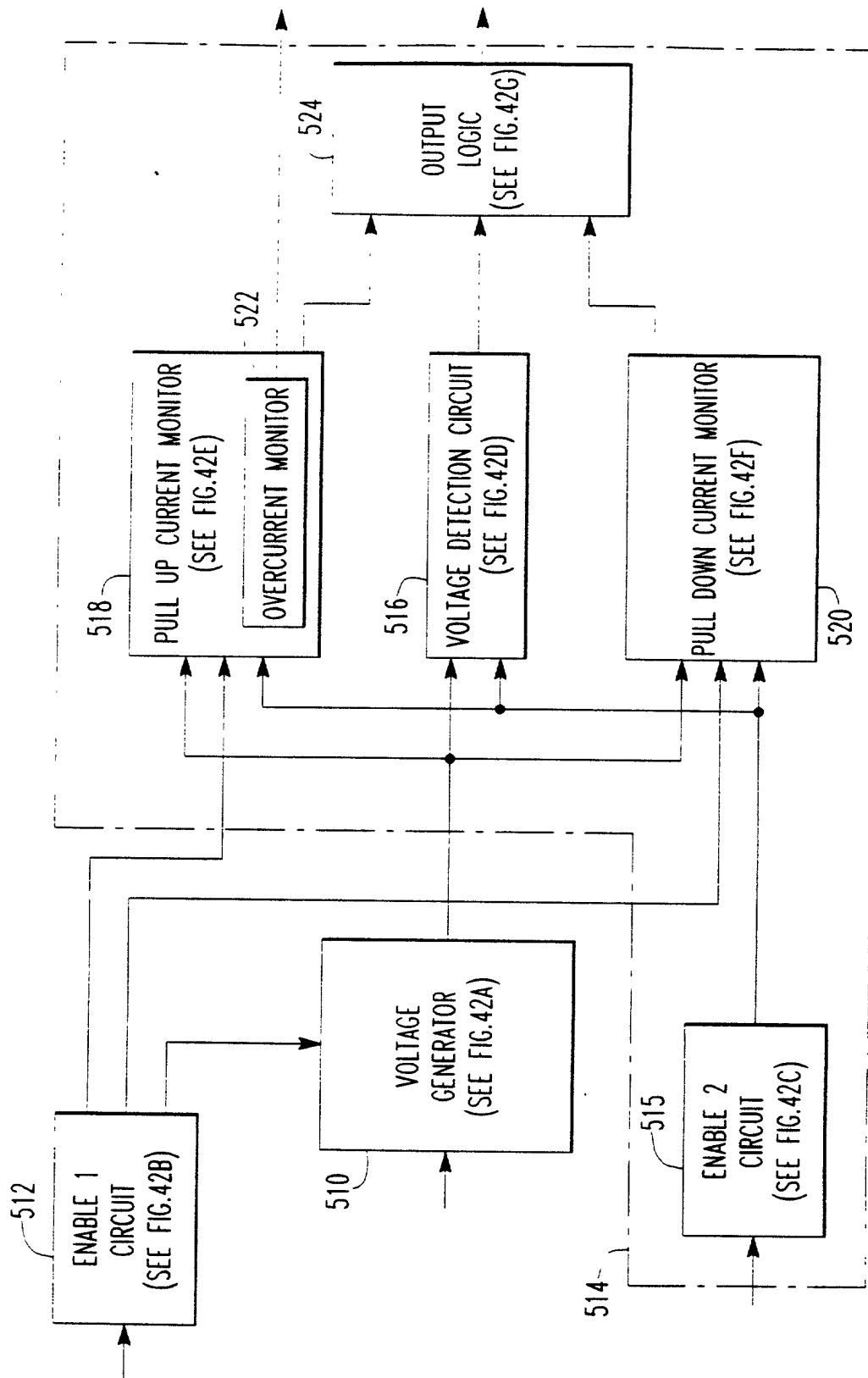


FIG. 40J



500

FIG. 11



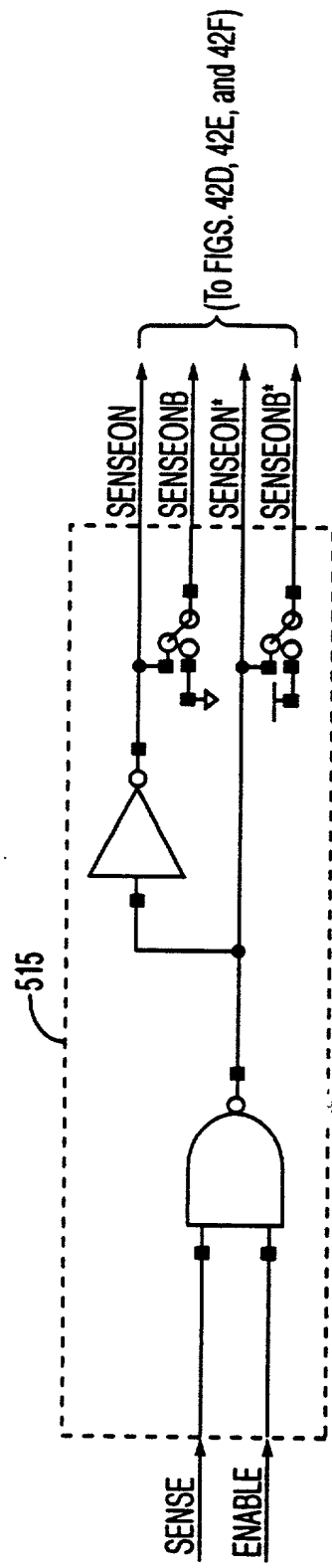


FIG. 42C

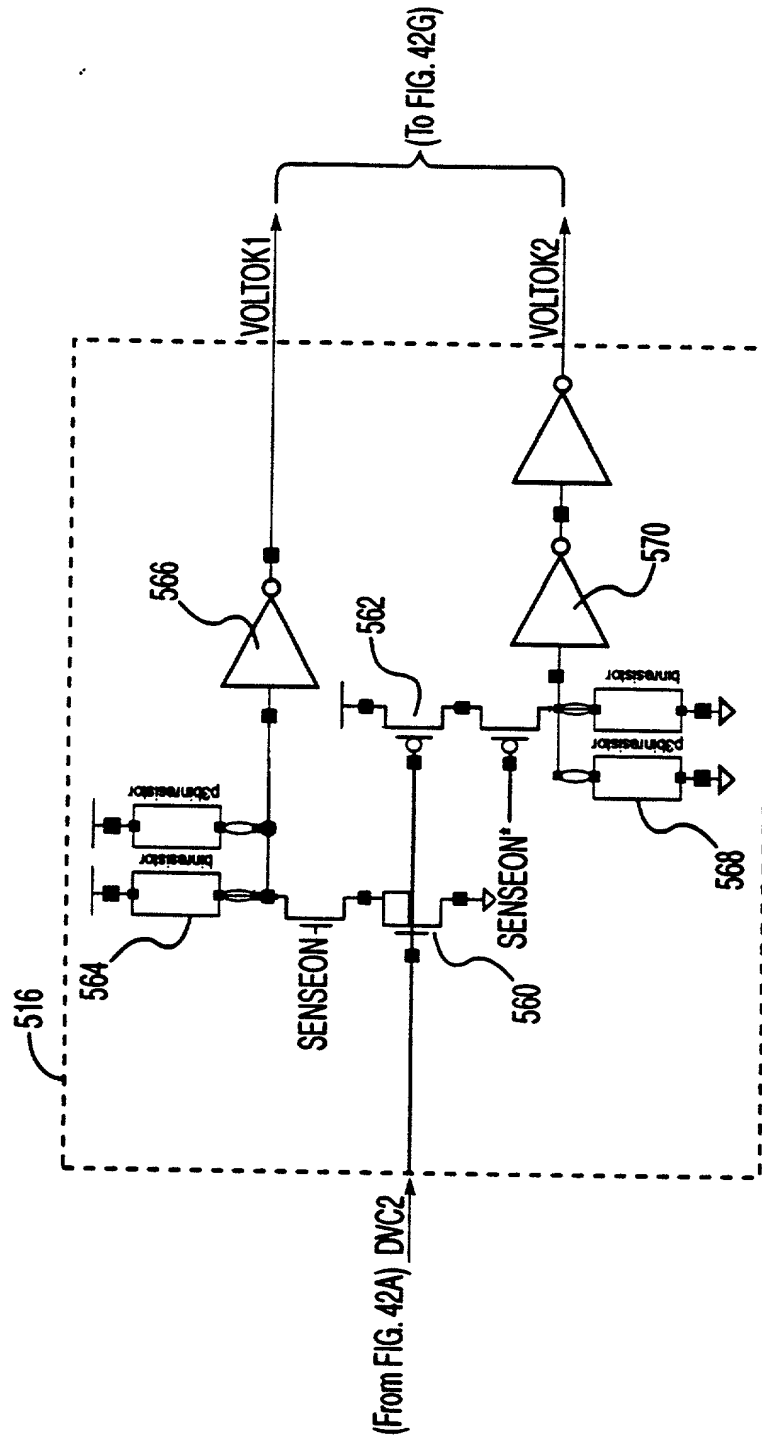


FIG. 42D

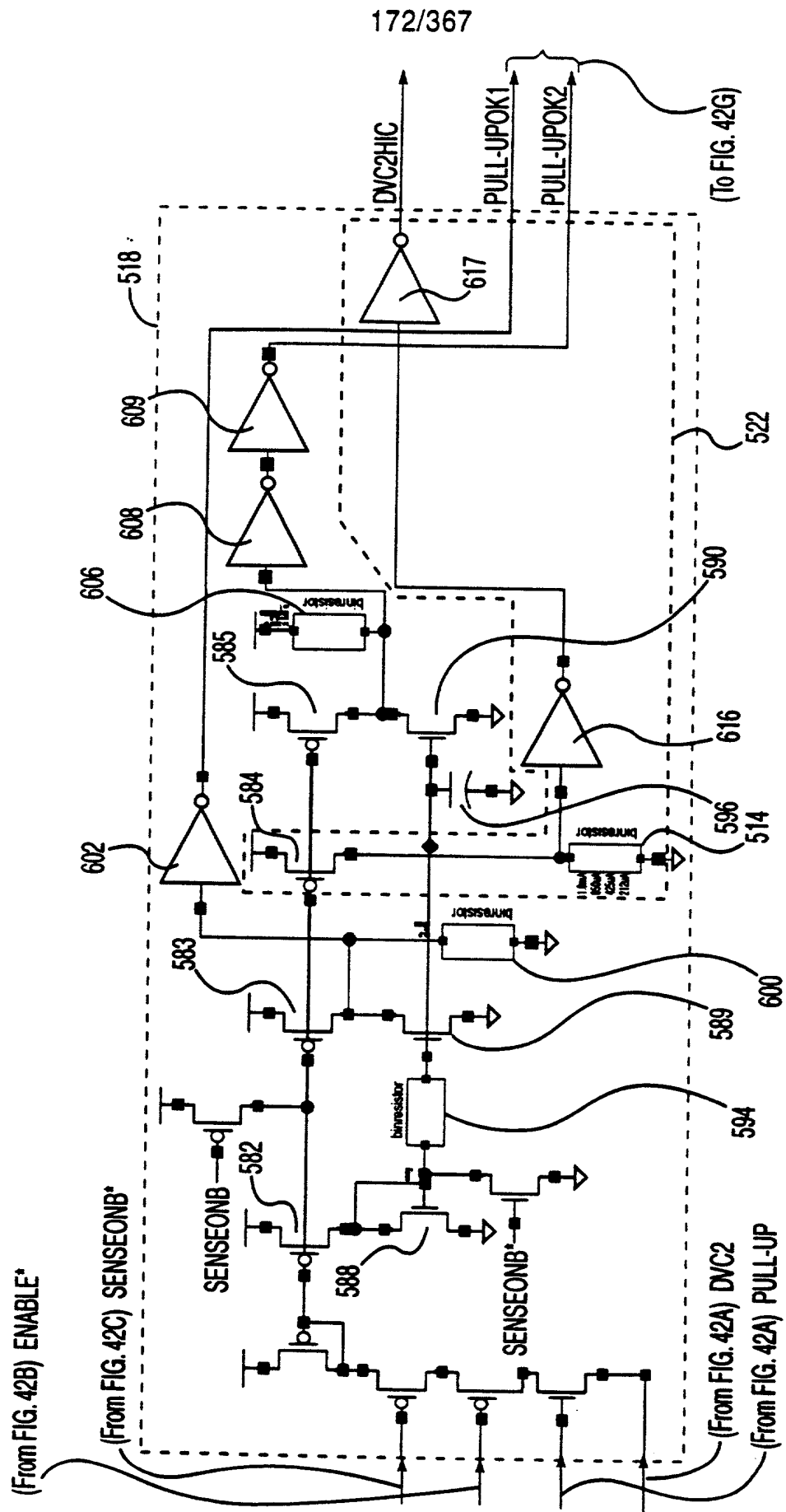


FIG. 42E



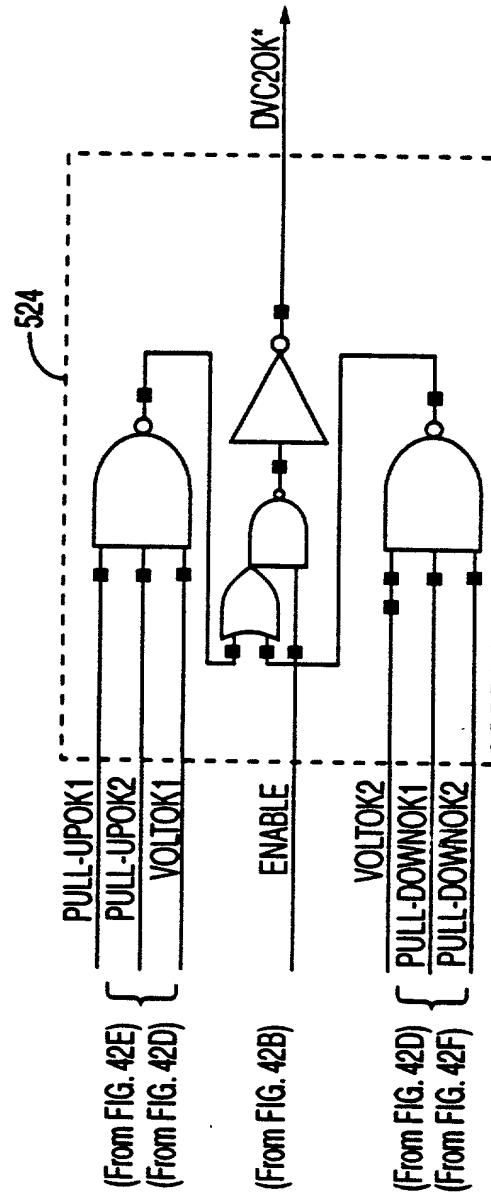


FIG. 42G

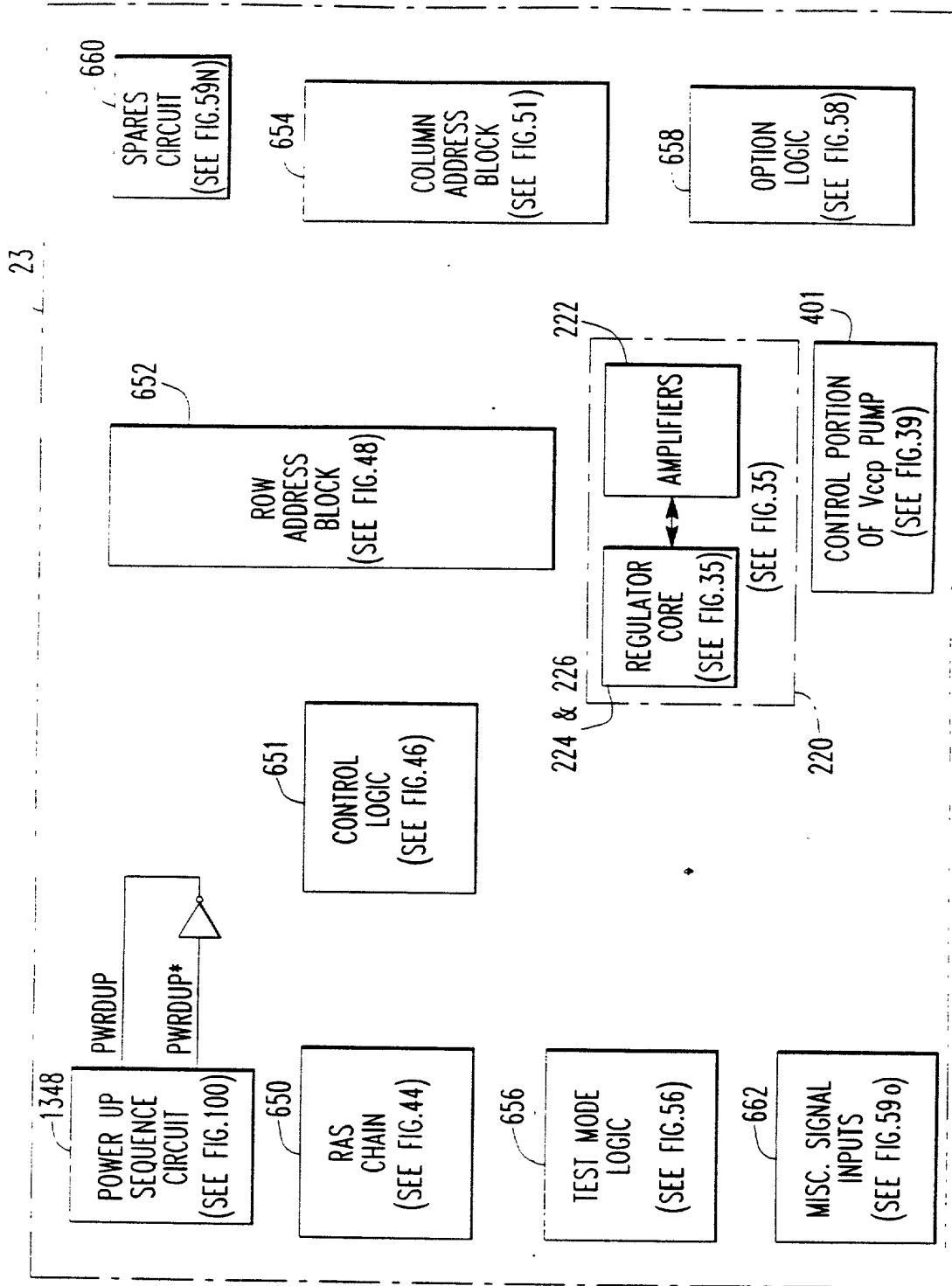


FIG. 43

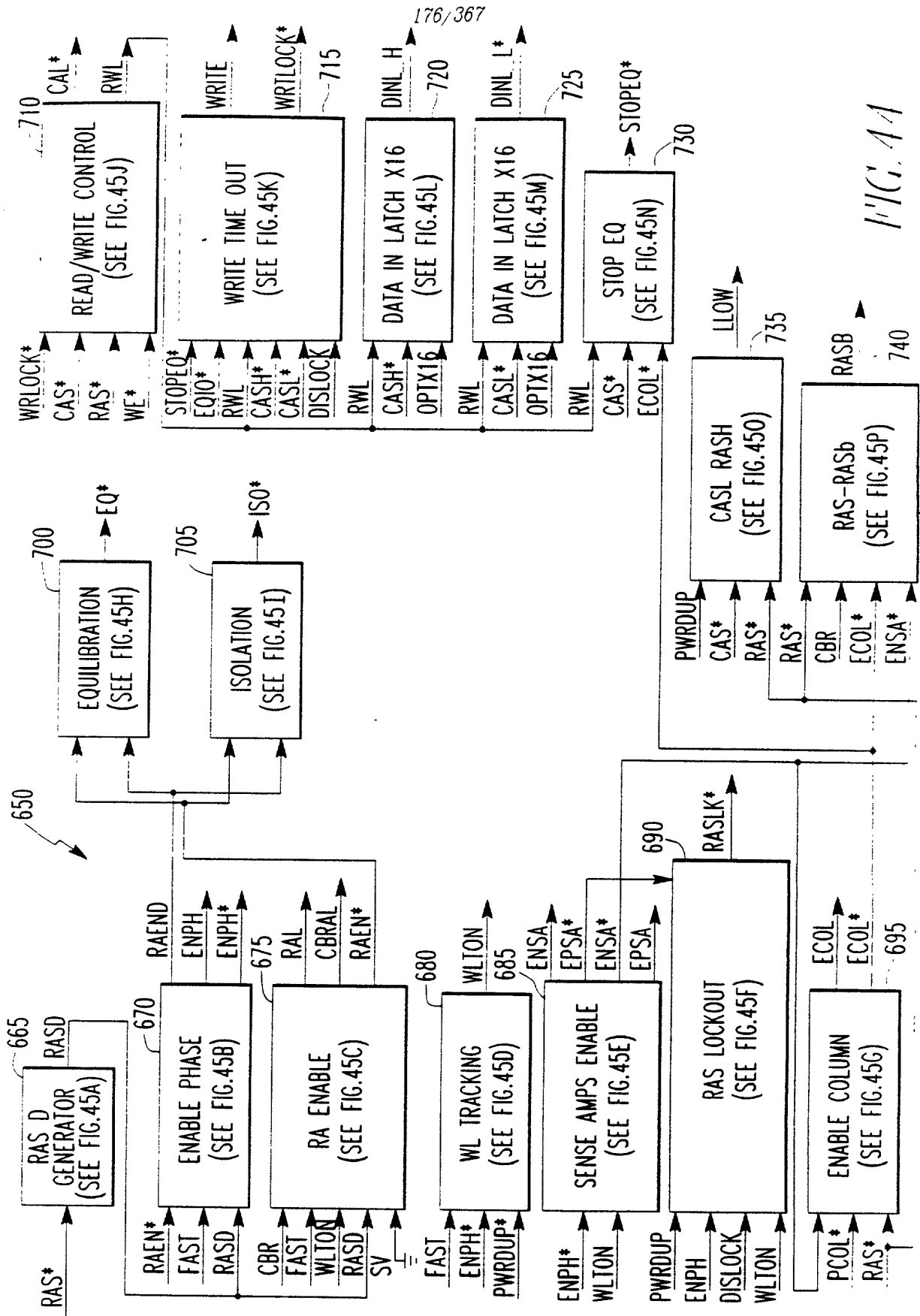


FIG. 44



FIG. 45A

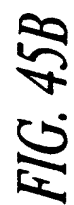


FIG. 45B

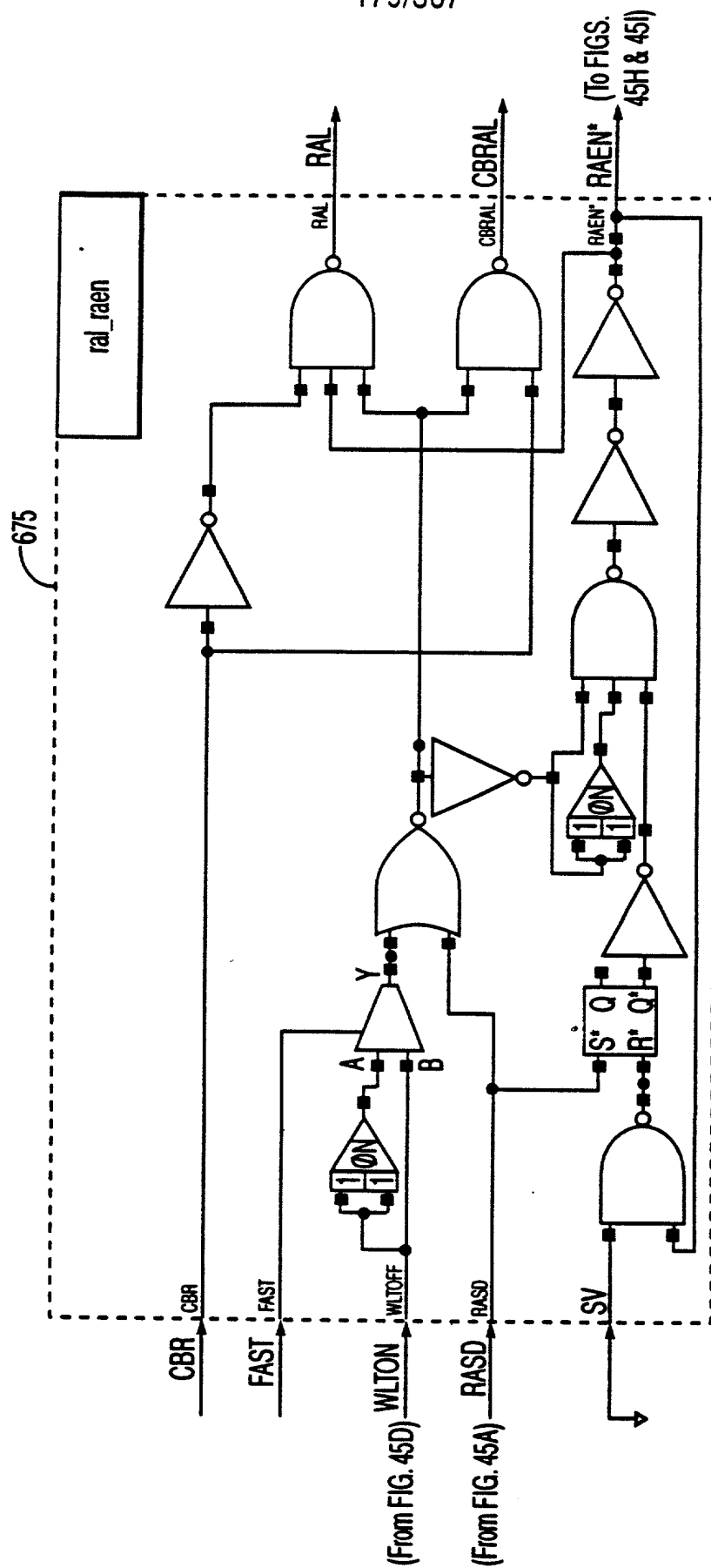


FIG. 45C

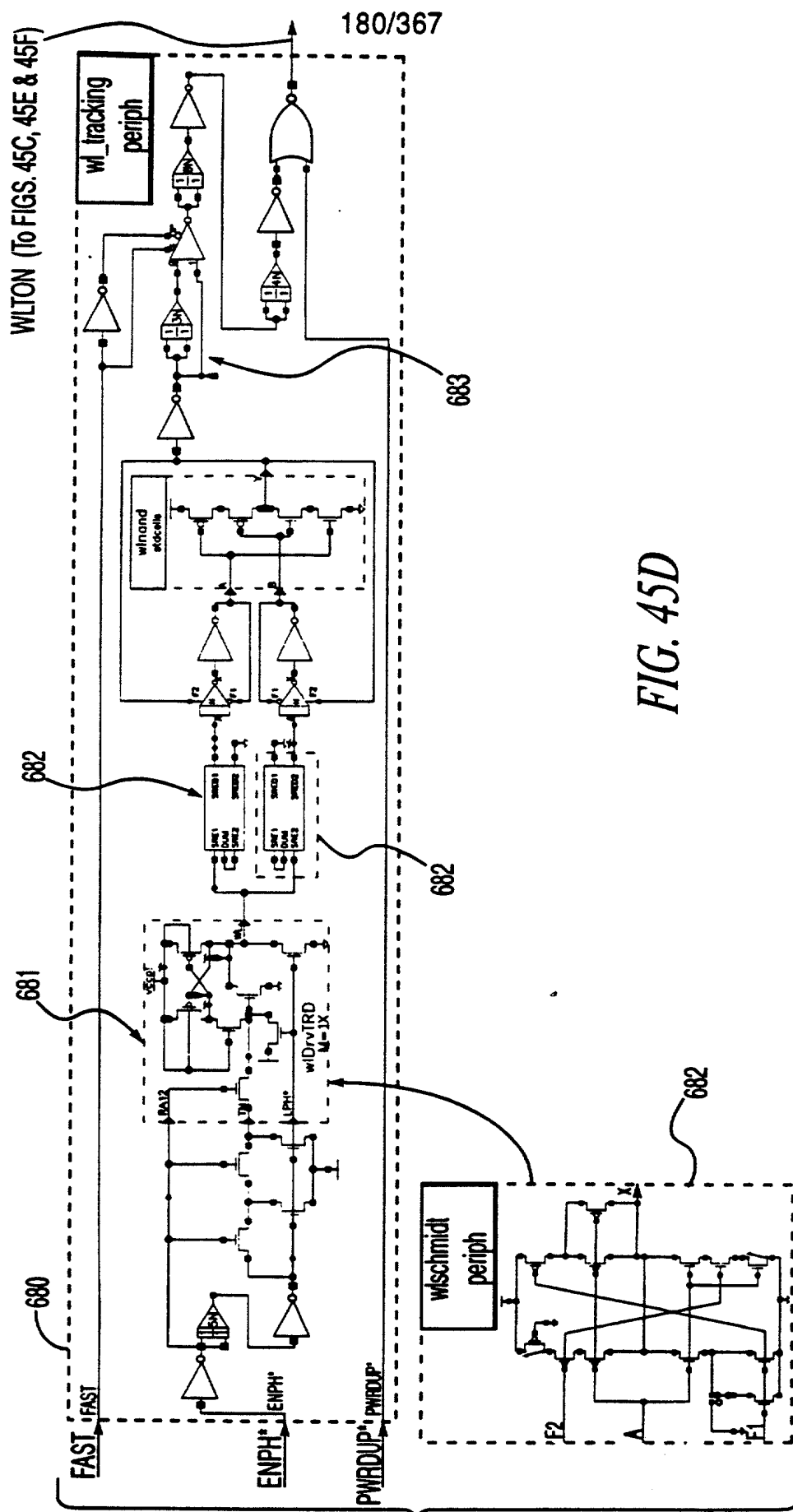


FIG. 45D

(From FIG. 45B)

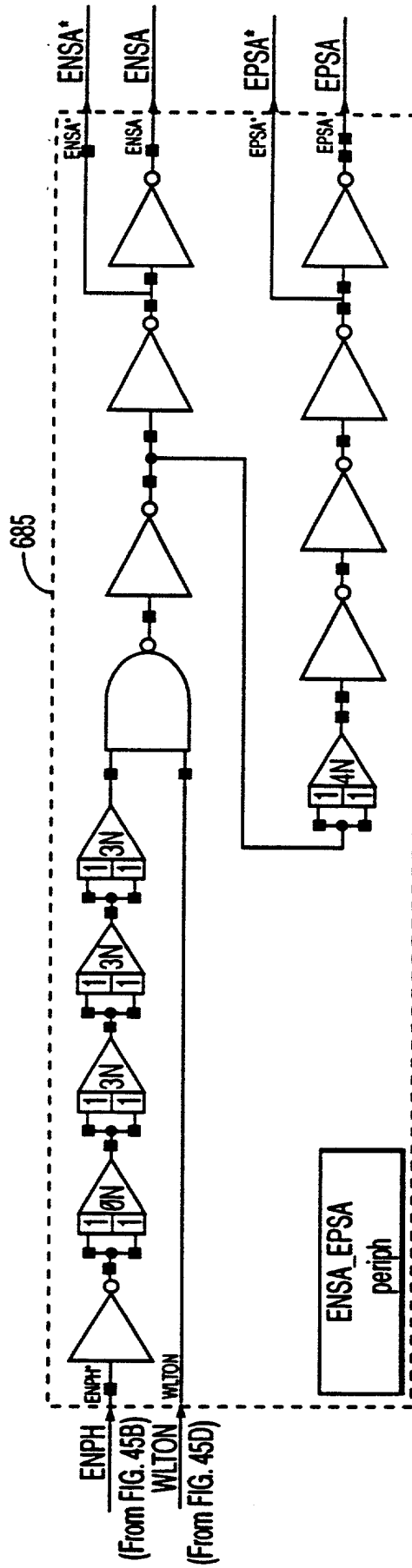


FIG. 45E

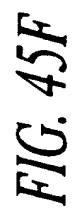


FIG. 45F

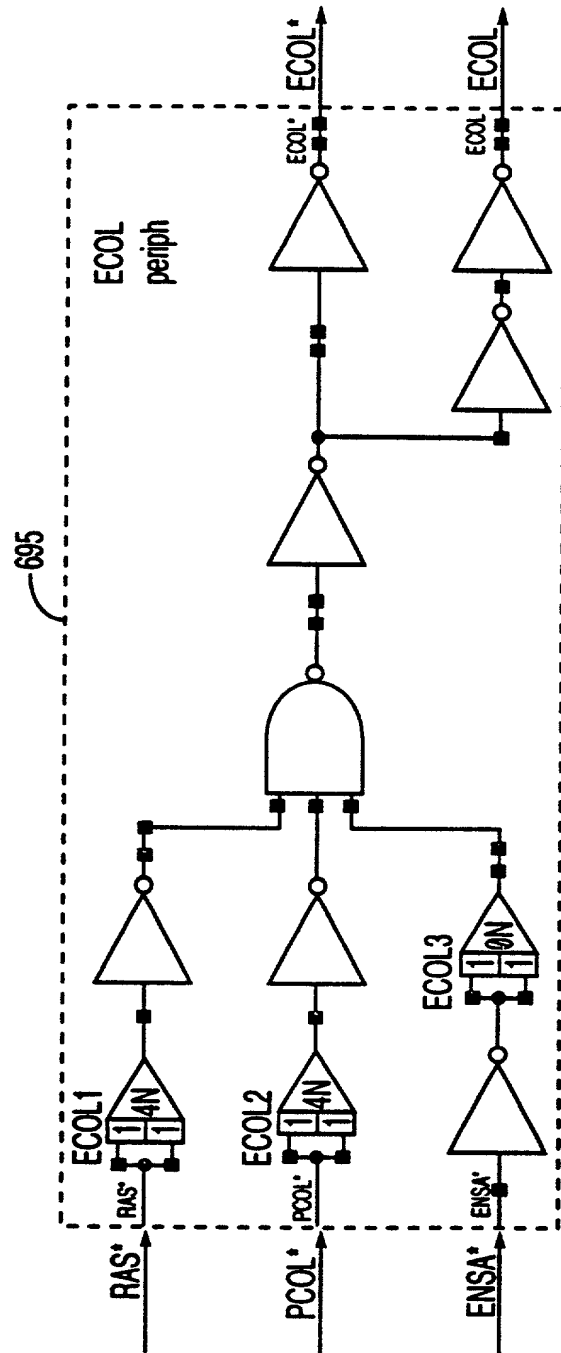


FIG. 45G



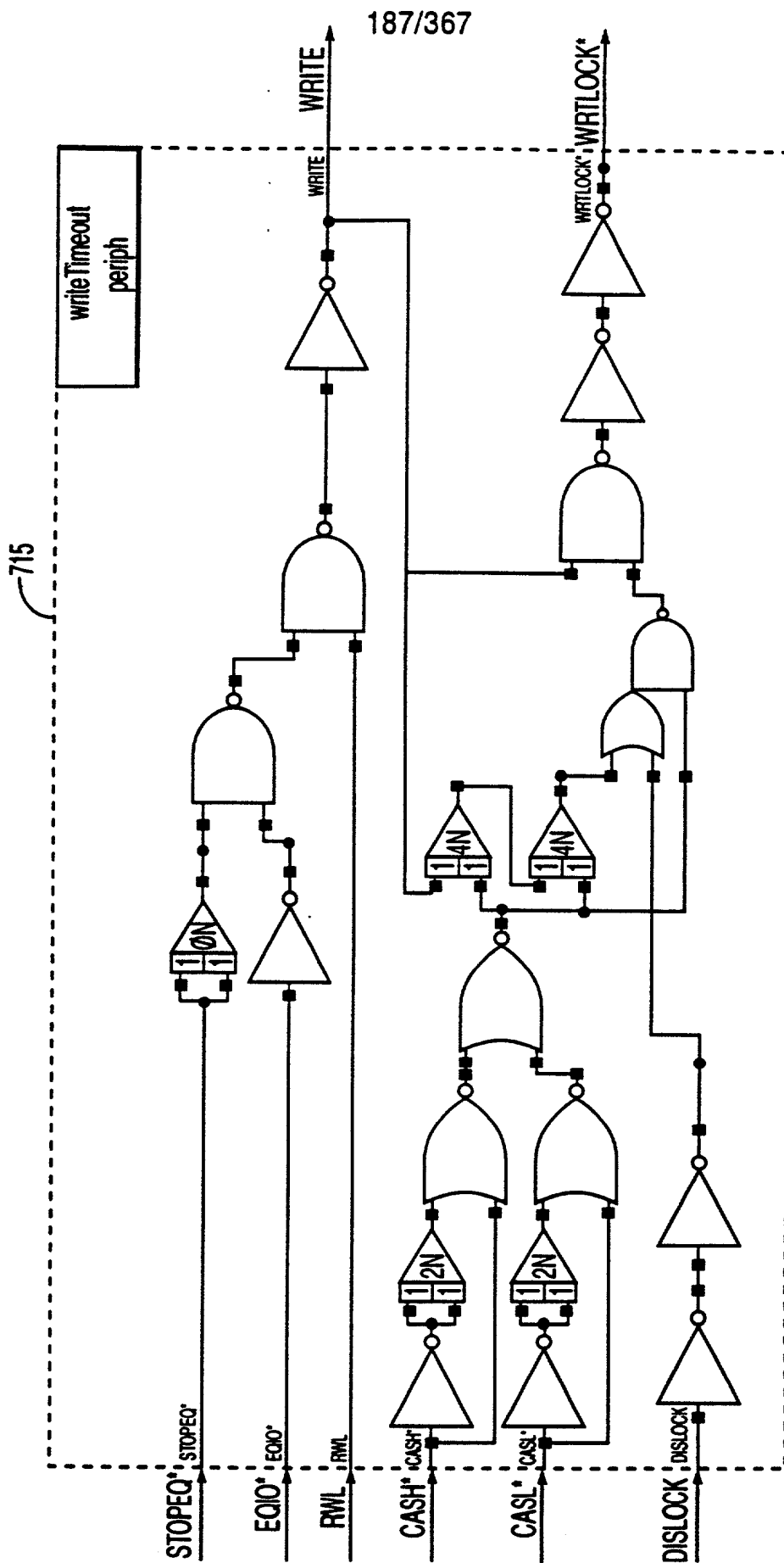


FIG. 45K

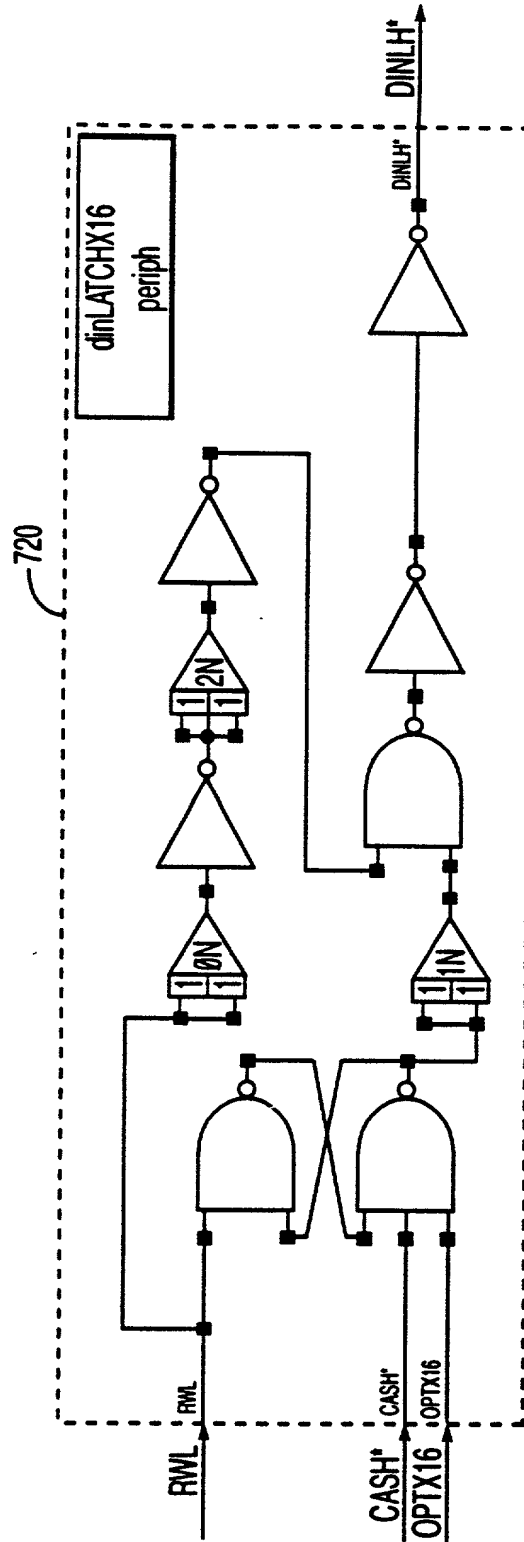


FIG. 45L

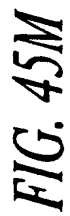


FIG. 45M

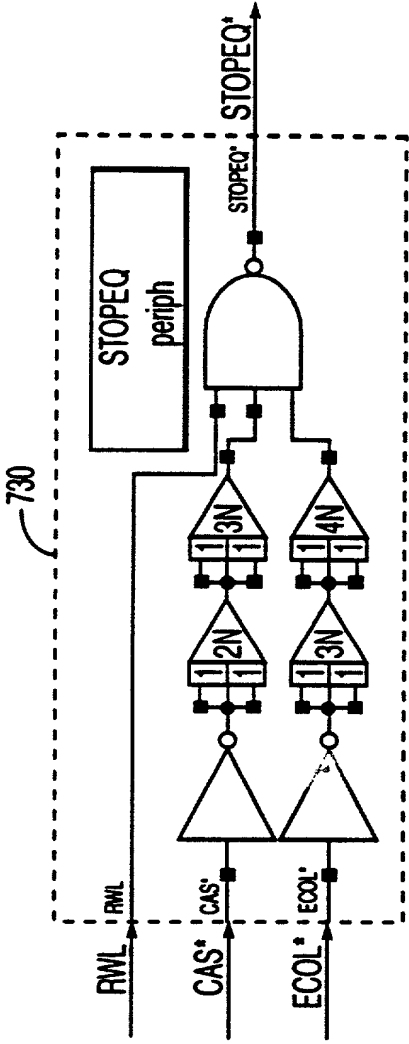


FIG. 45N

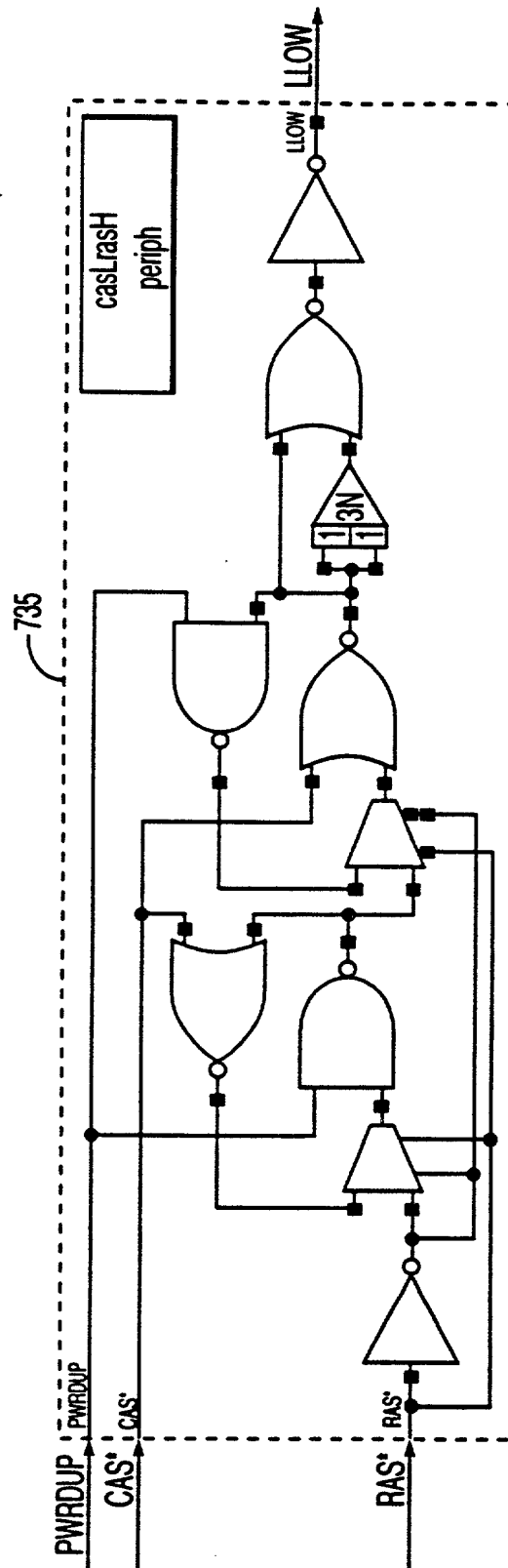


FIG. 450

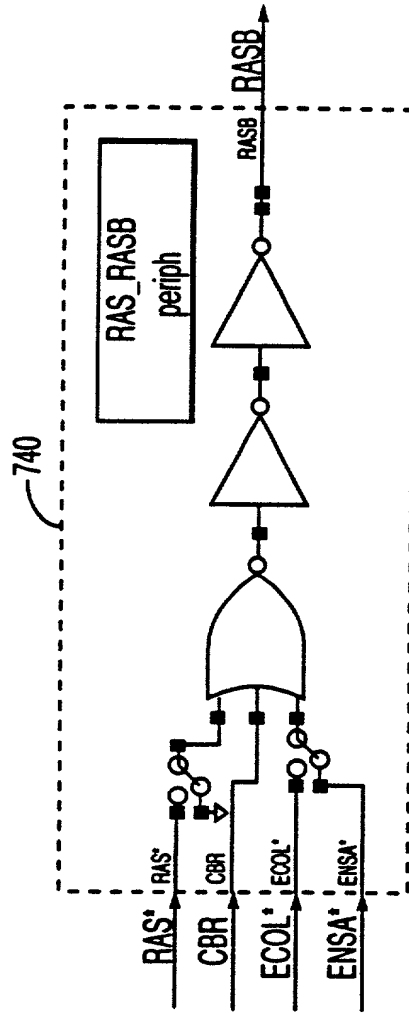


FIG. 45P

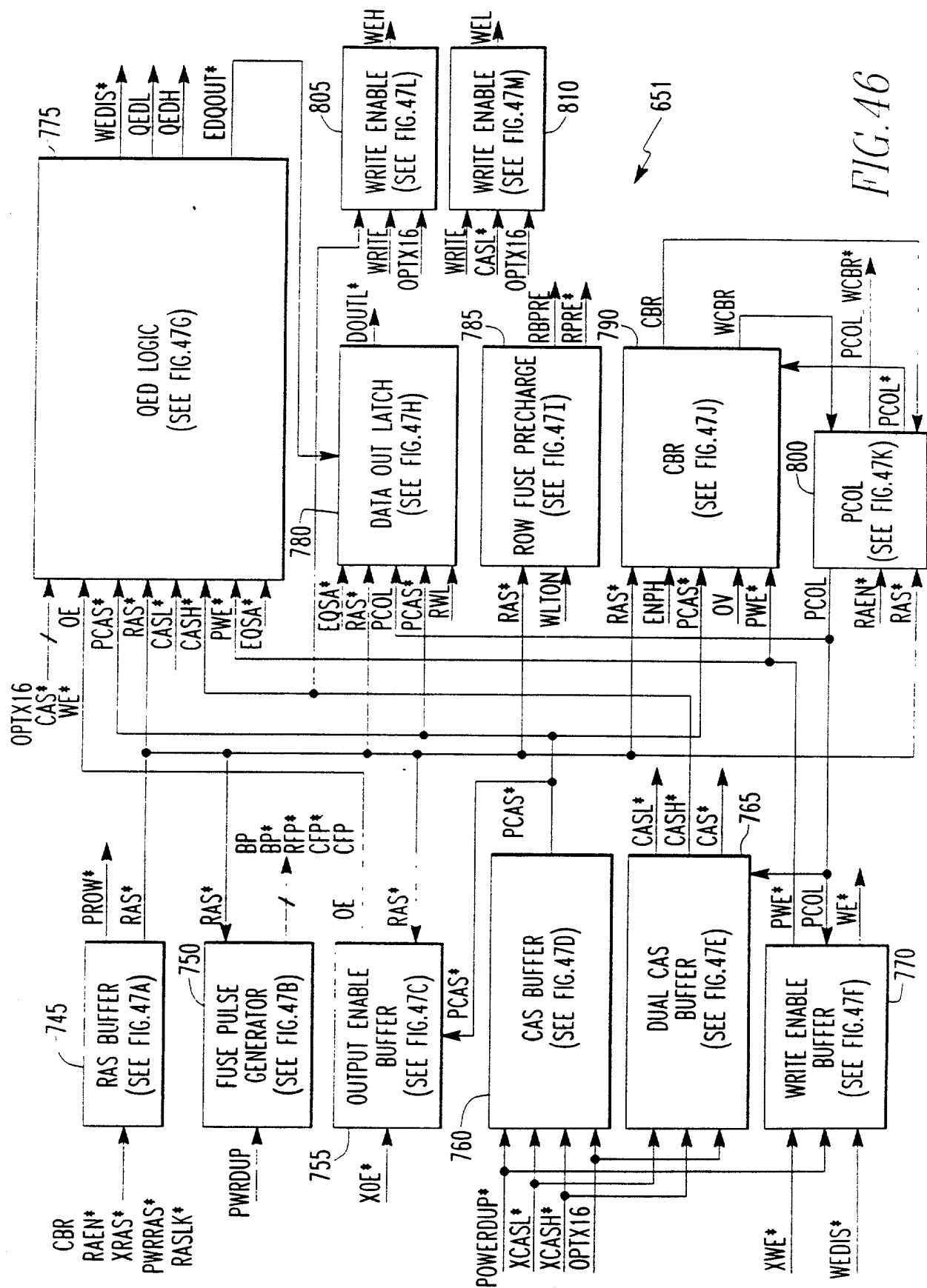


FIG. 46



FIG. 47A

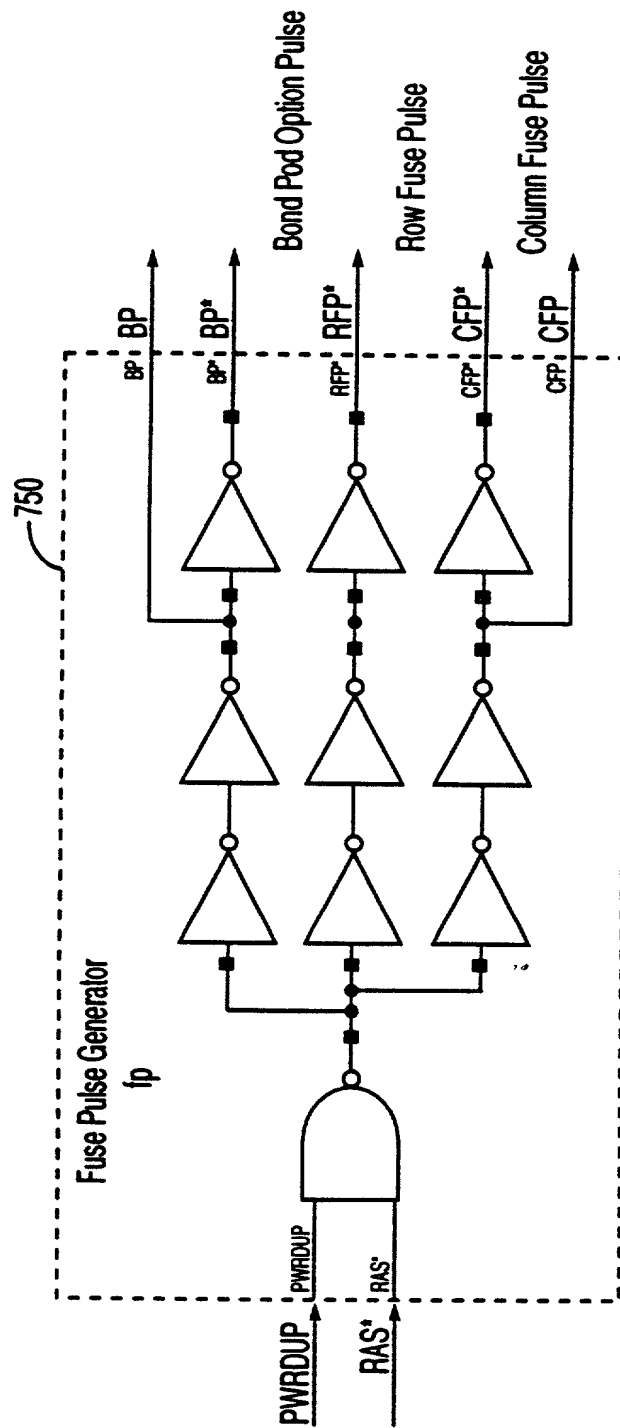


FIG. 47B

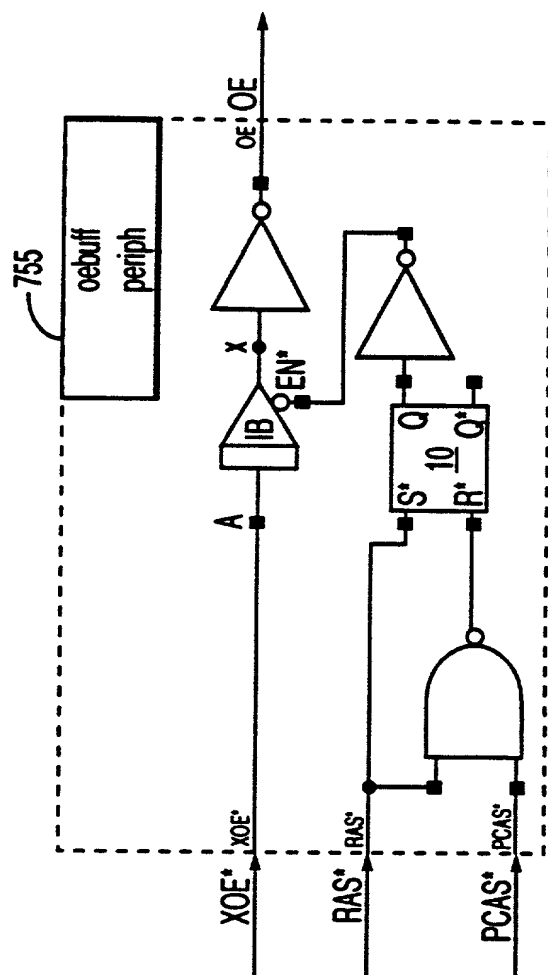


FIG. 47C

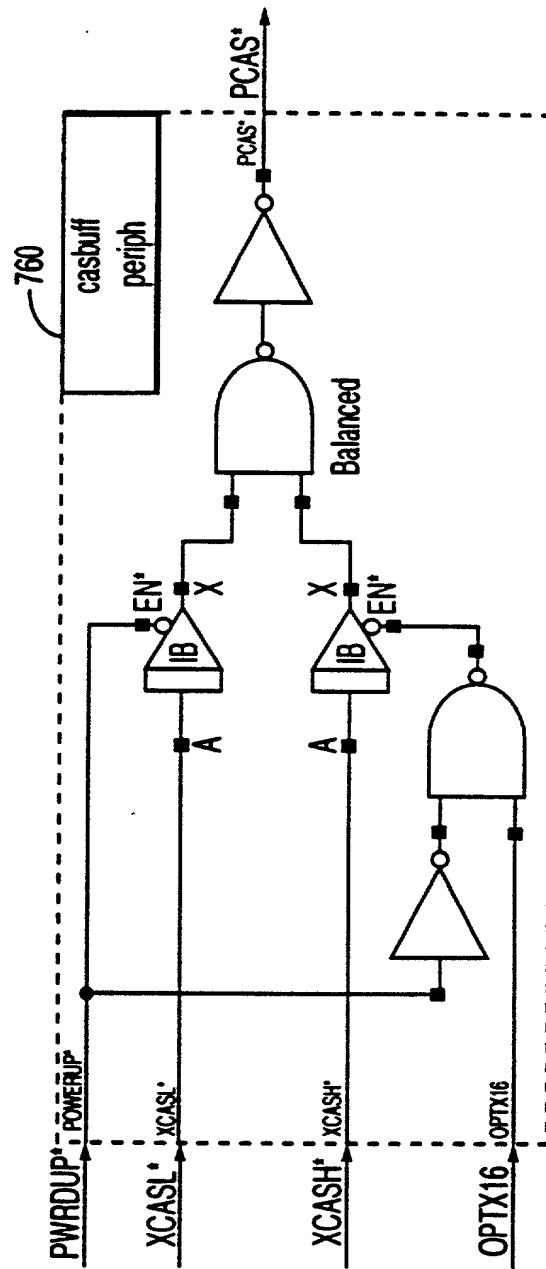


FIG. 47D

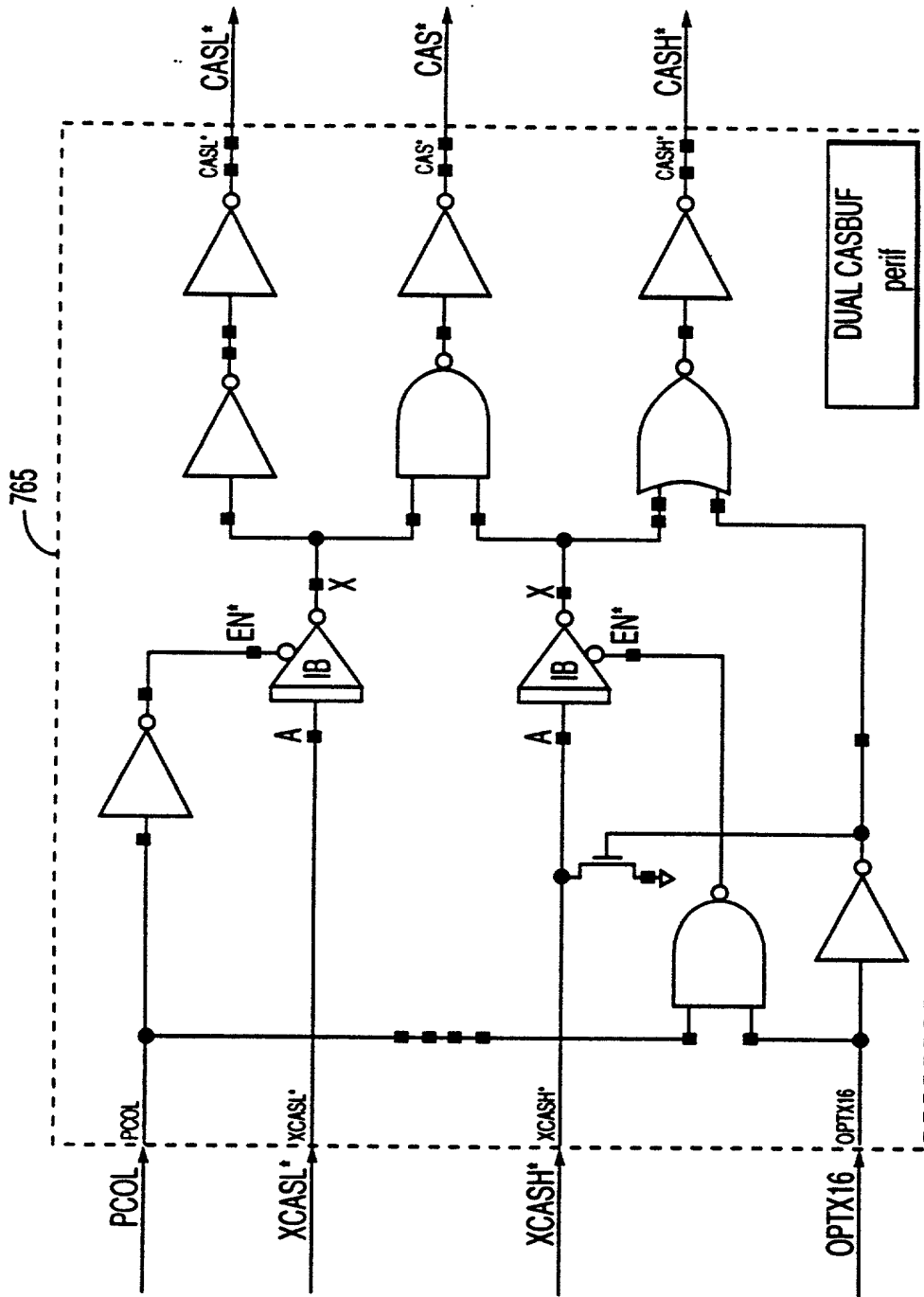


FIG. 47E

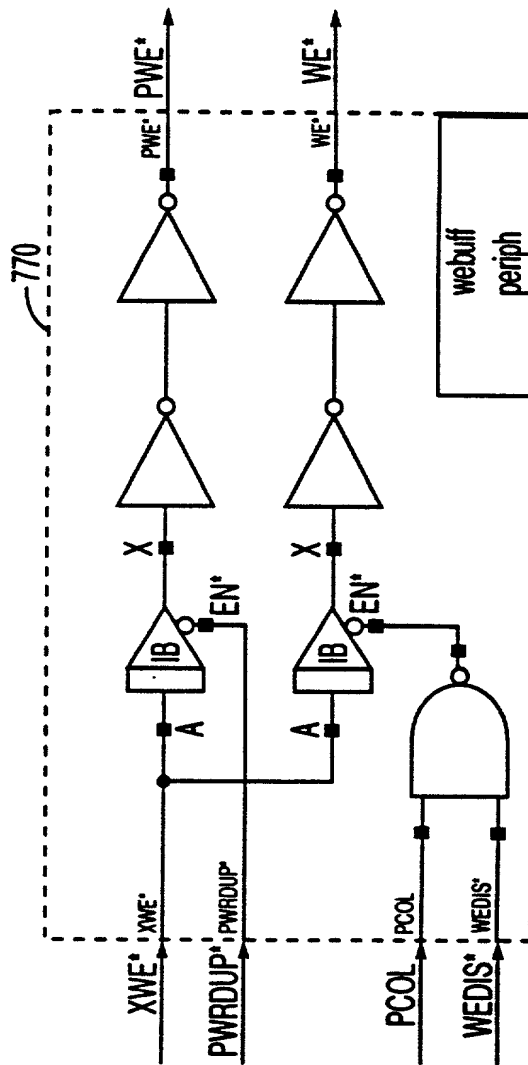


FIG. 47F



FIG. 47G

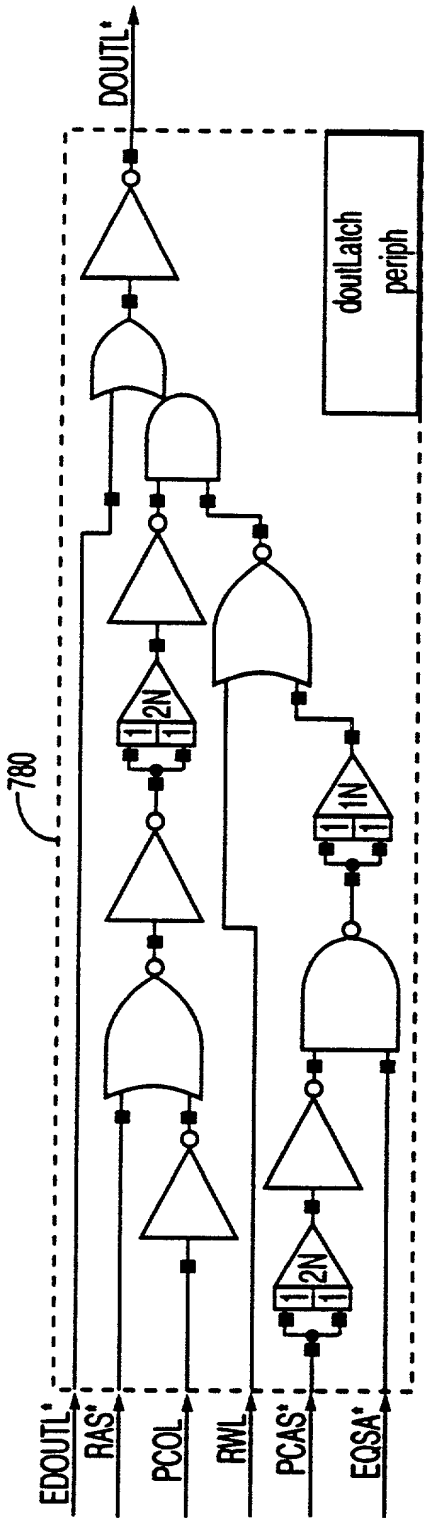


FIG. 47H

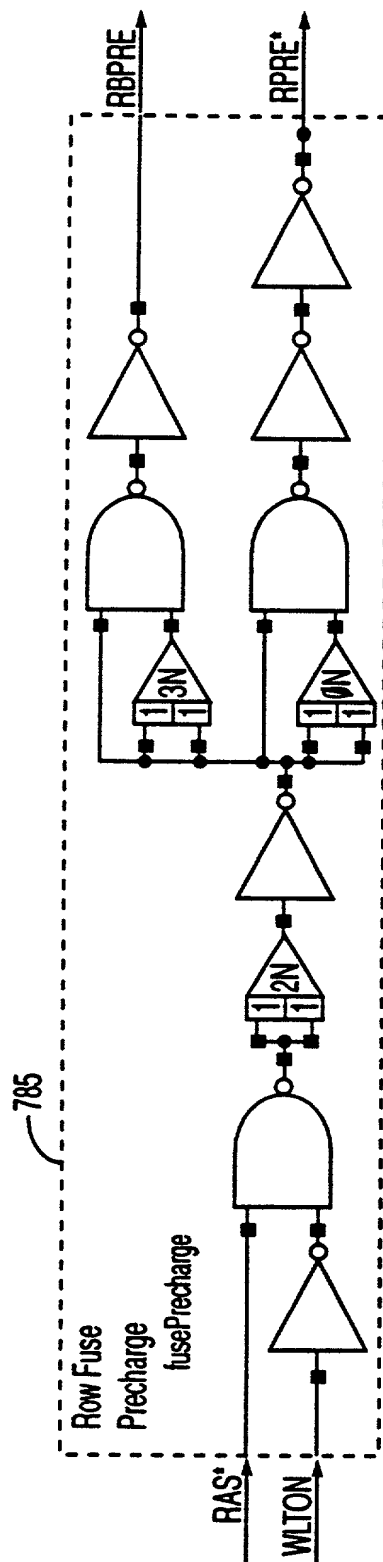


FIG. 471

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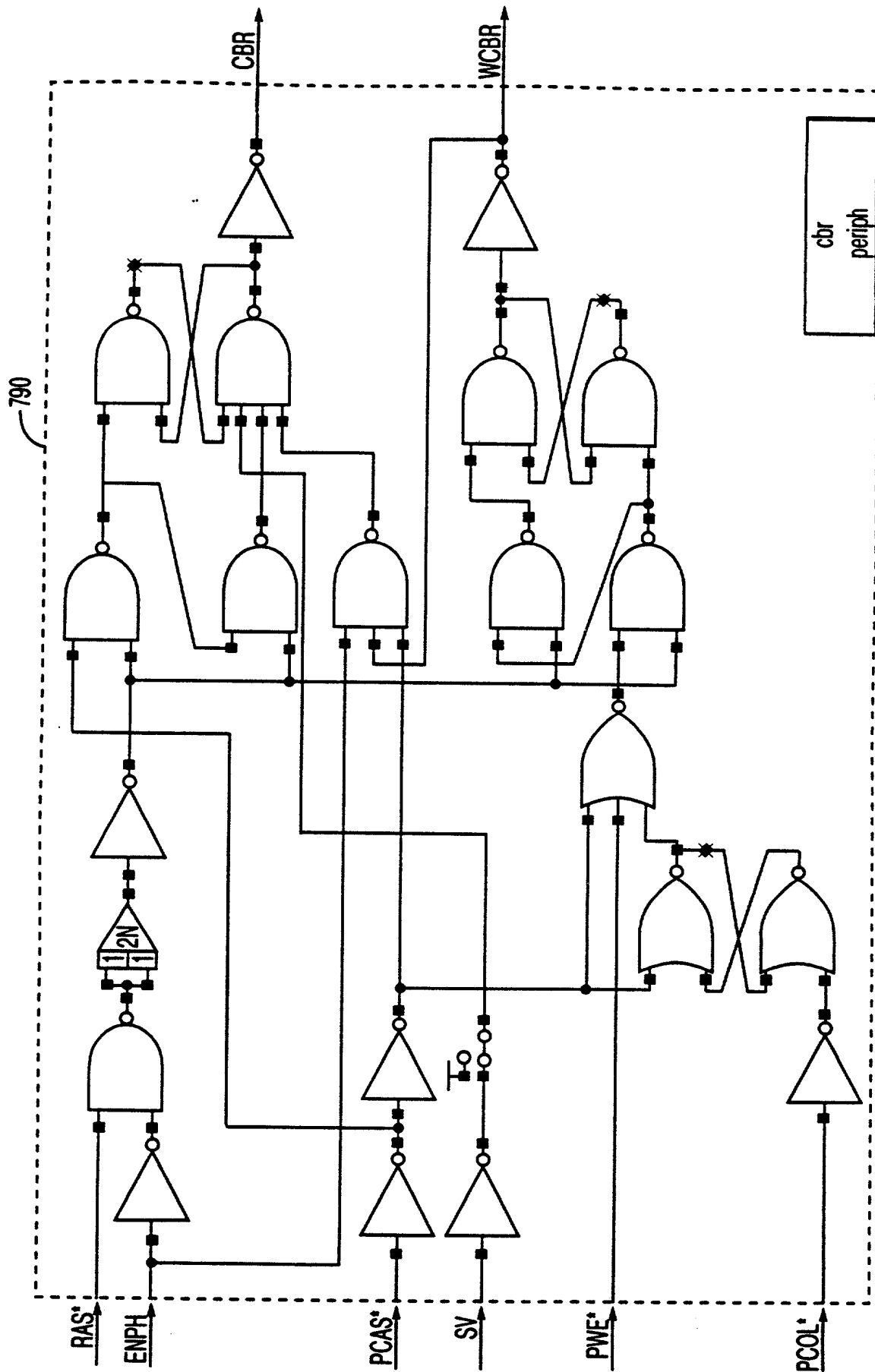


FIG. 47J

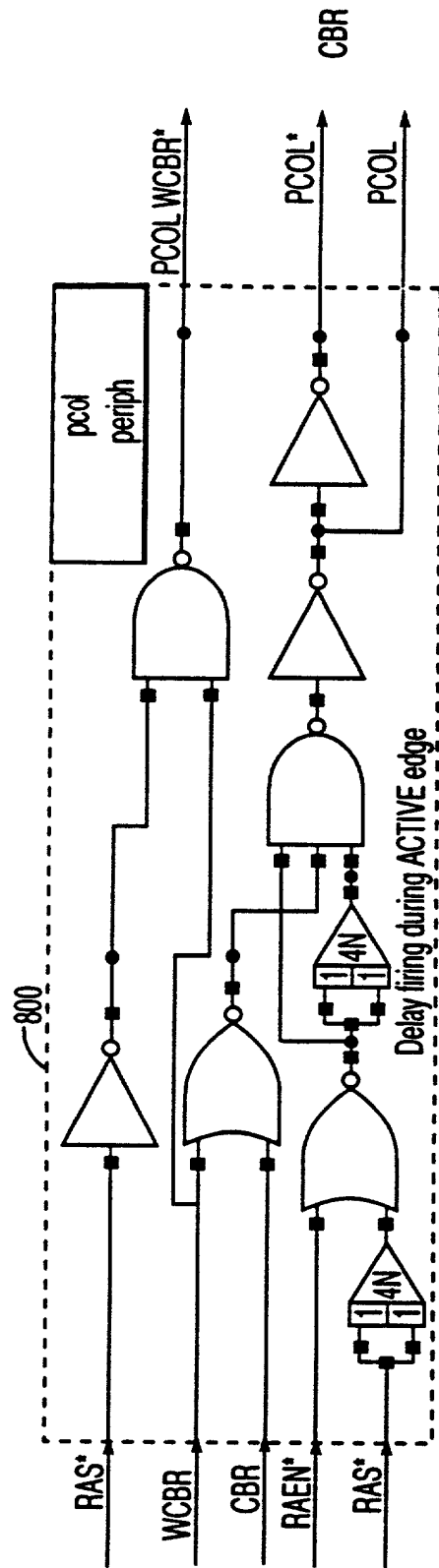


FIG. 47K



FIG. 47L



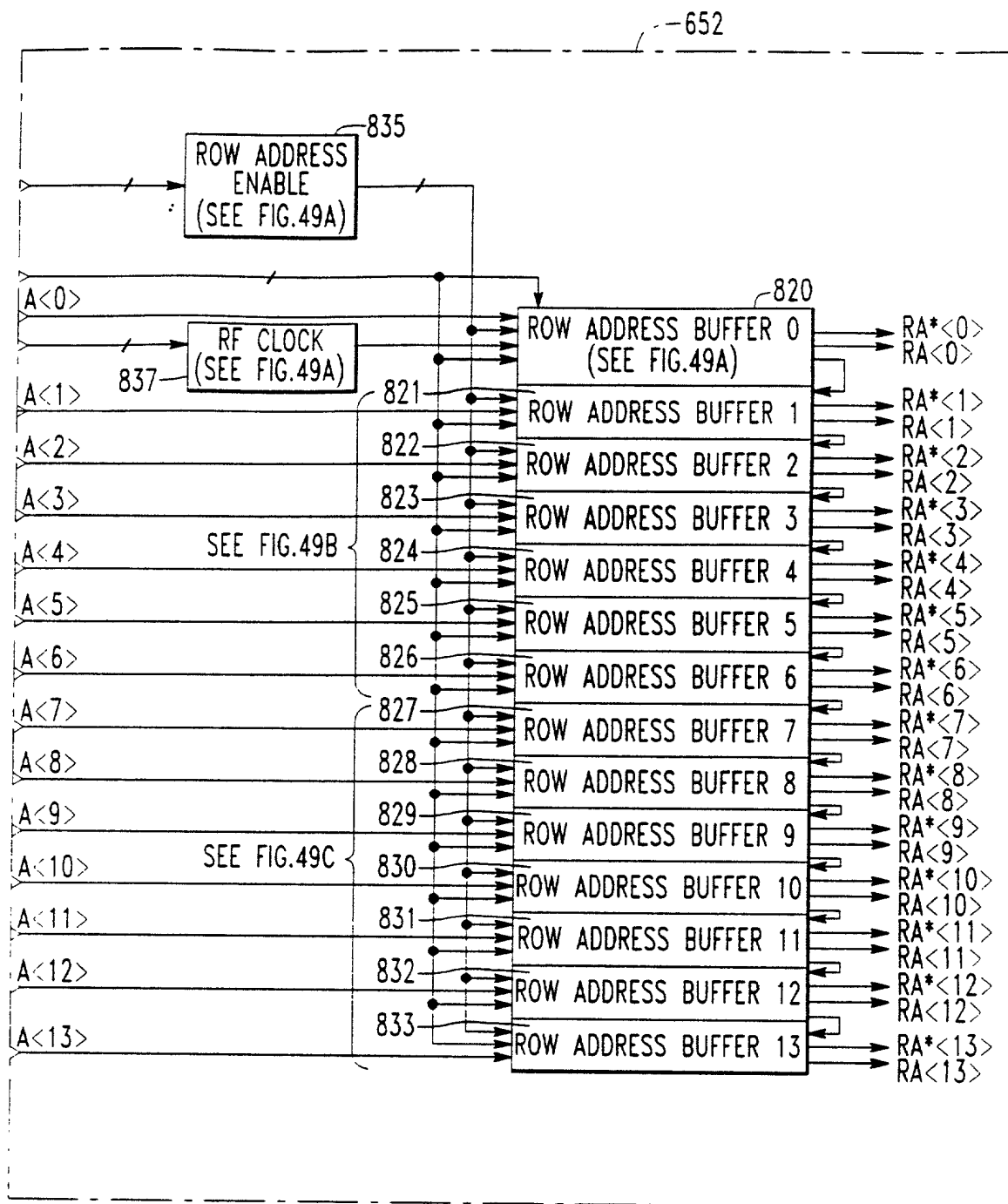


FIG. 48A

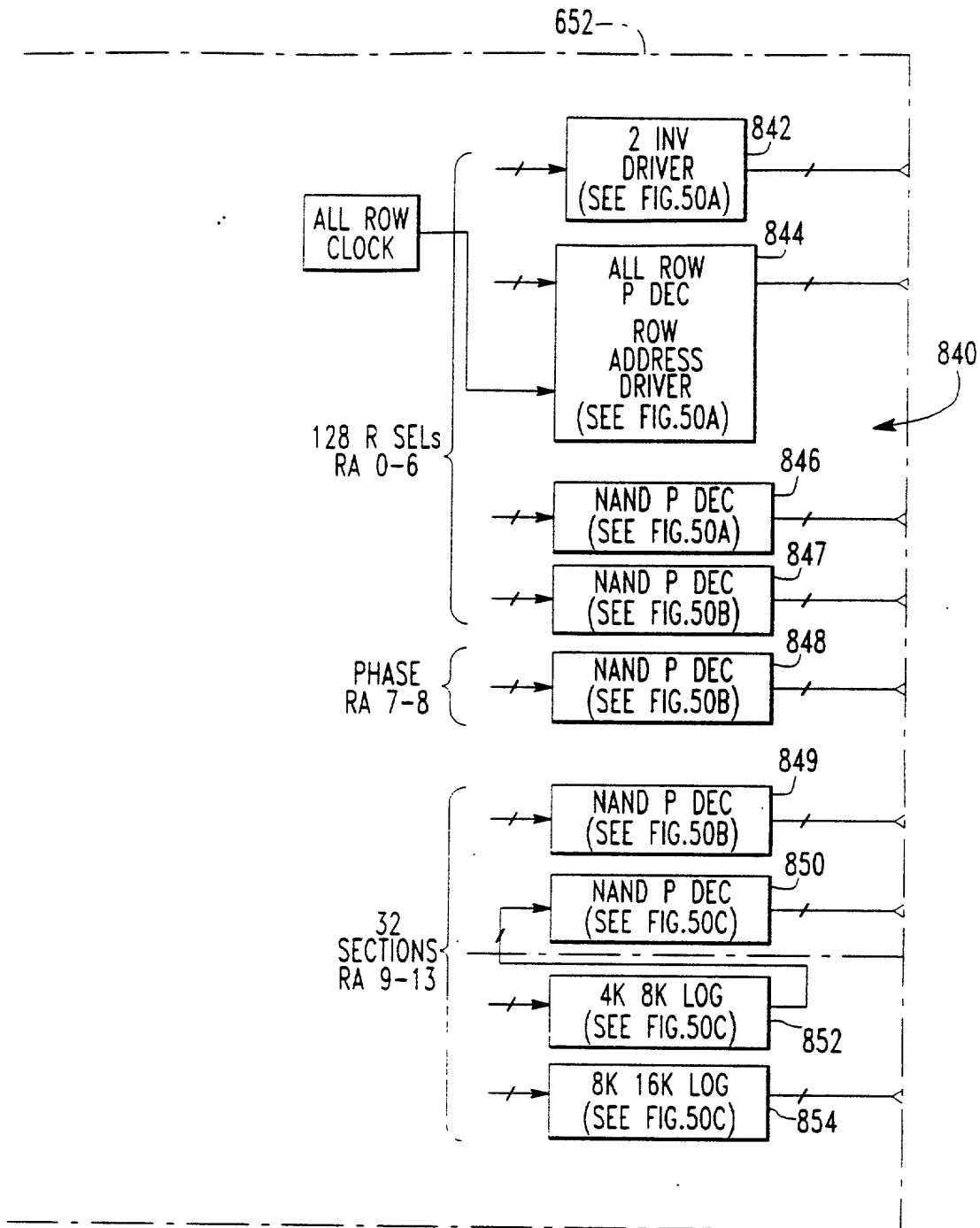
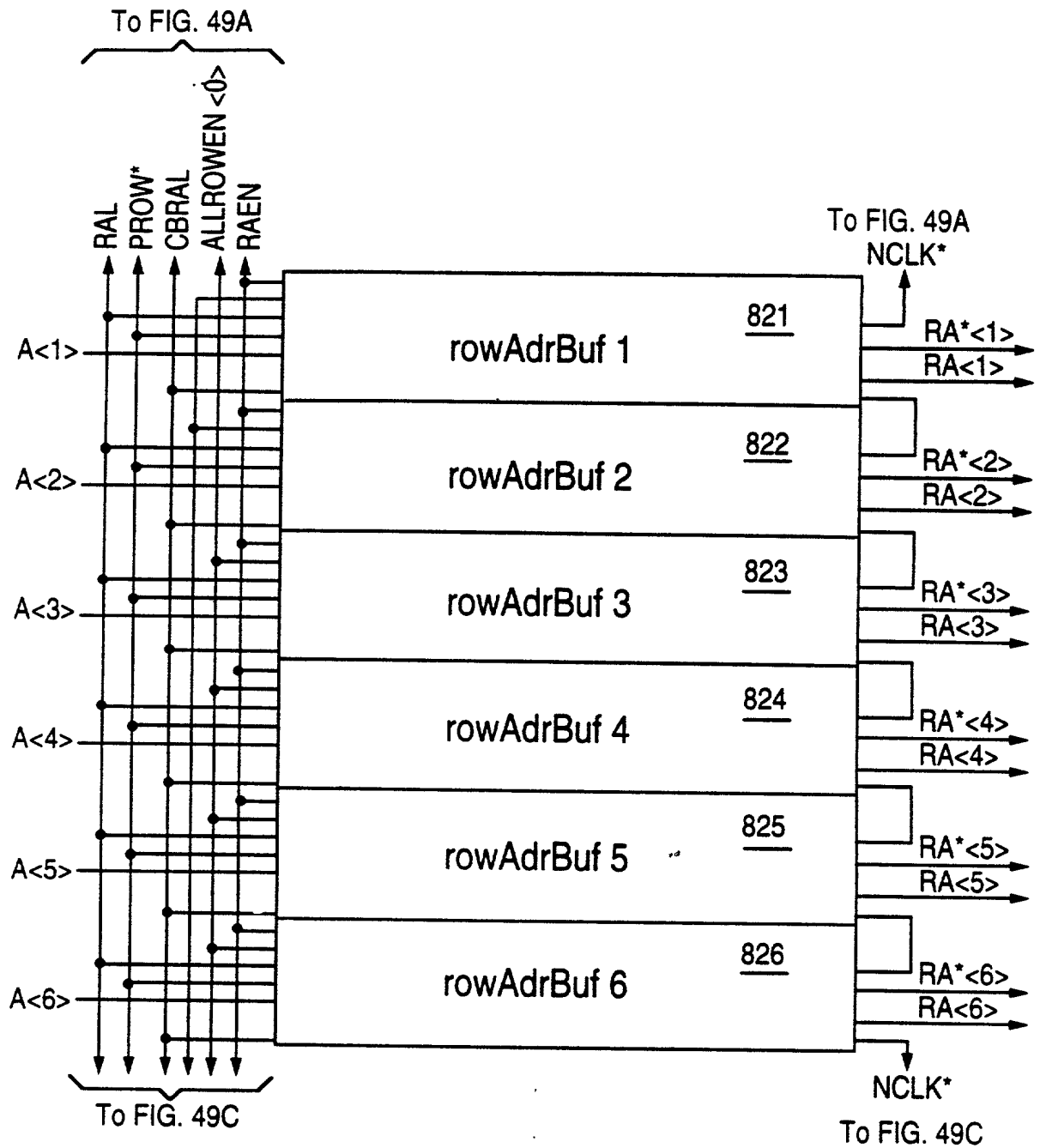
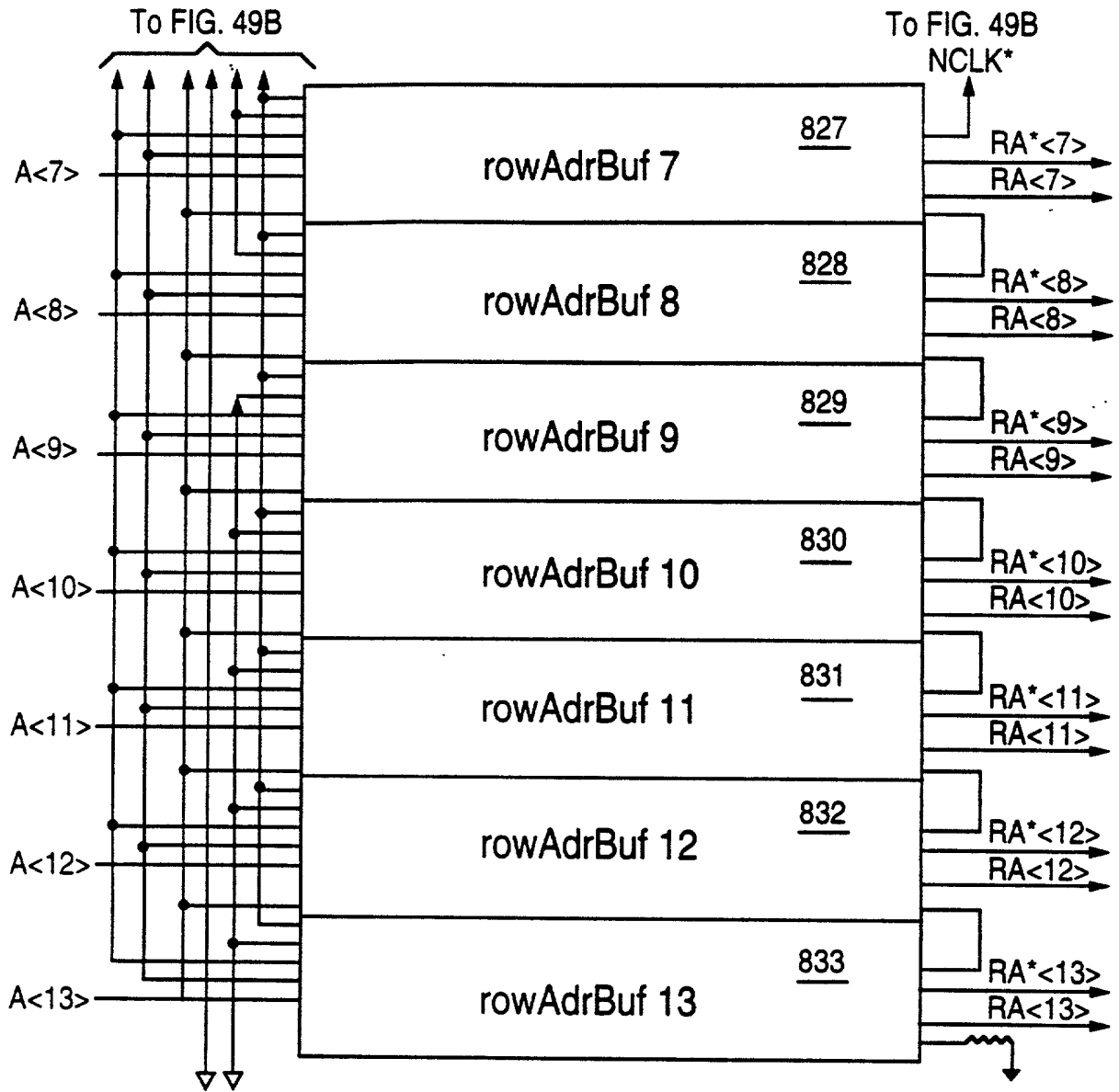


FIG. 48B



**FIG. 49B**

**FIG. 49C**

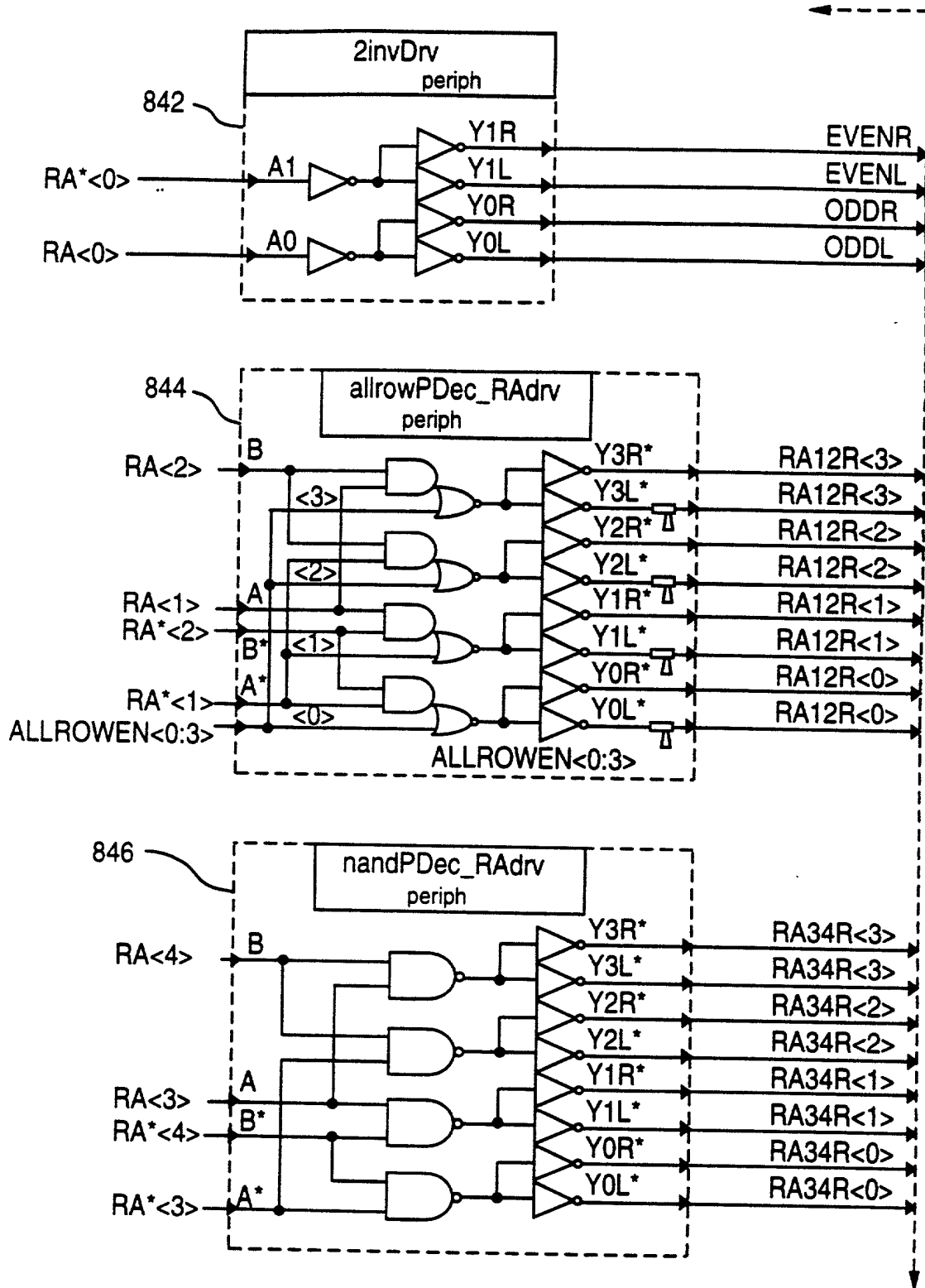
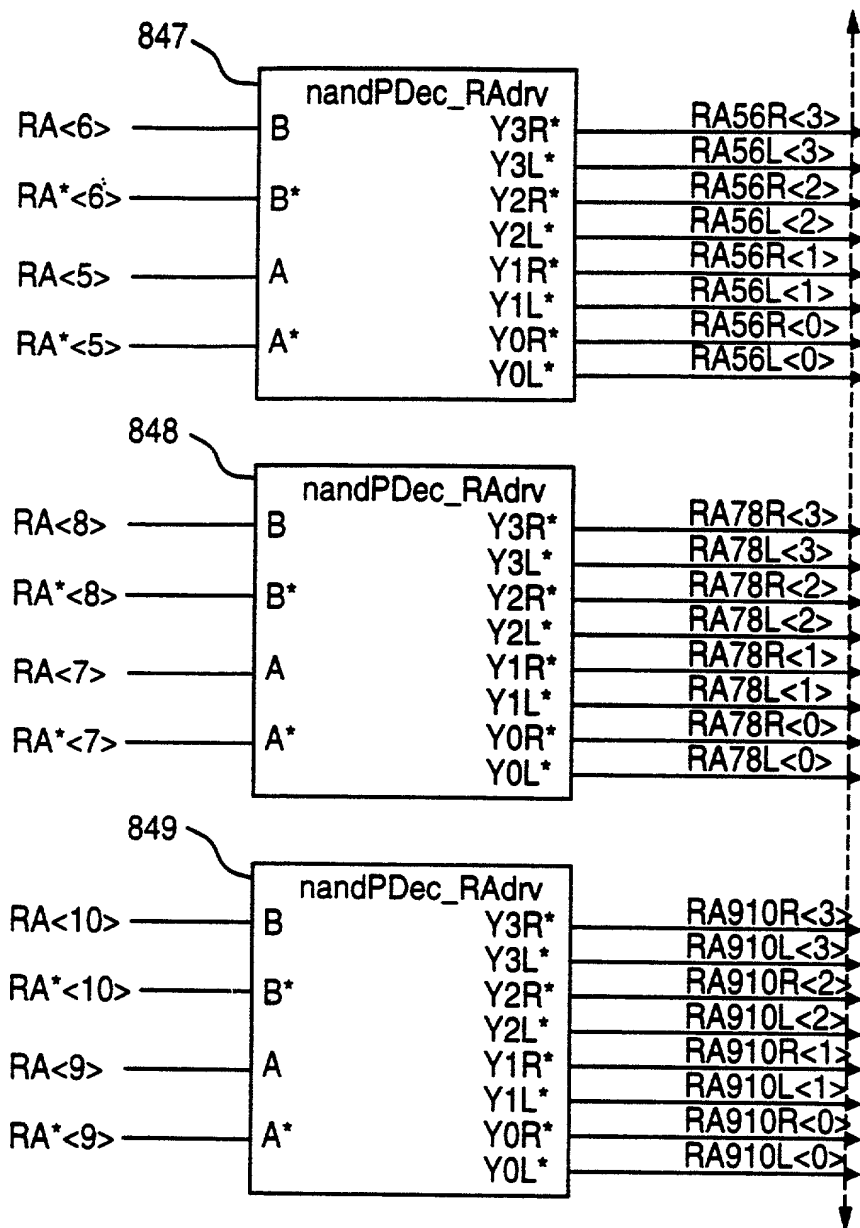


FIG. 50A

**FIG. 50B**

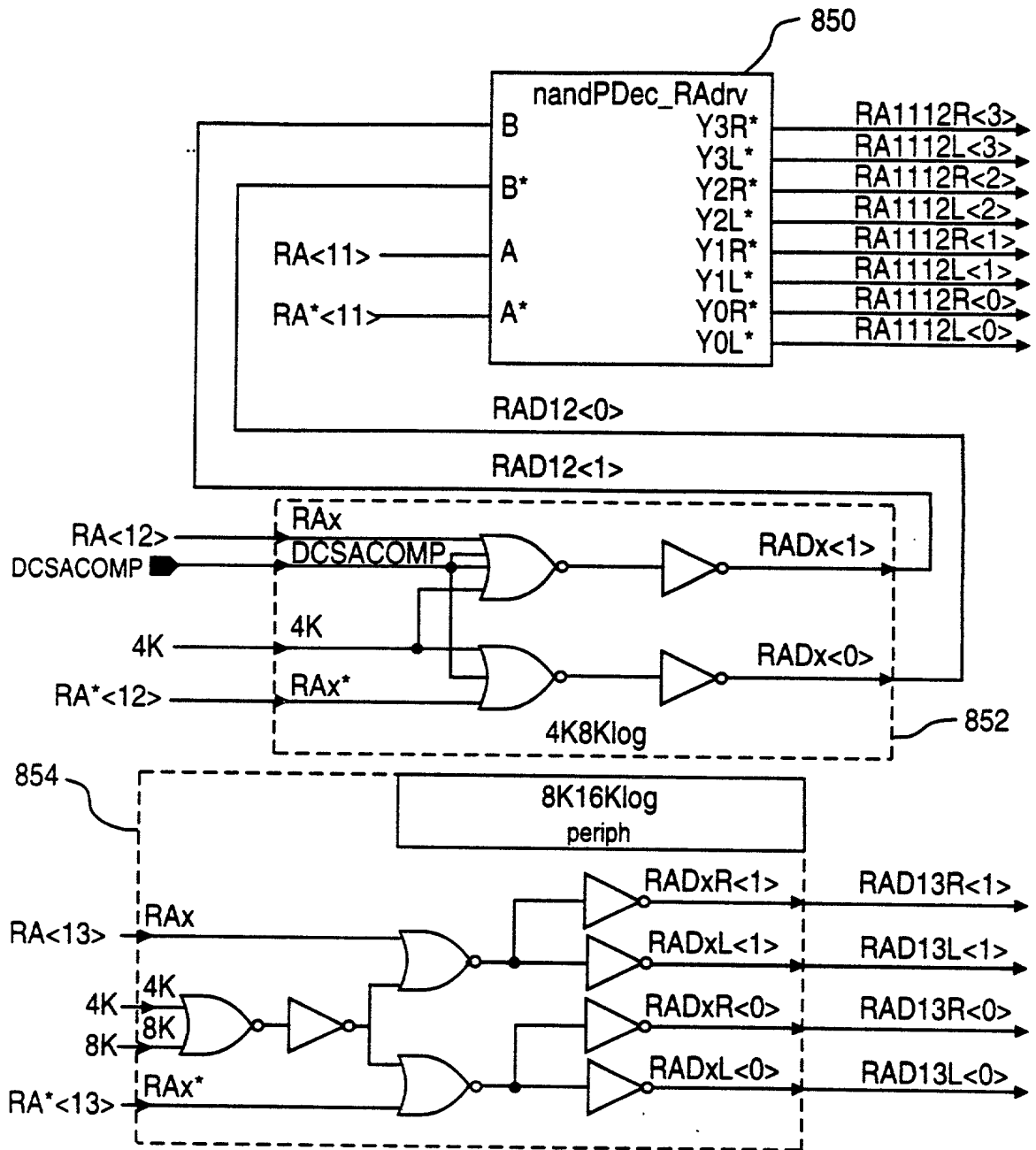


FIG. 50C

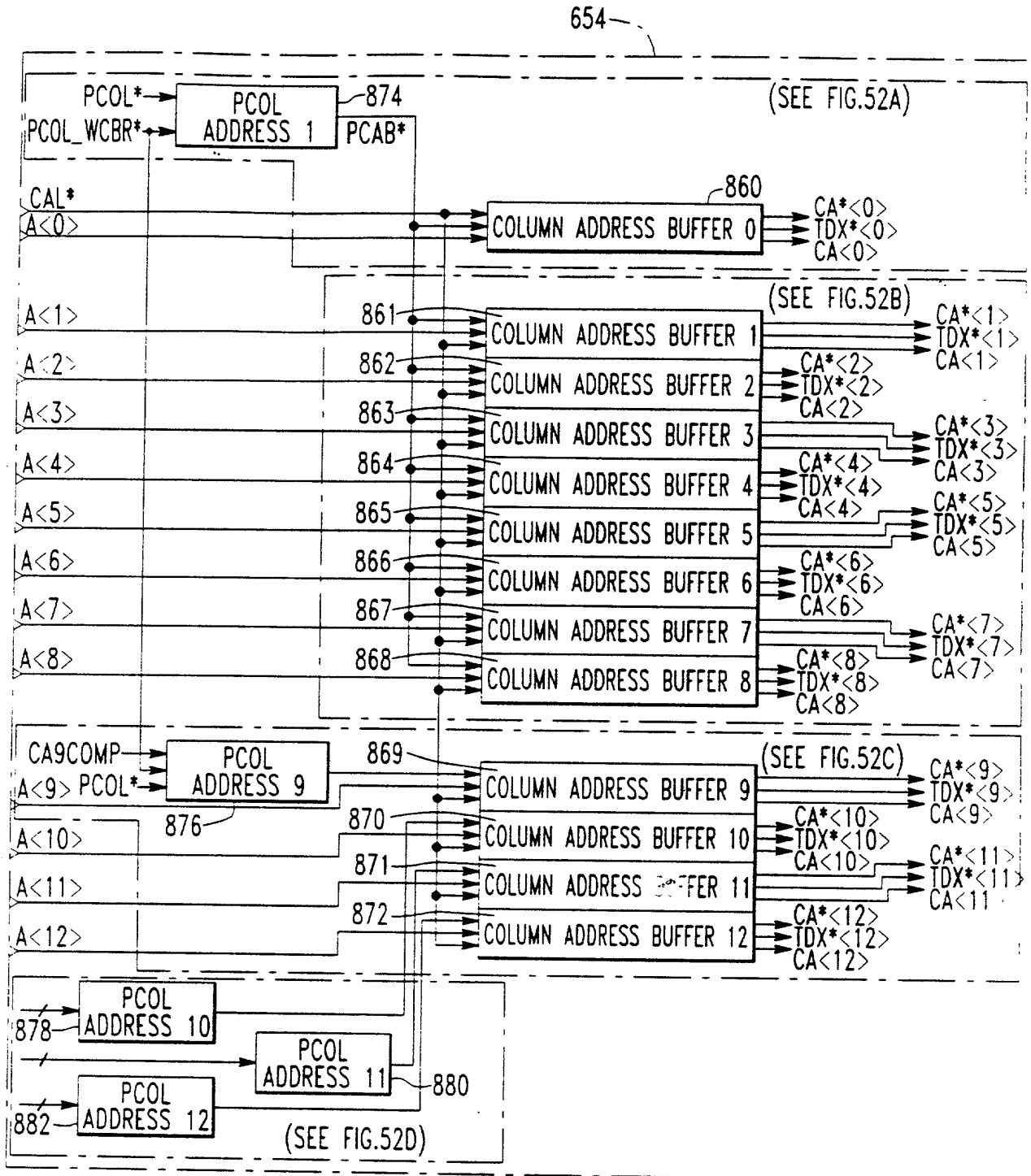


FIG. 51A

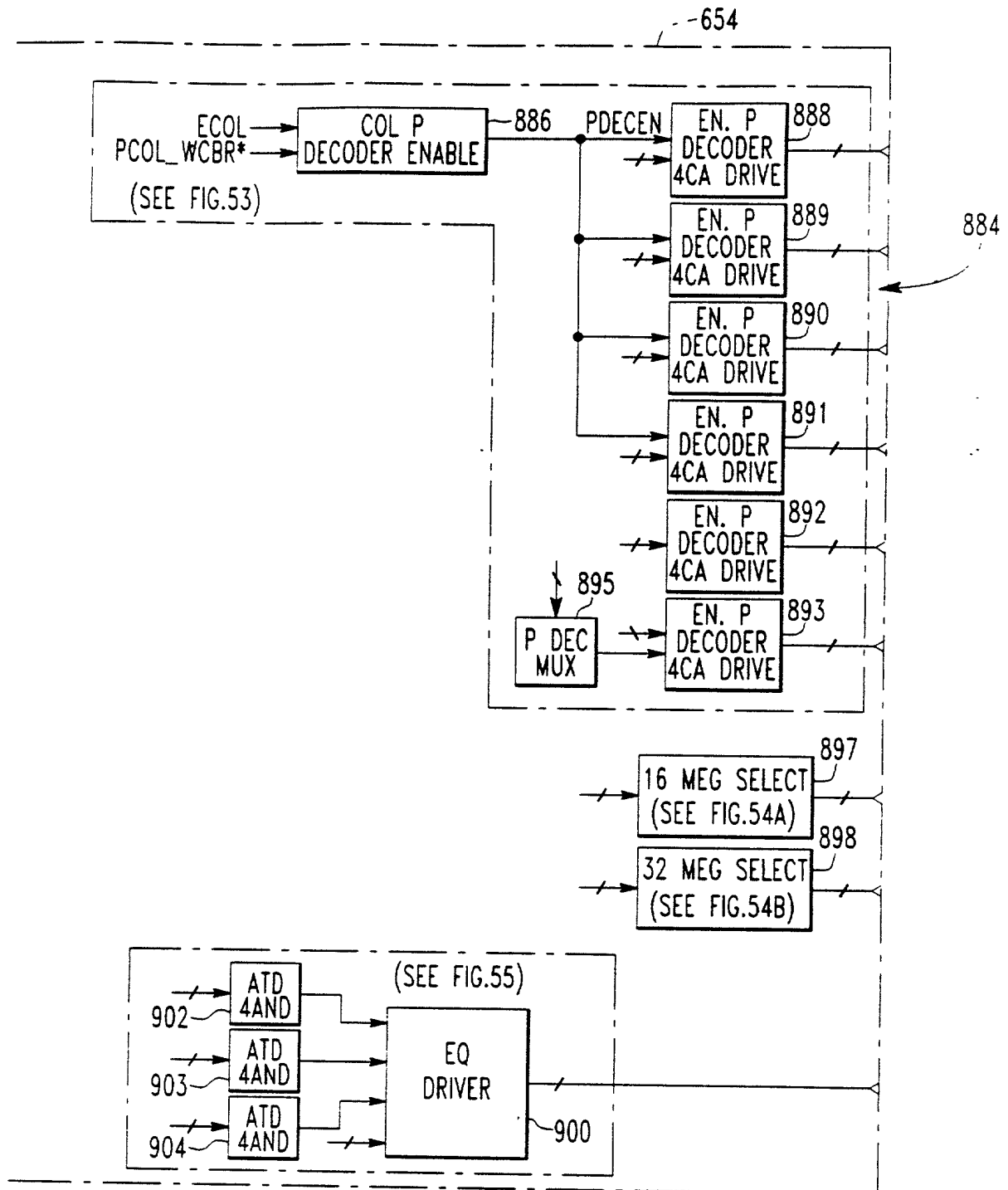


FIG. 51B

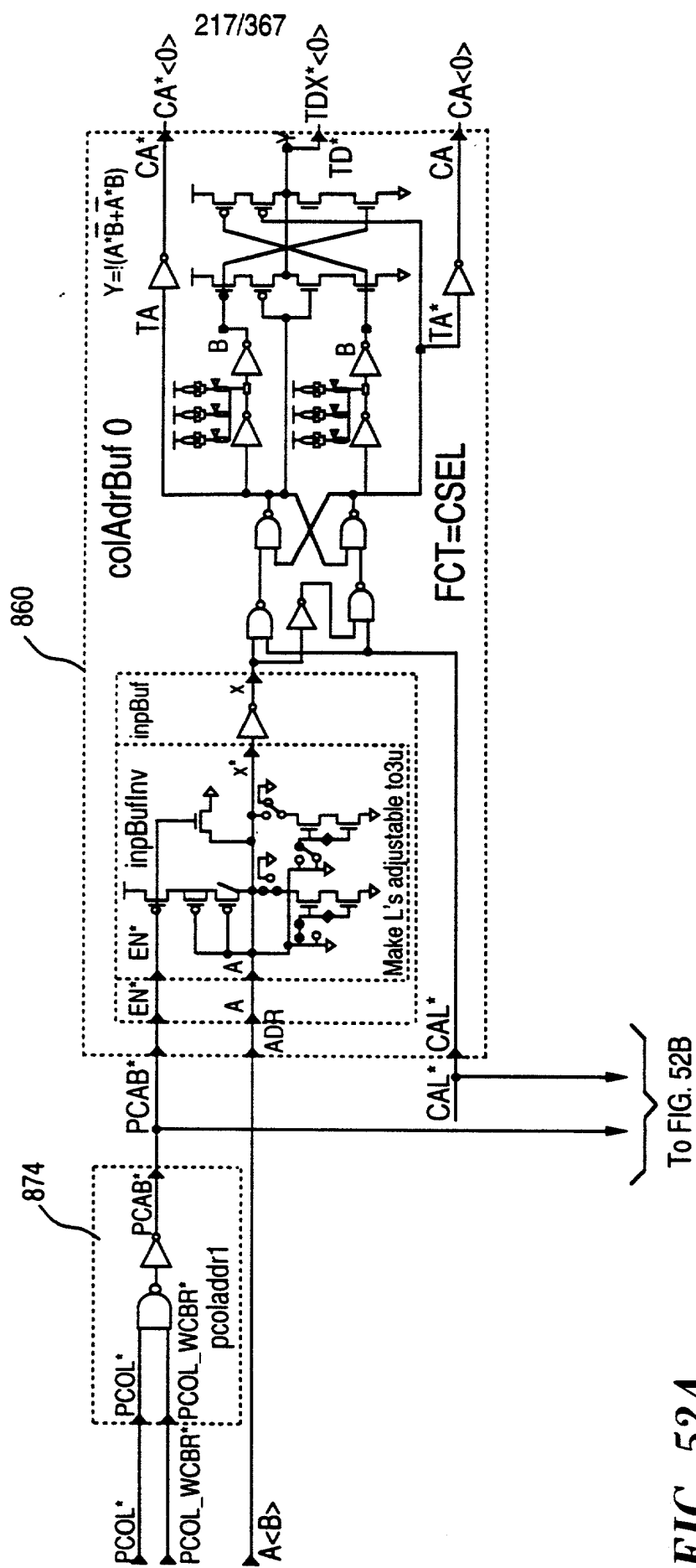


FIG. 52A

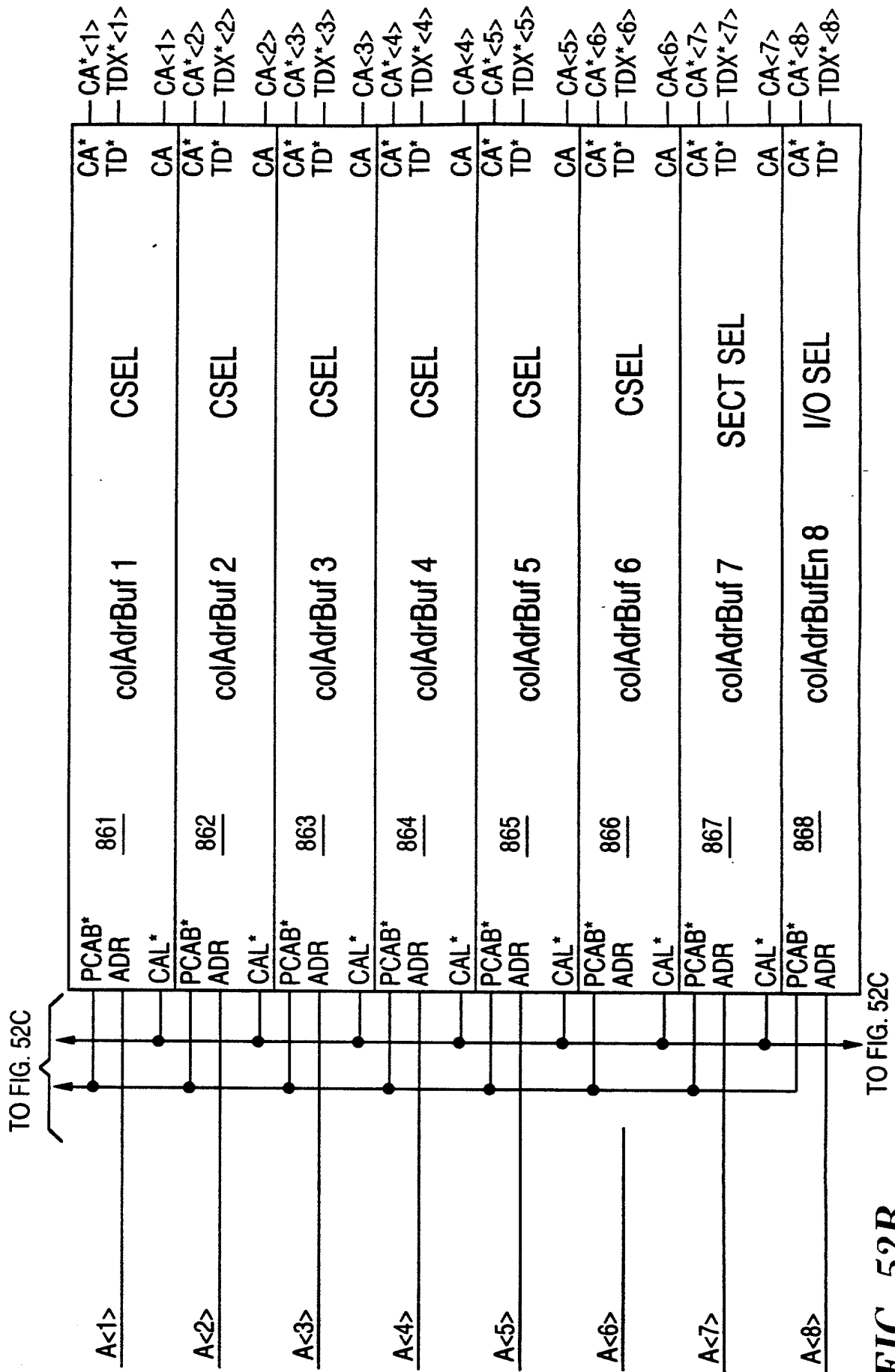


FIG. 52B

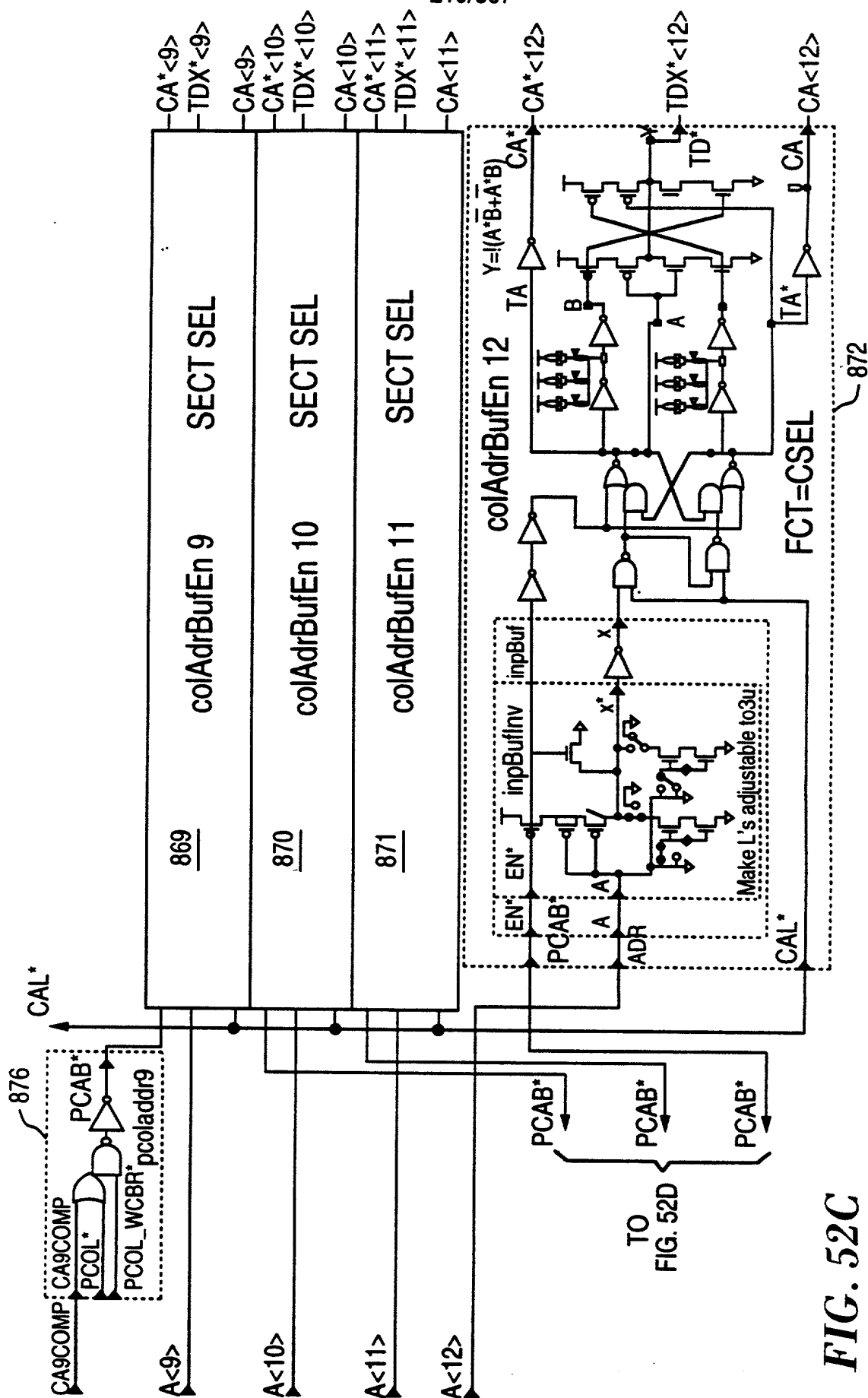


FIG. 52C

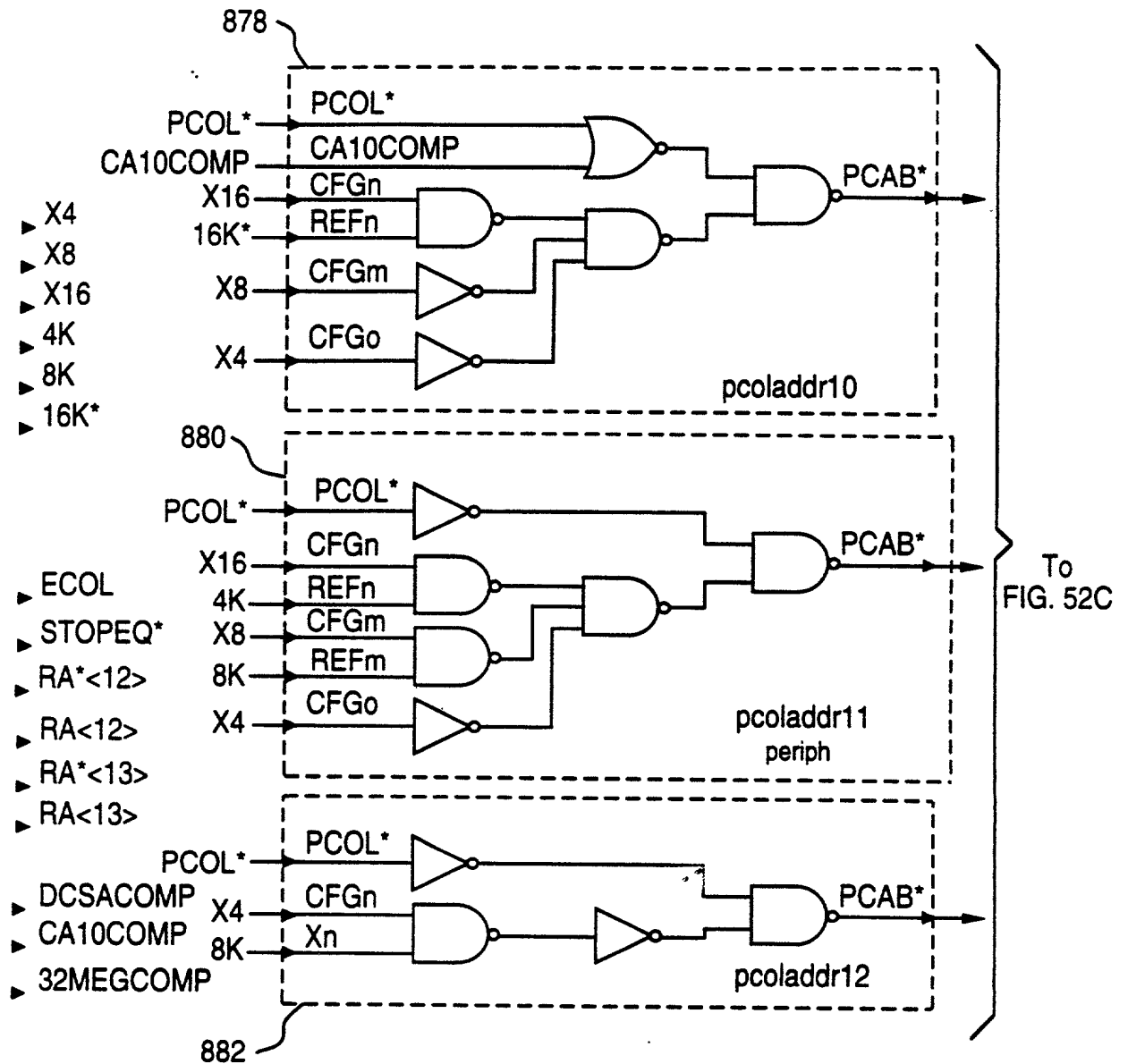


FIG. 52D

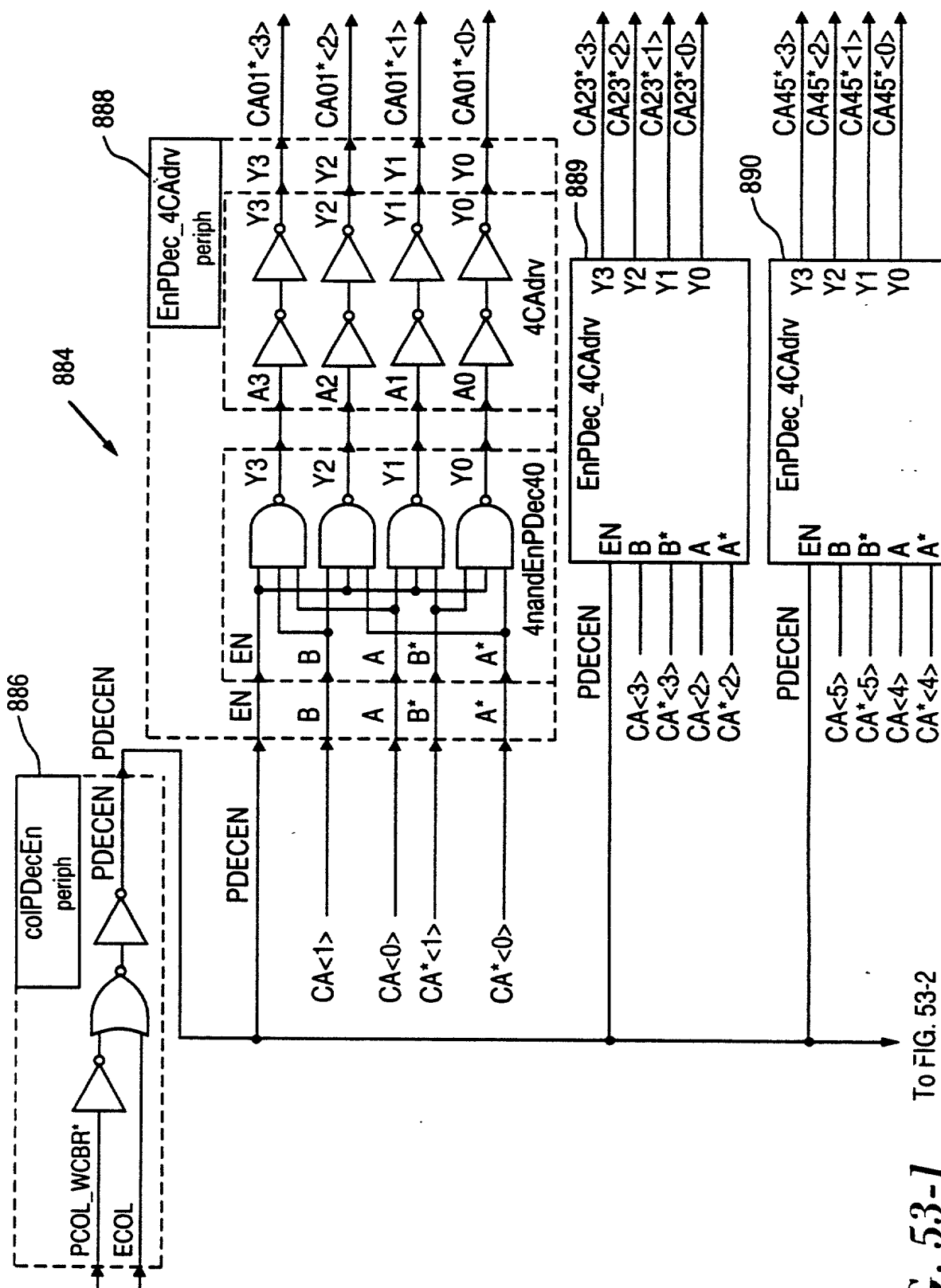


FIG. 53-1 To FIG. 53-2

To FIG. 53-1

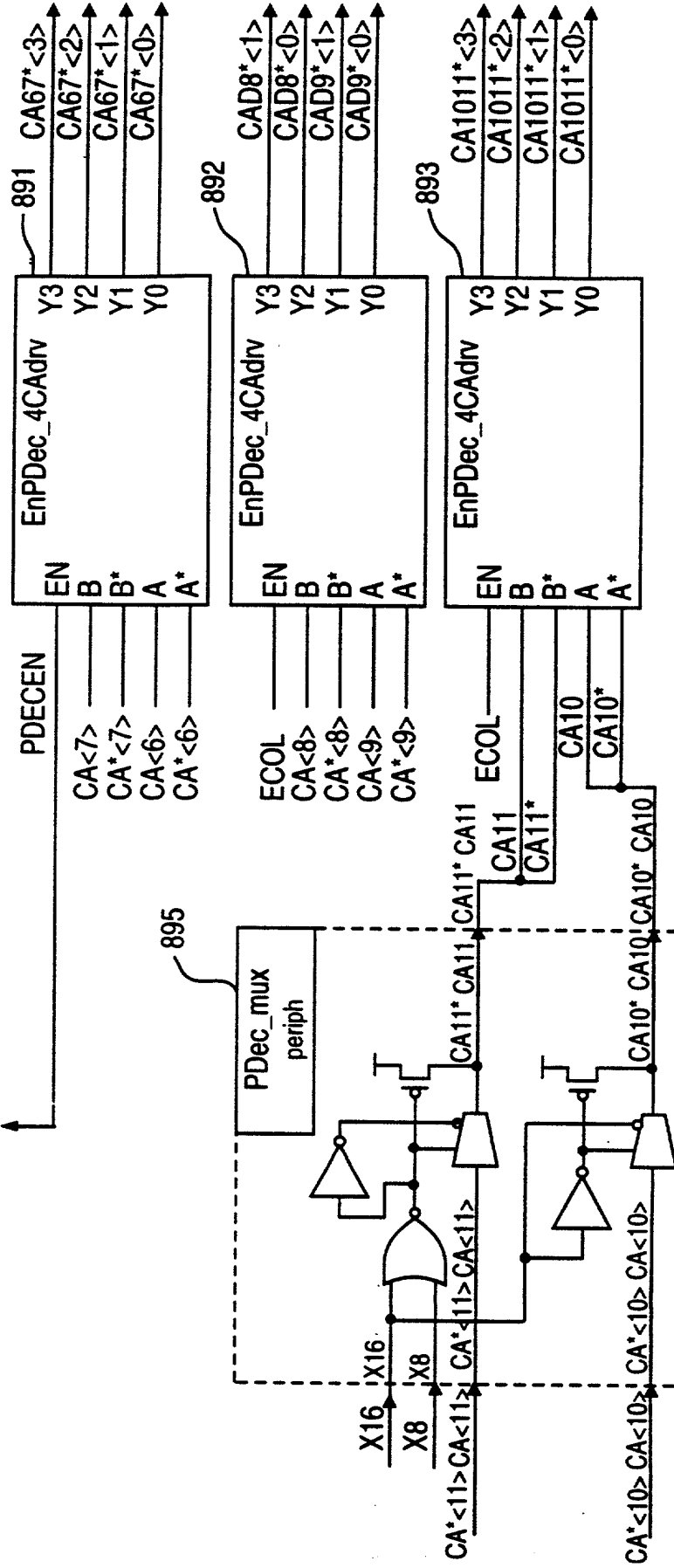


FIG. 53-2

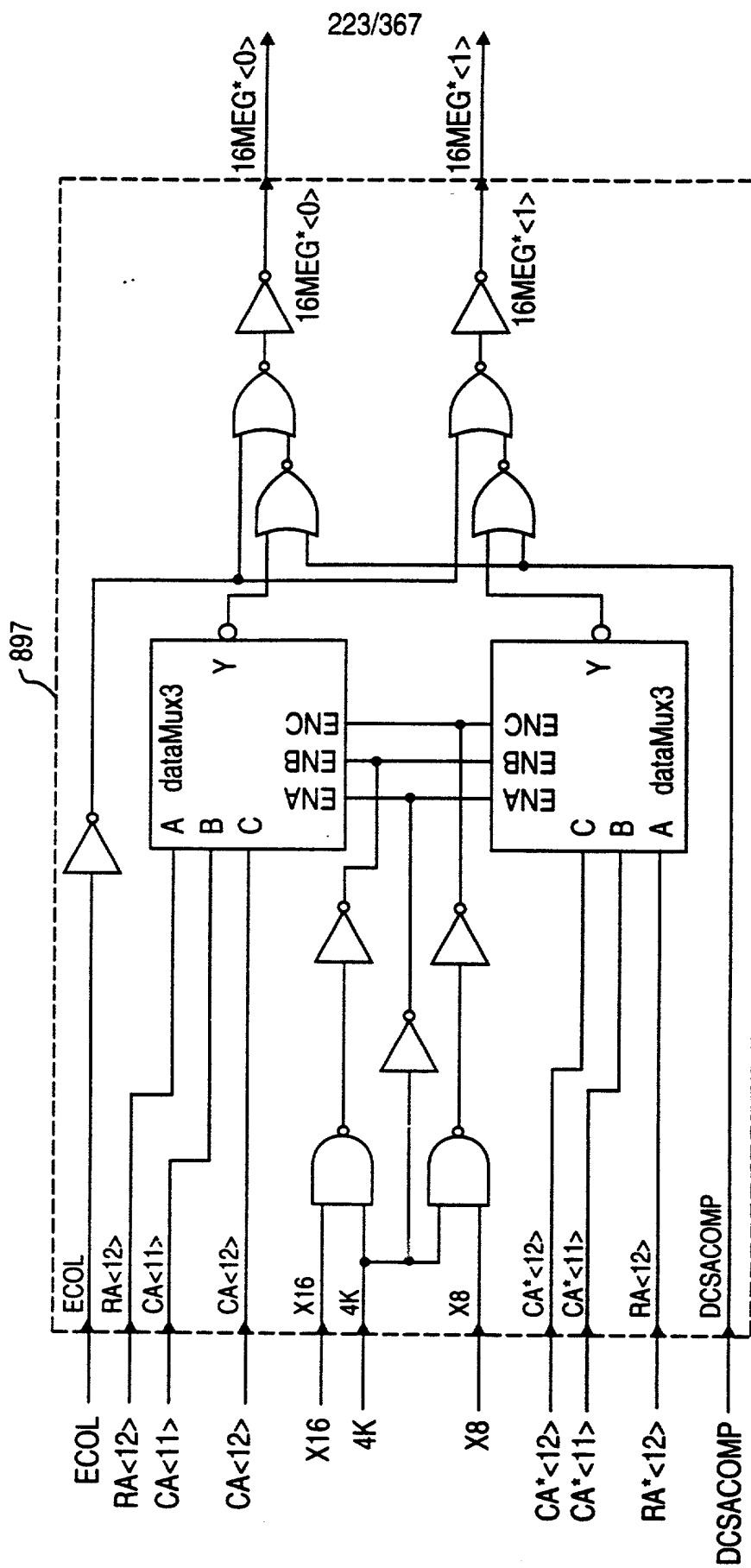


FIG. 54A

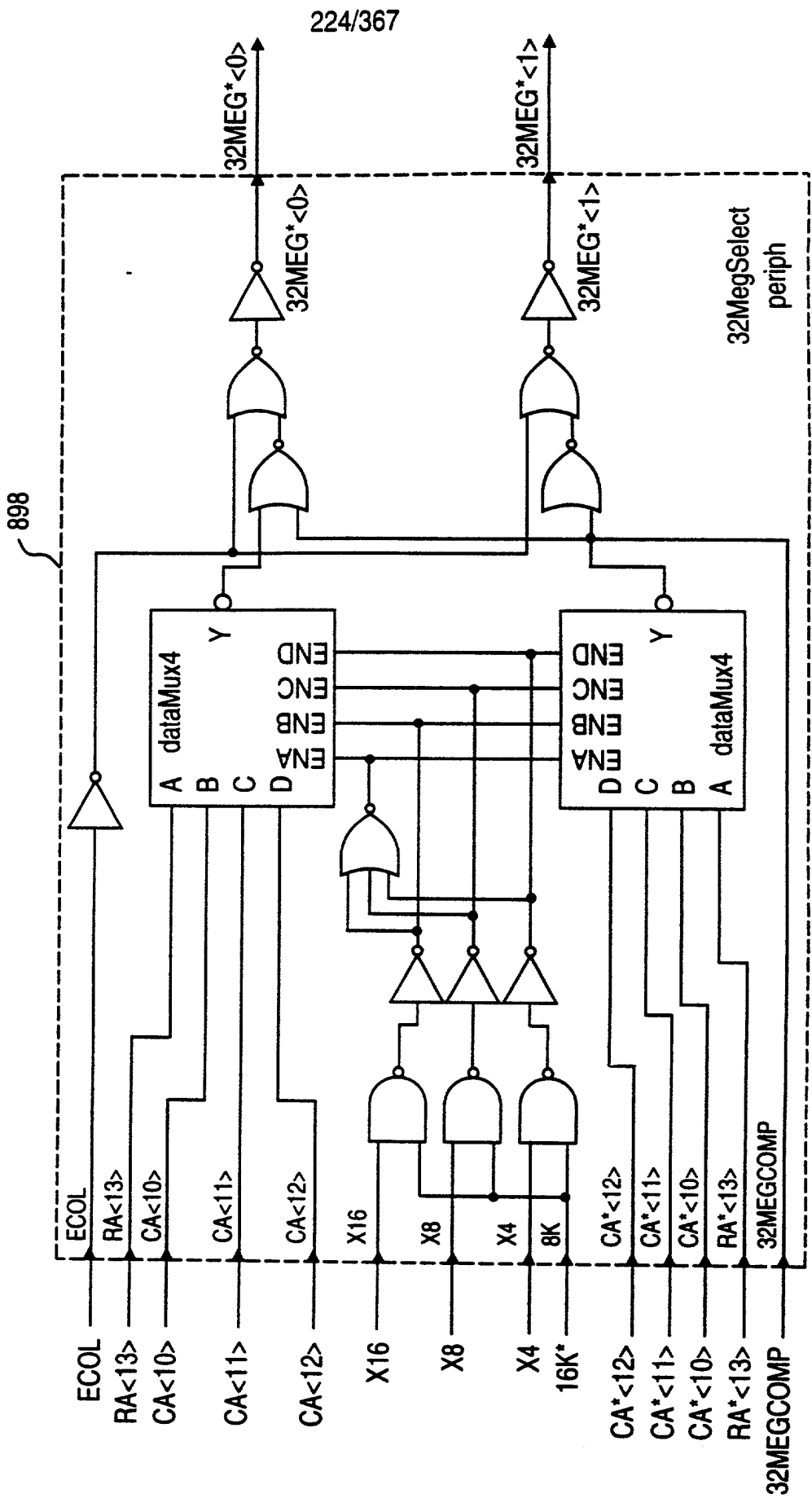


FIG. 54B

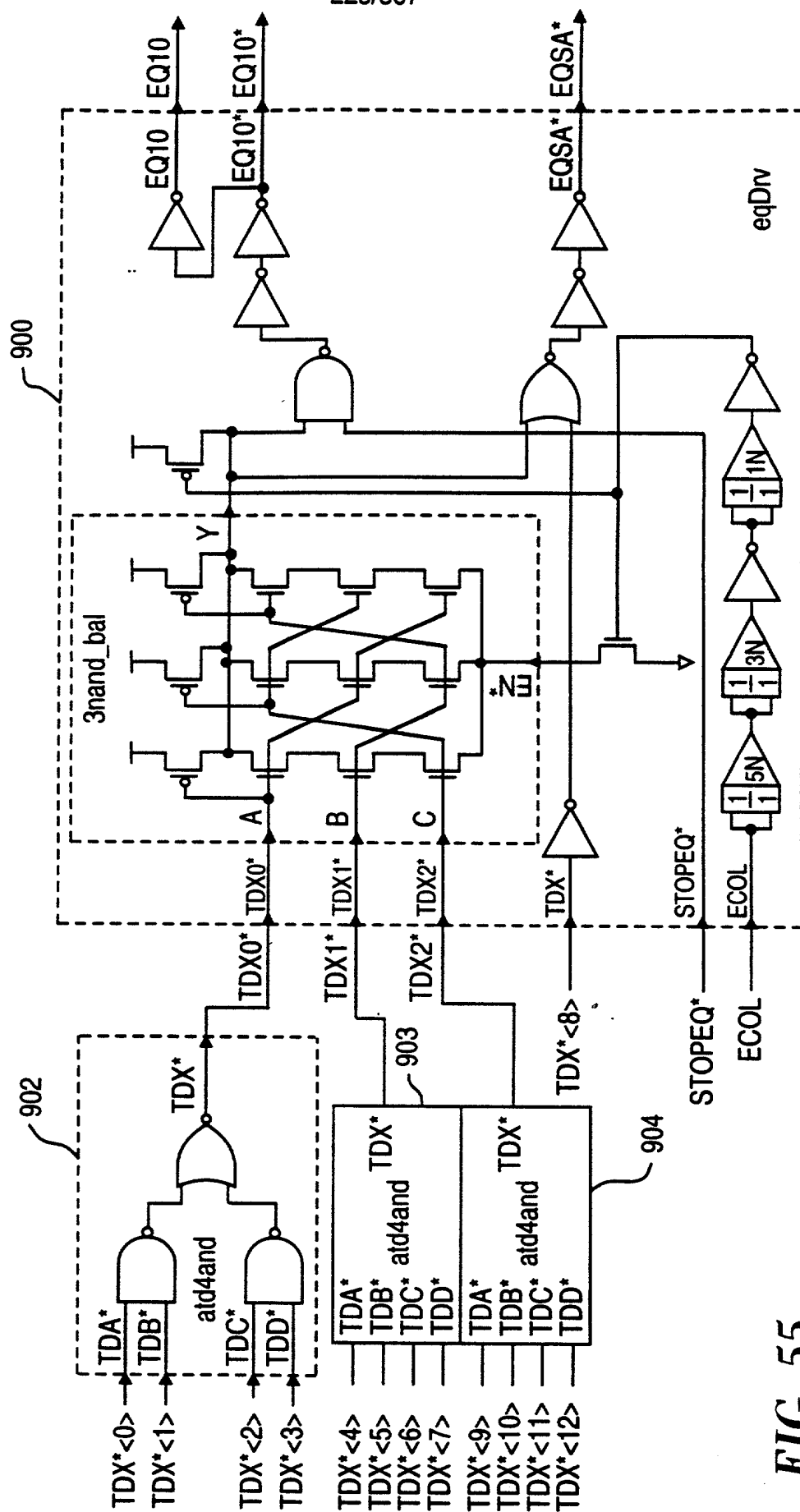


FIG. 55

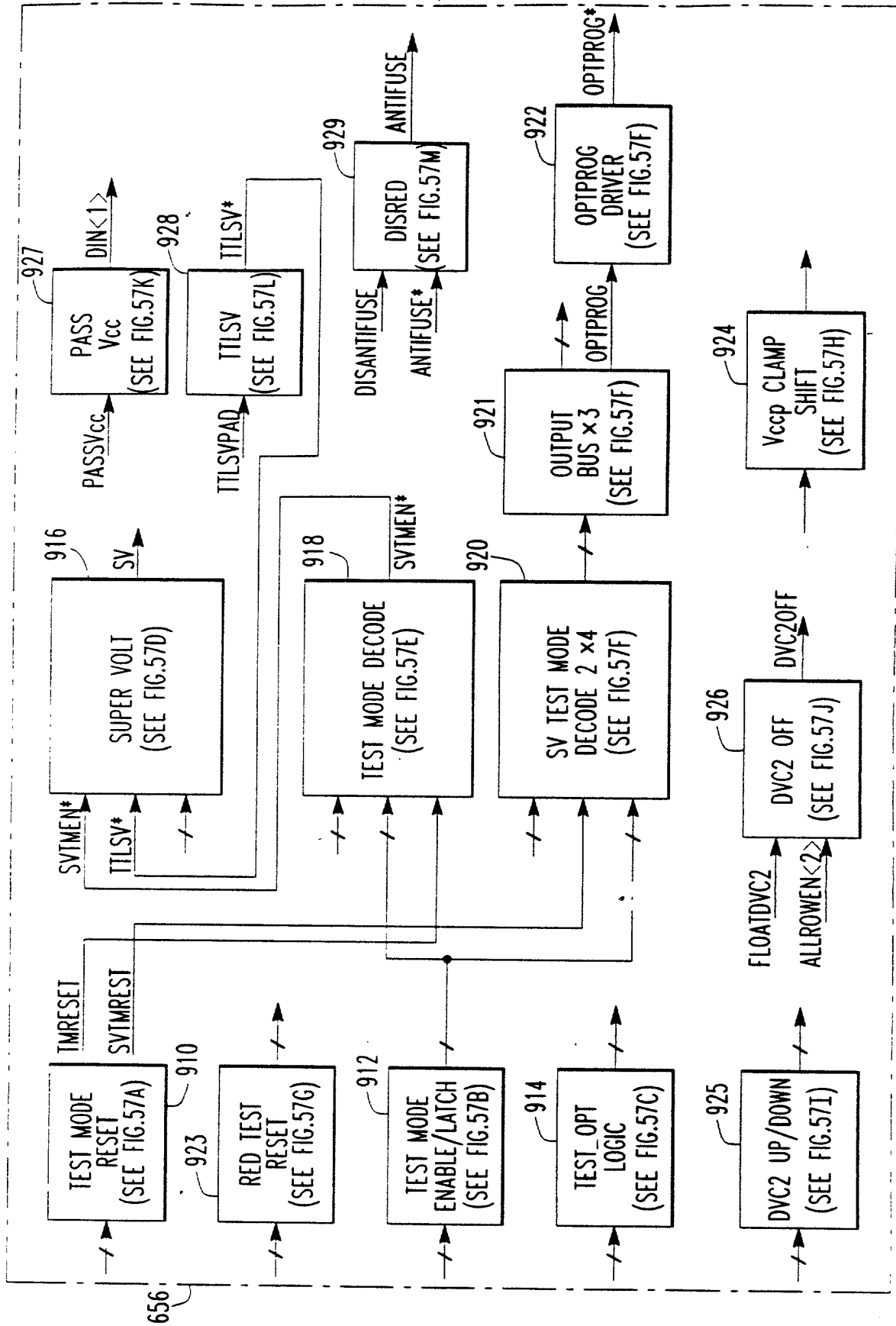


FIG. 56

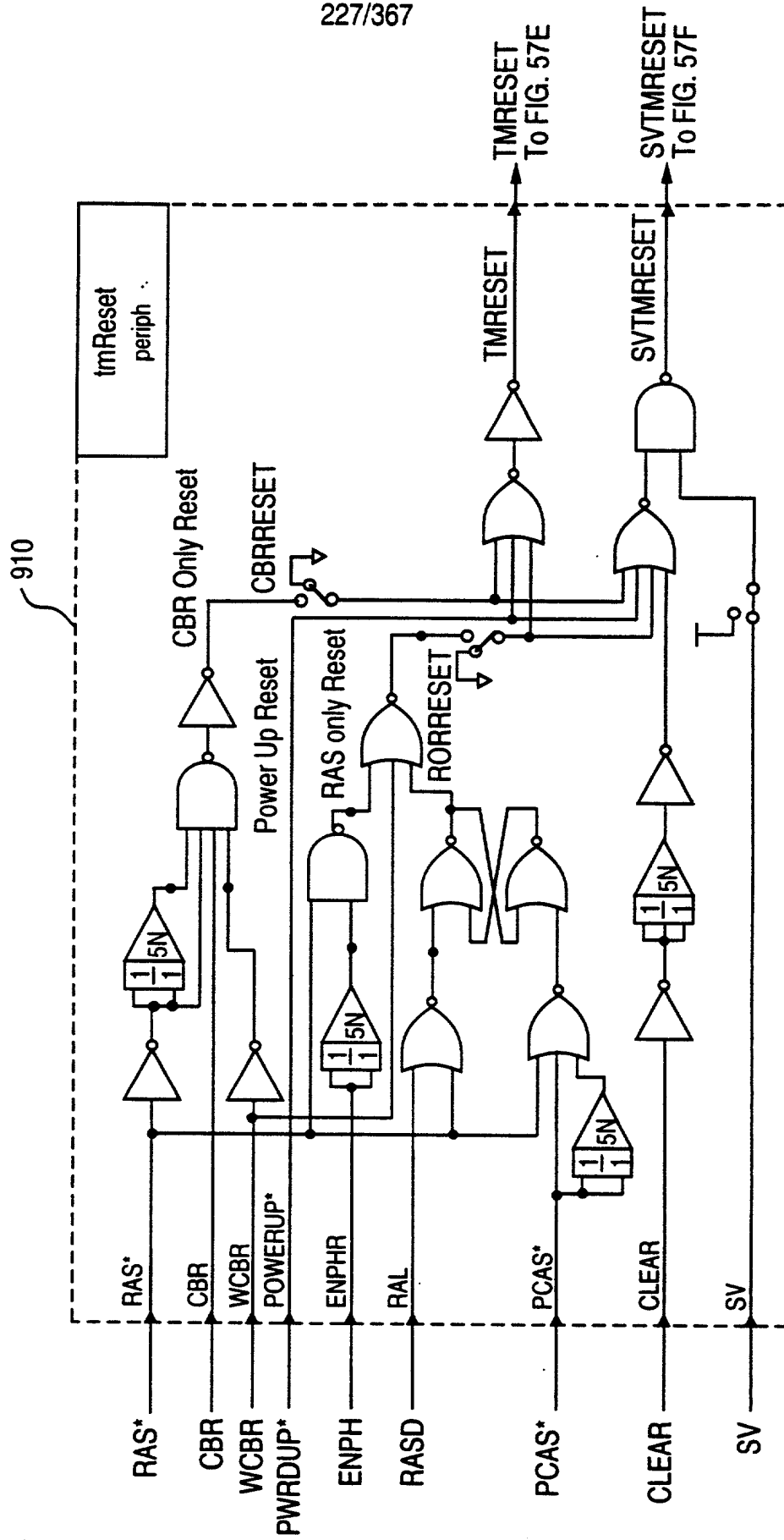


FIG. 57A

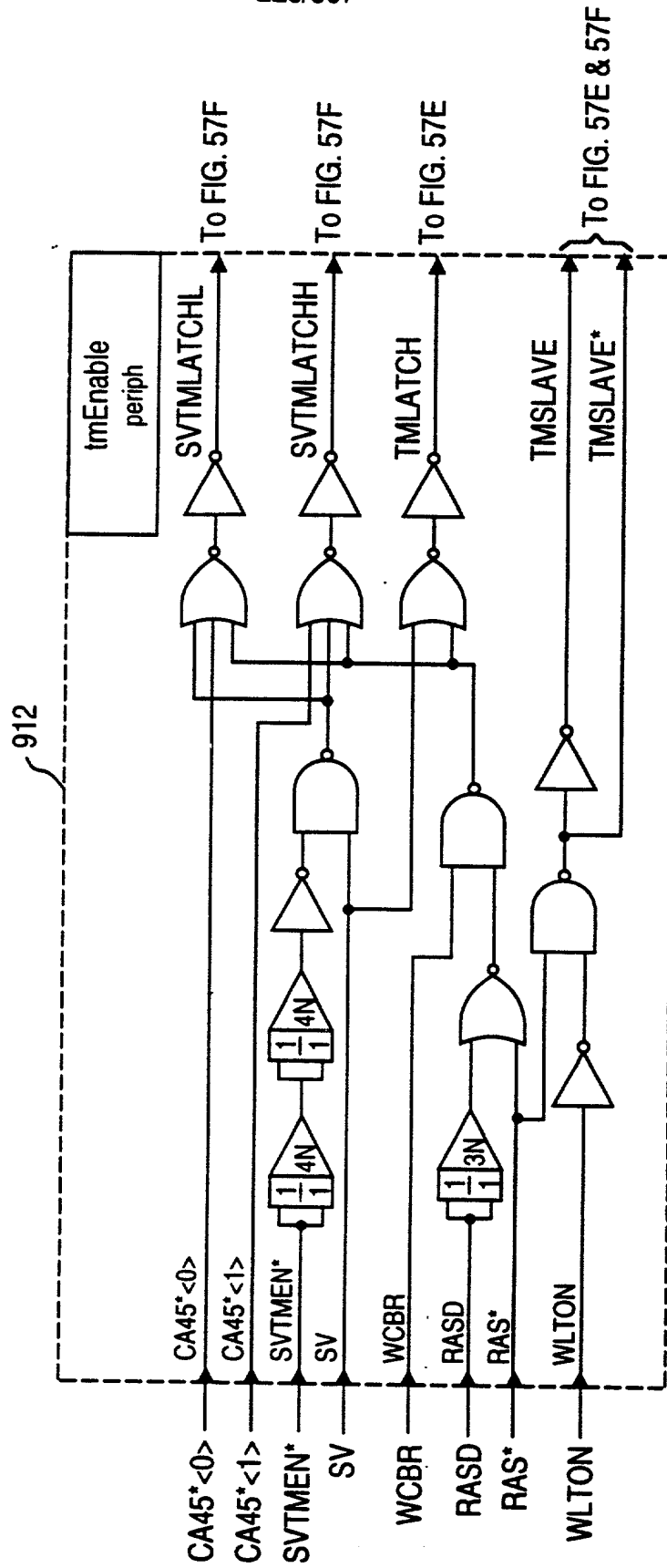


FIG. 57B

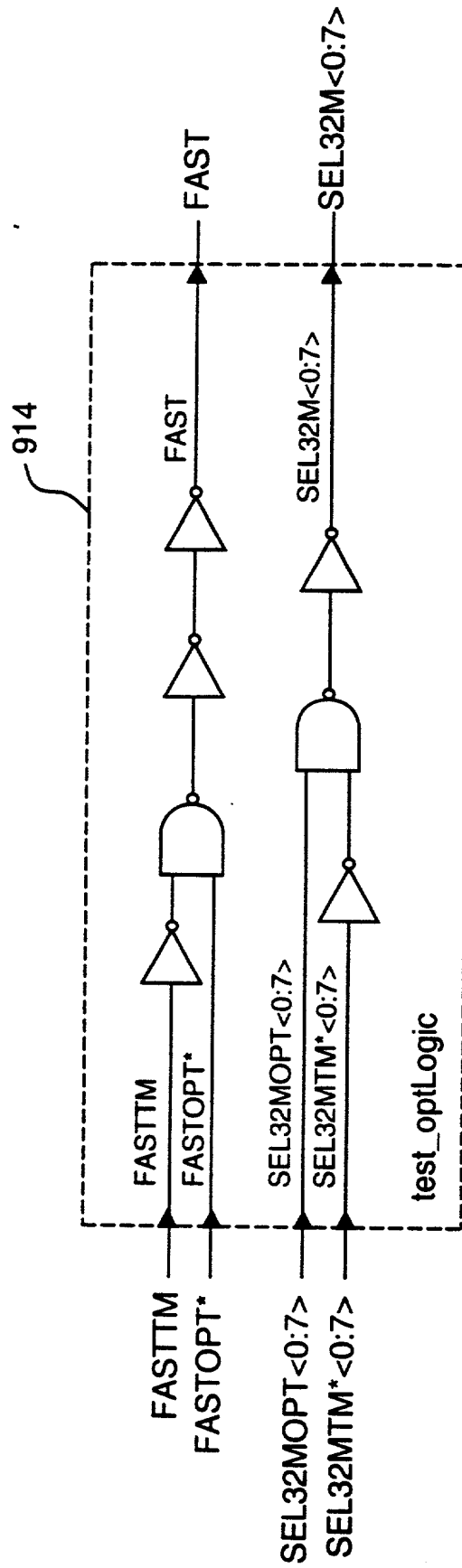


FIG. 57C

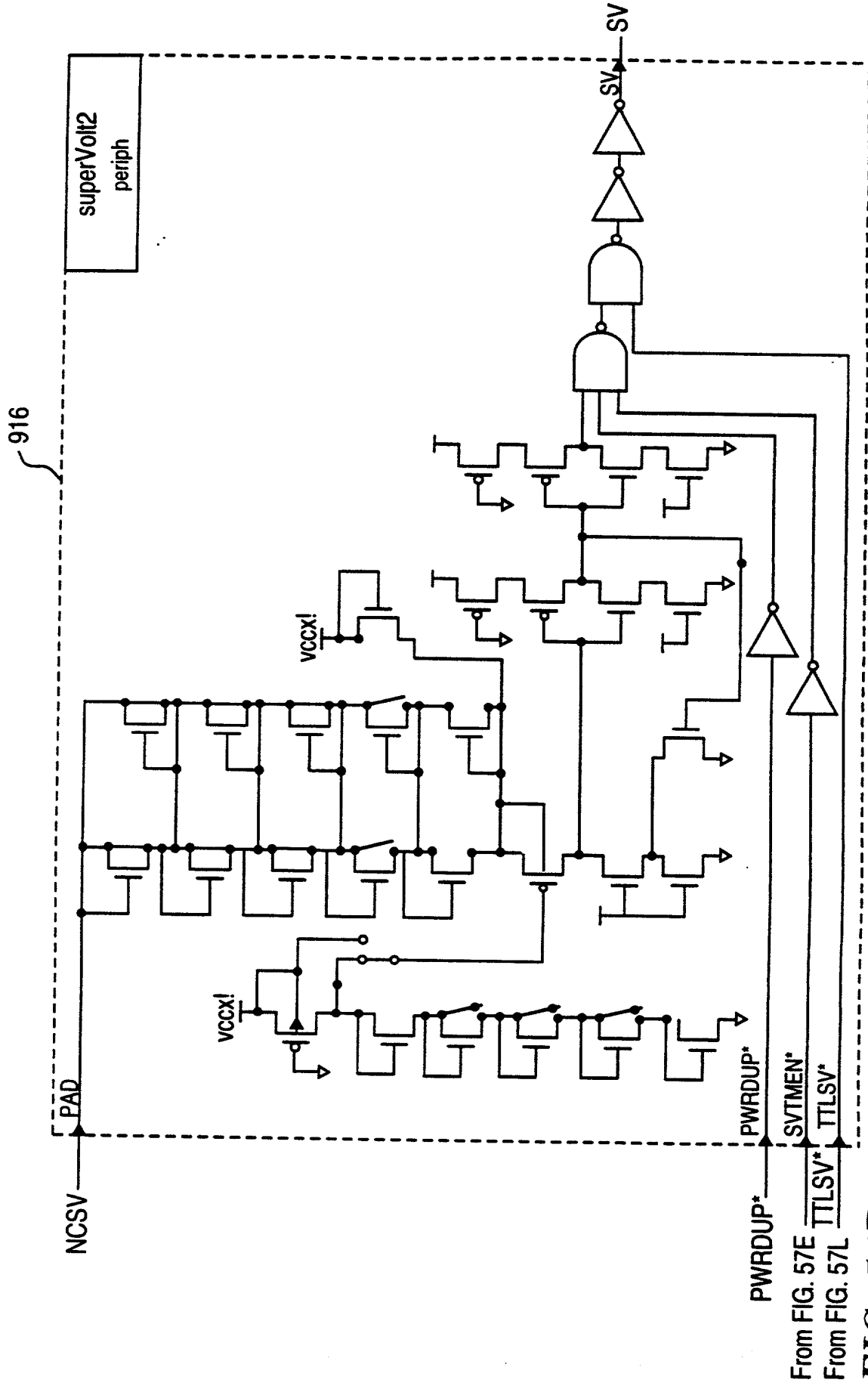


FIG. 57D

From FIG. 57E

From FIG. 57L

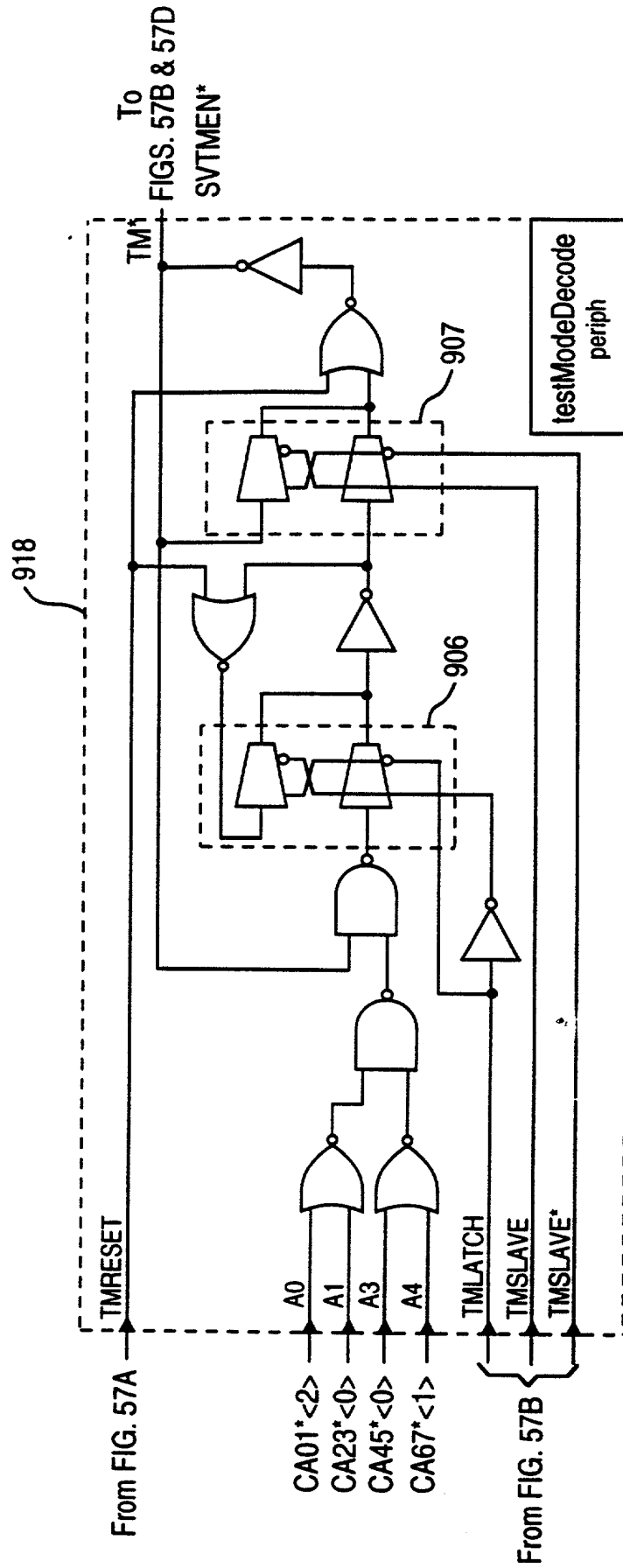


FIG. 57E

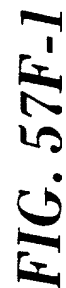


FIG. 57F-3

FIG. 57F-2

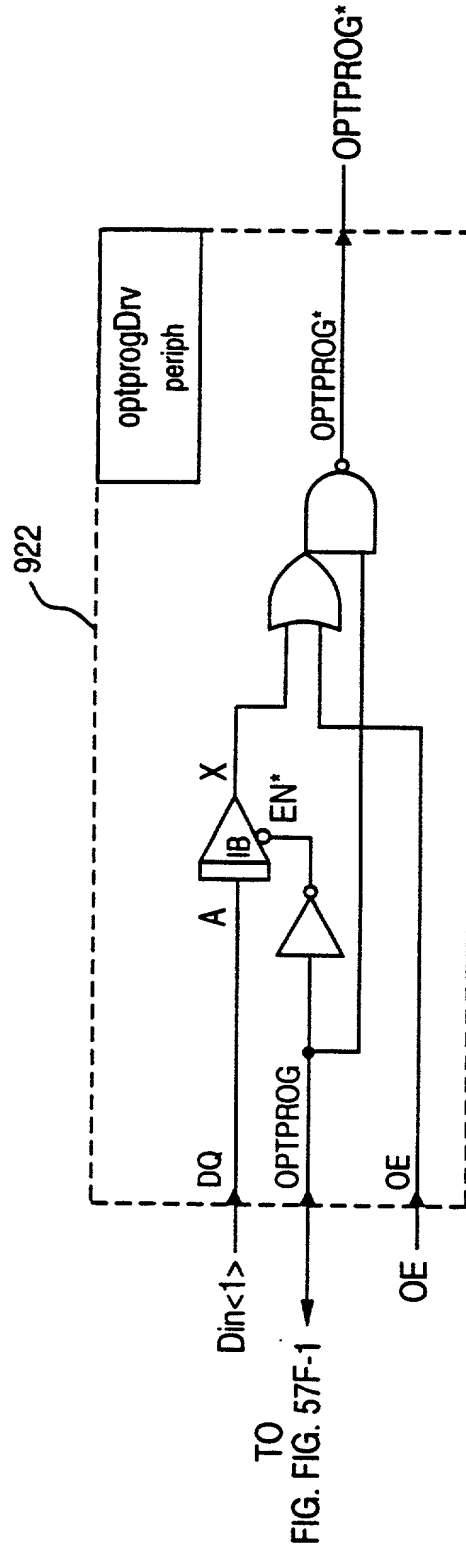


FIG. 57F-2

FIG. 57F-1

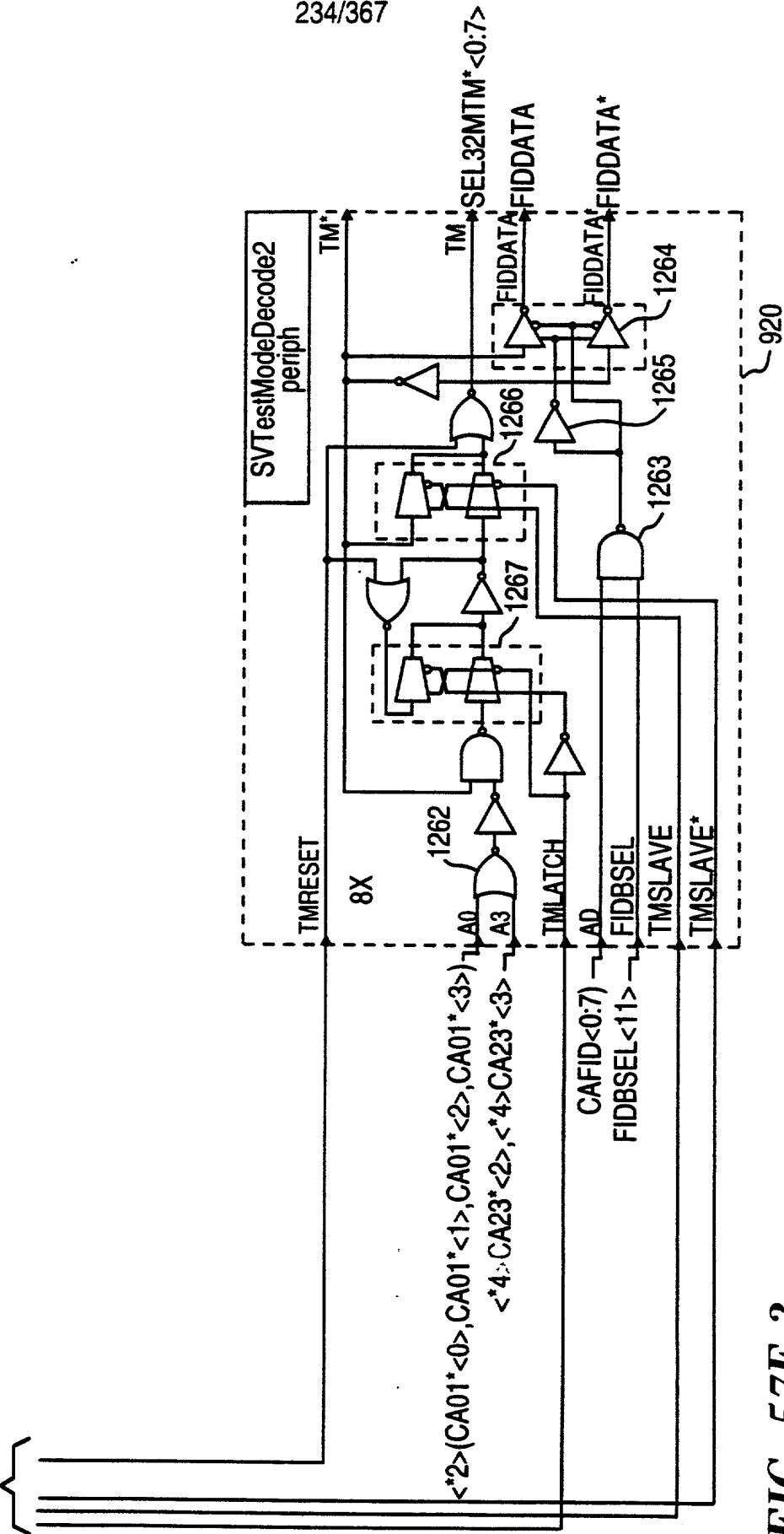


FIG. 57F-3

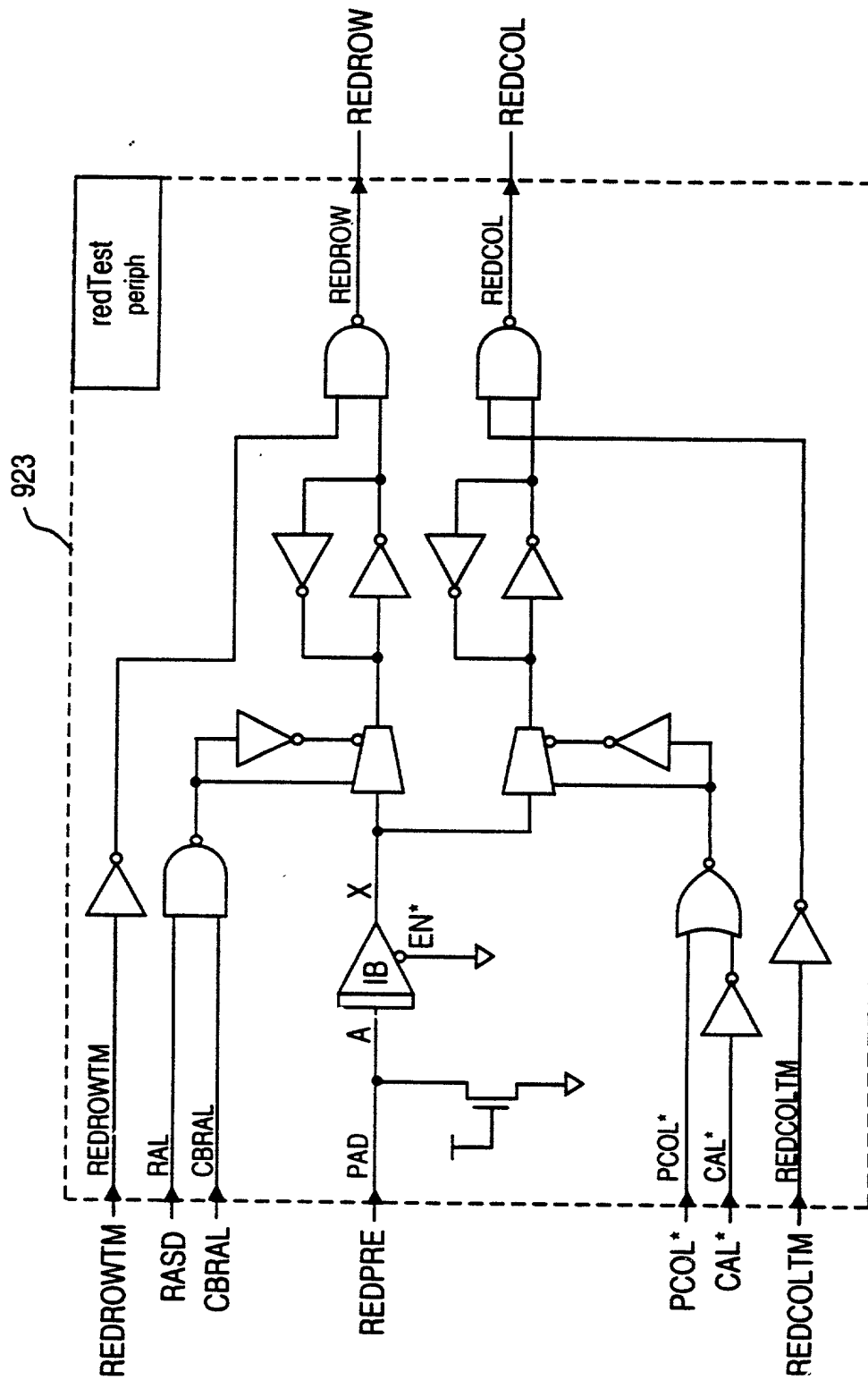
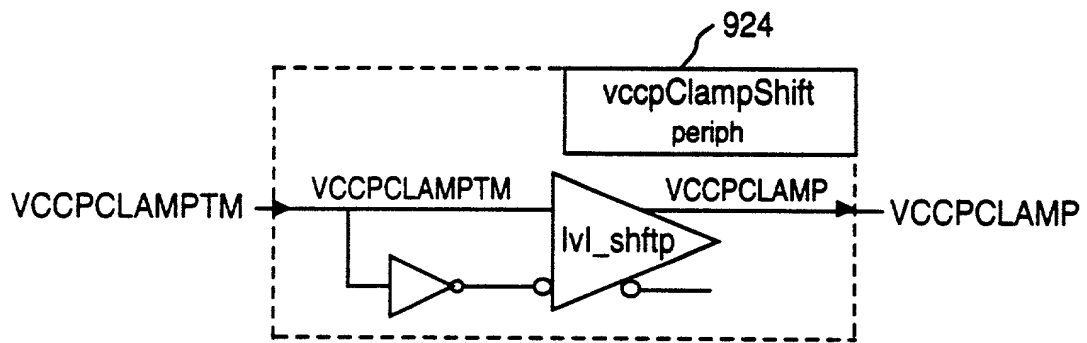
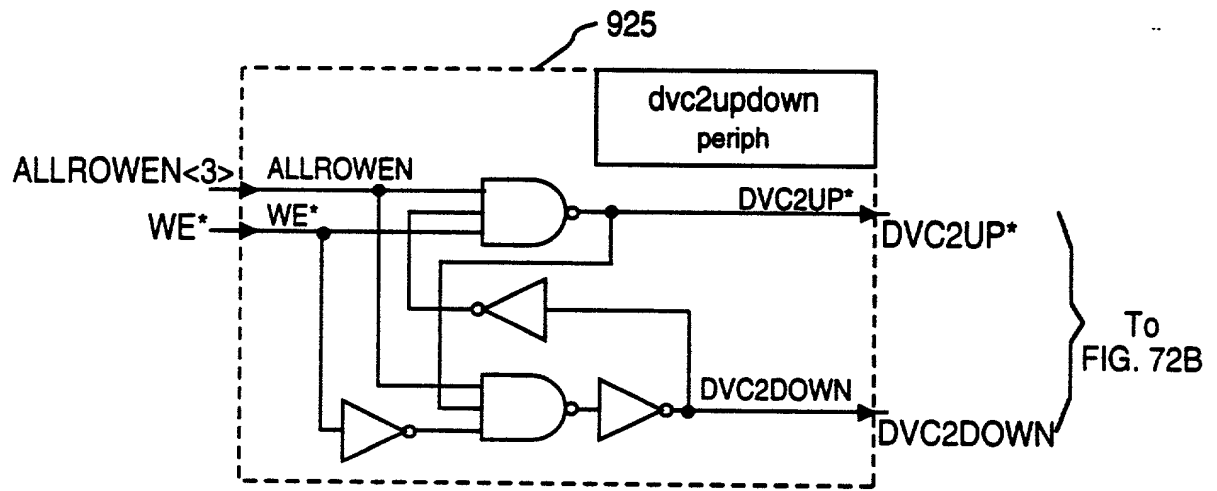
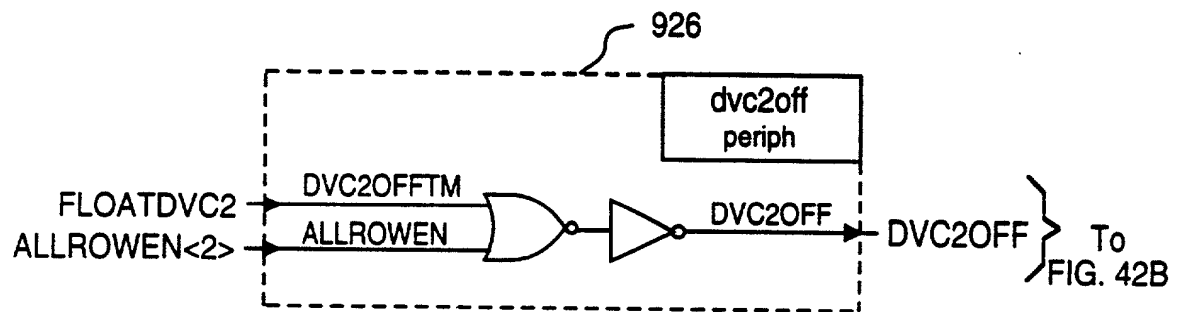
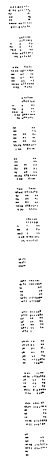


FIG. 57C

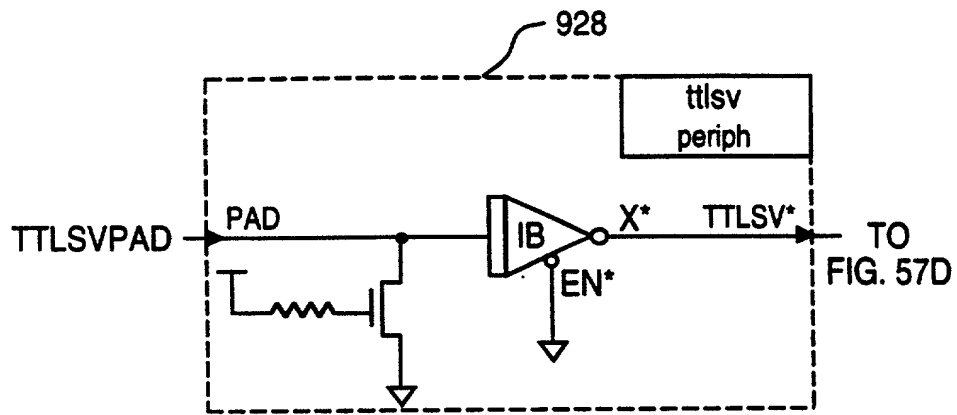
**FIG. 57H**

**FIG. 57I**

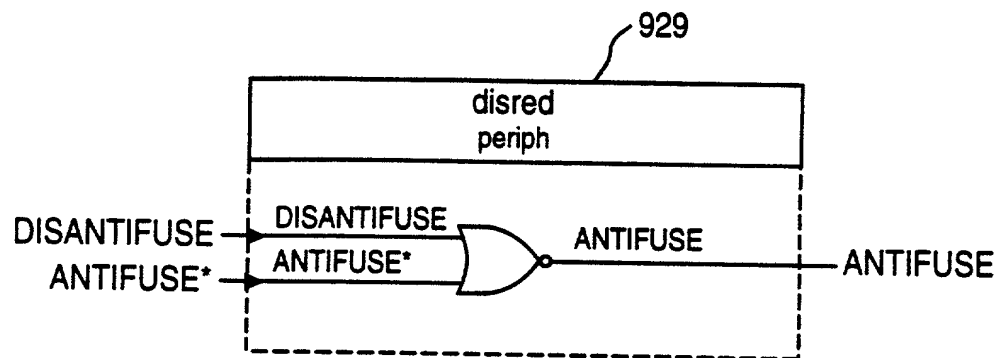
**FIG. 57J**



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**FIG. 57L**



**FIG. 57M**

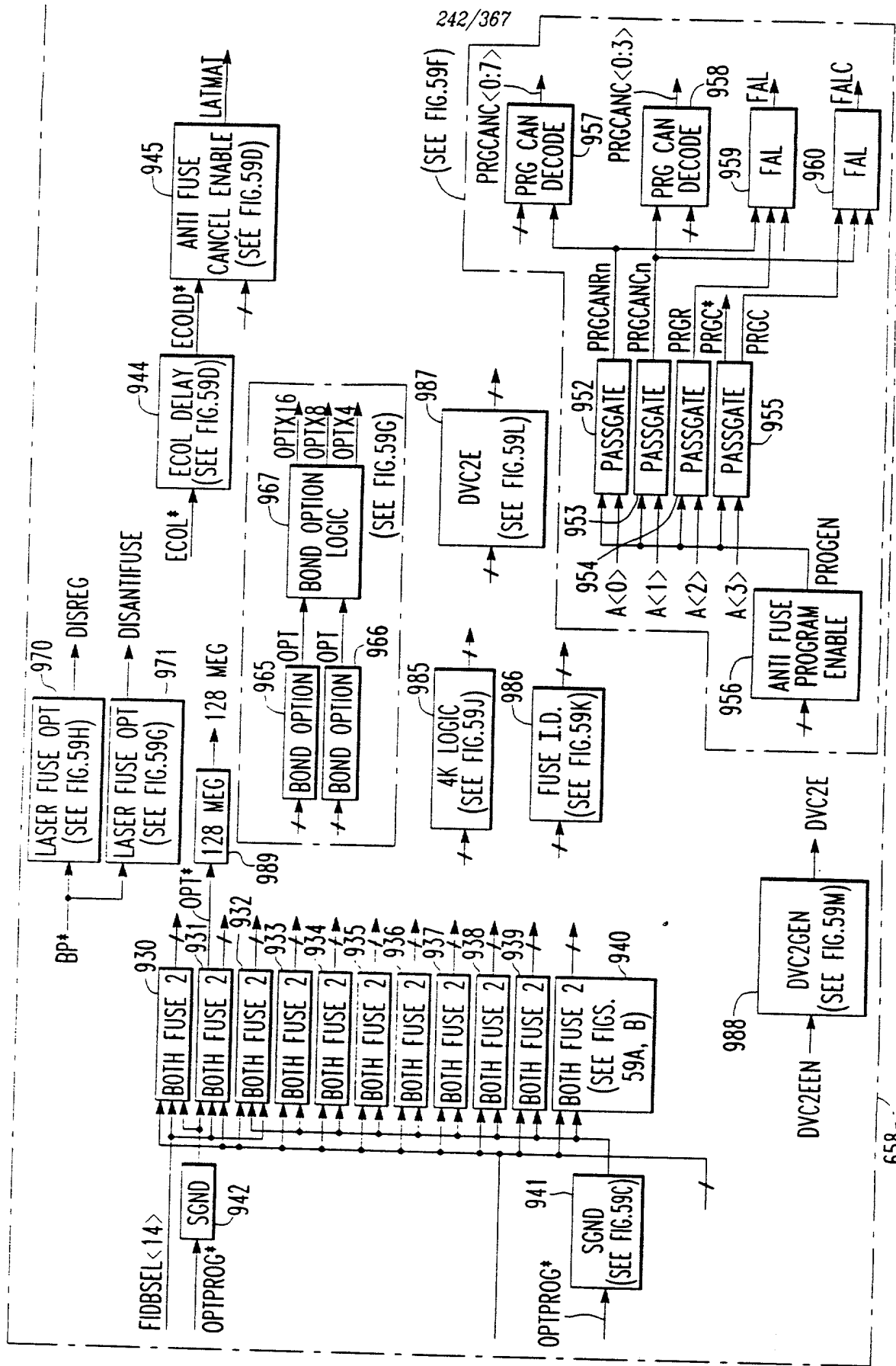


FIG. 58A

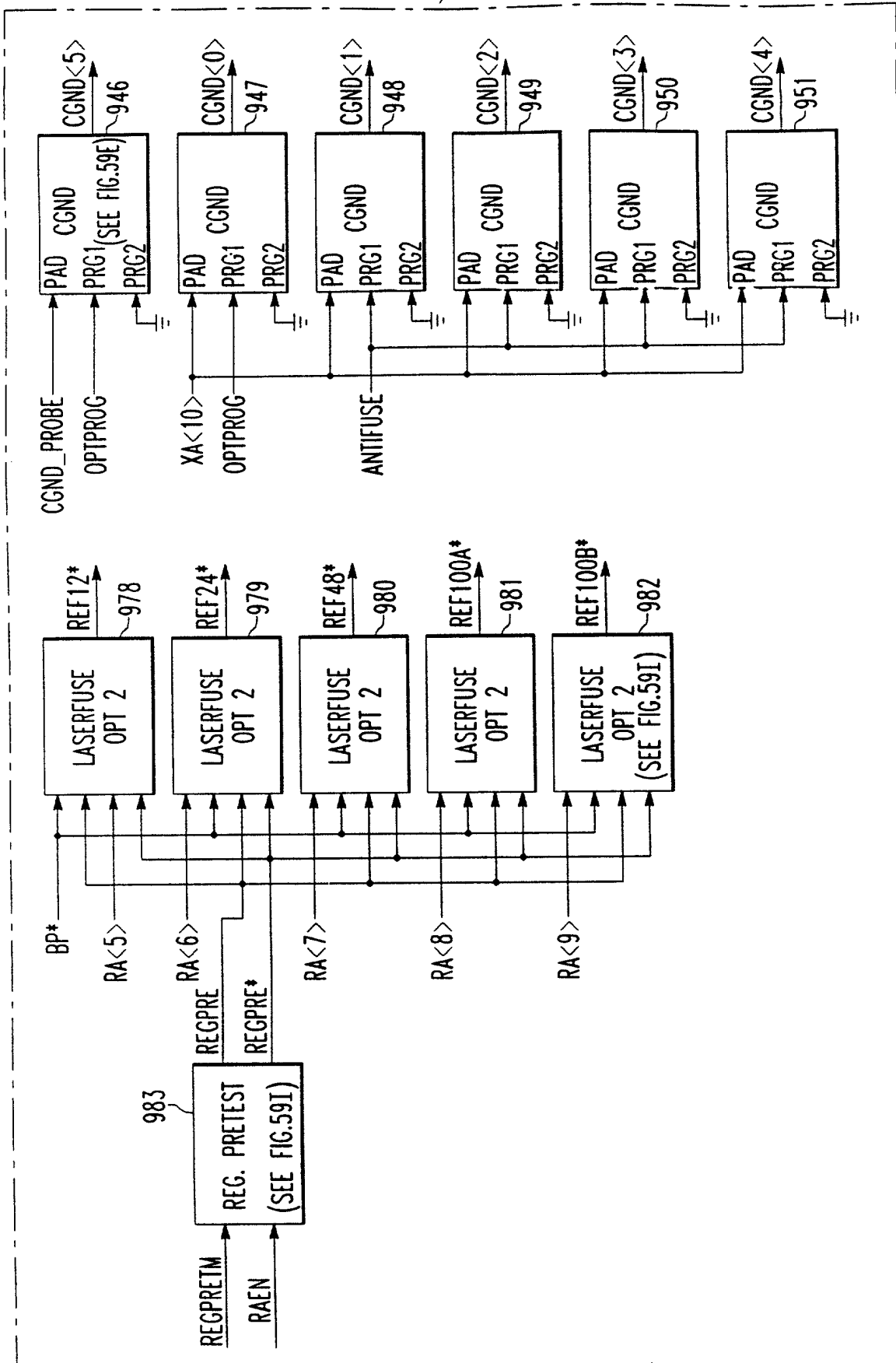
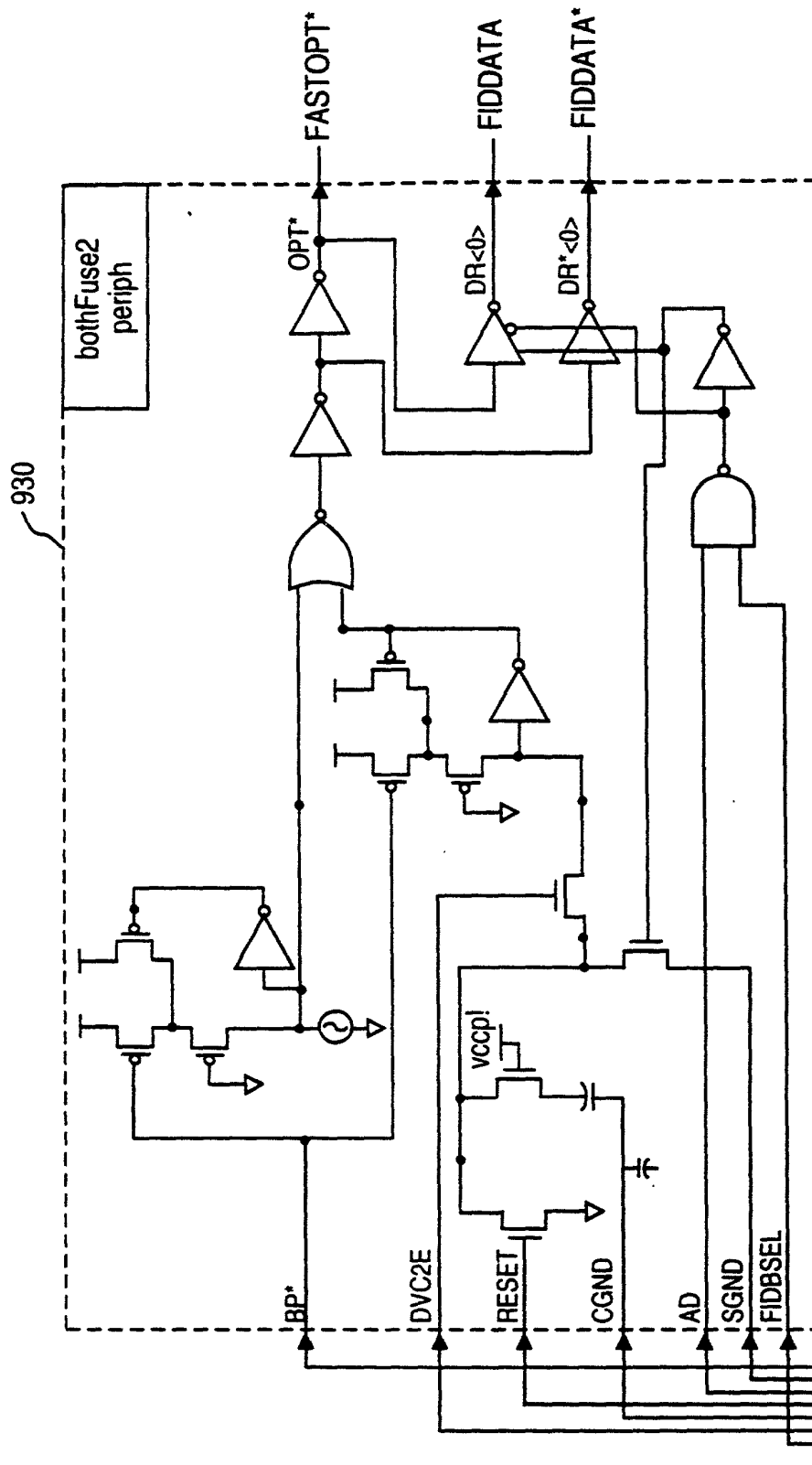


FIG. 58B



To  
FIG. 59B

FIG. 59A



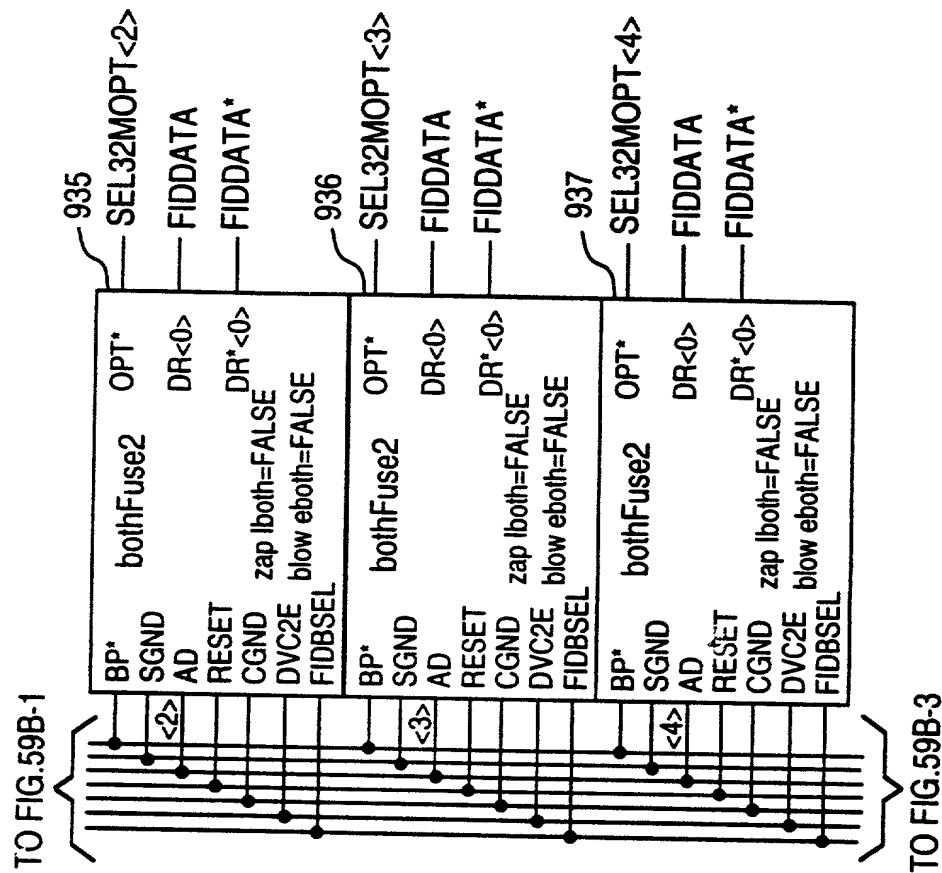


FIG. 59B-2

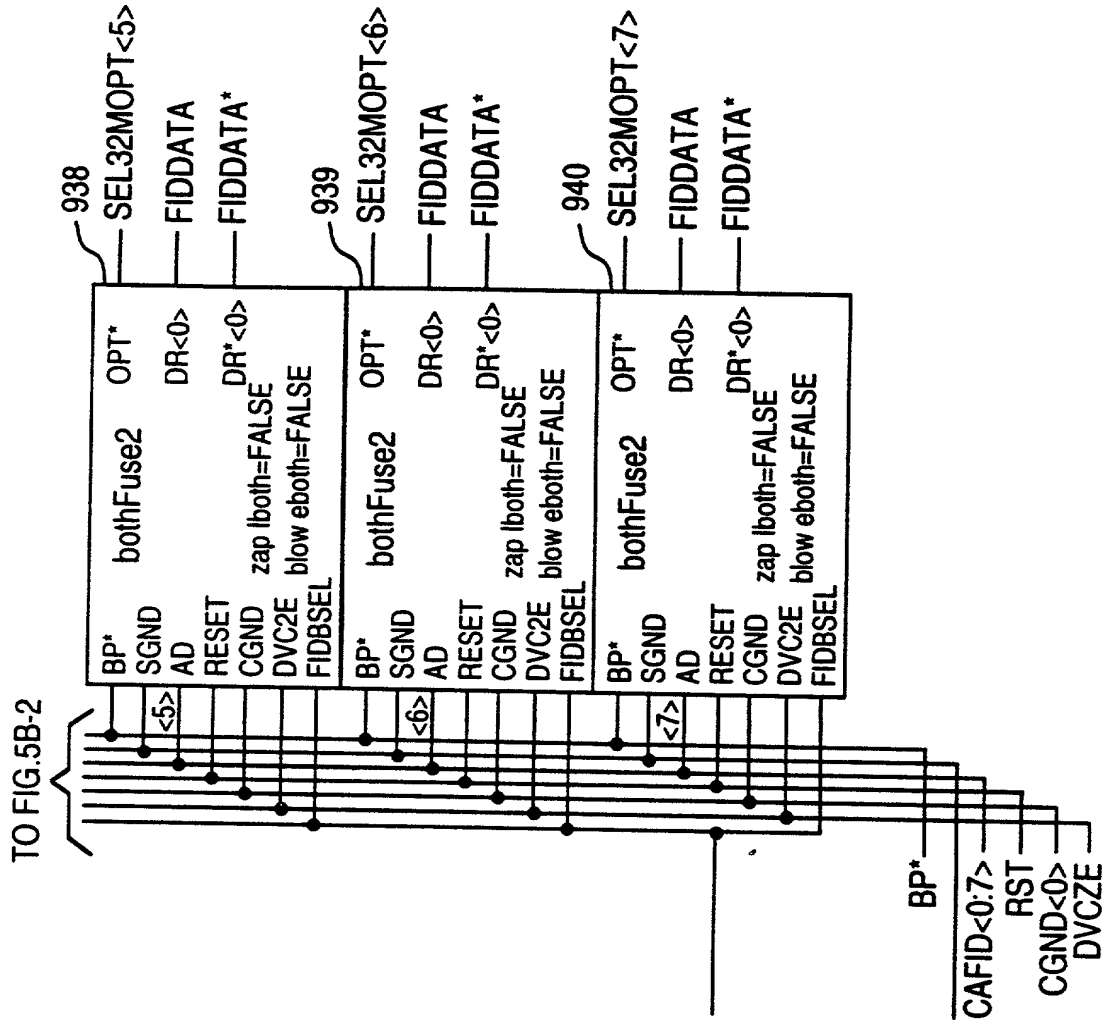
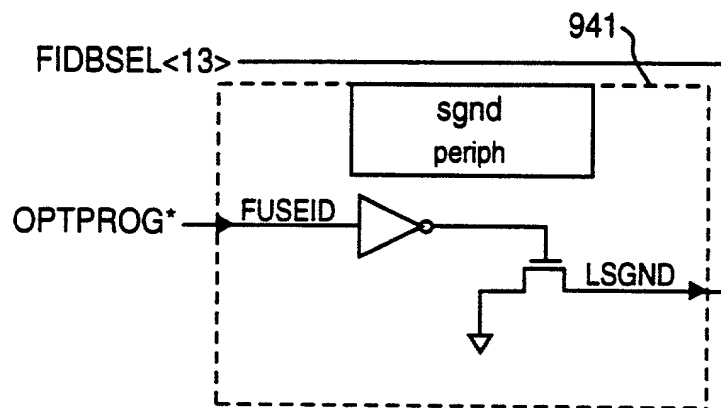


FIG. 59B-3

**FIG. 59C**



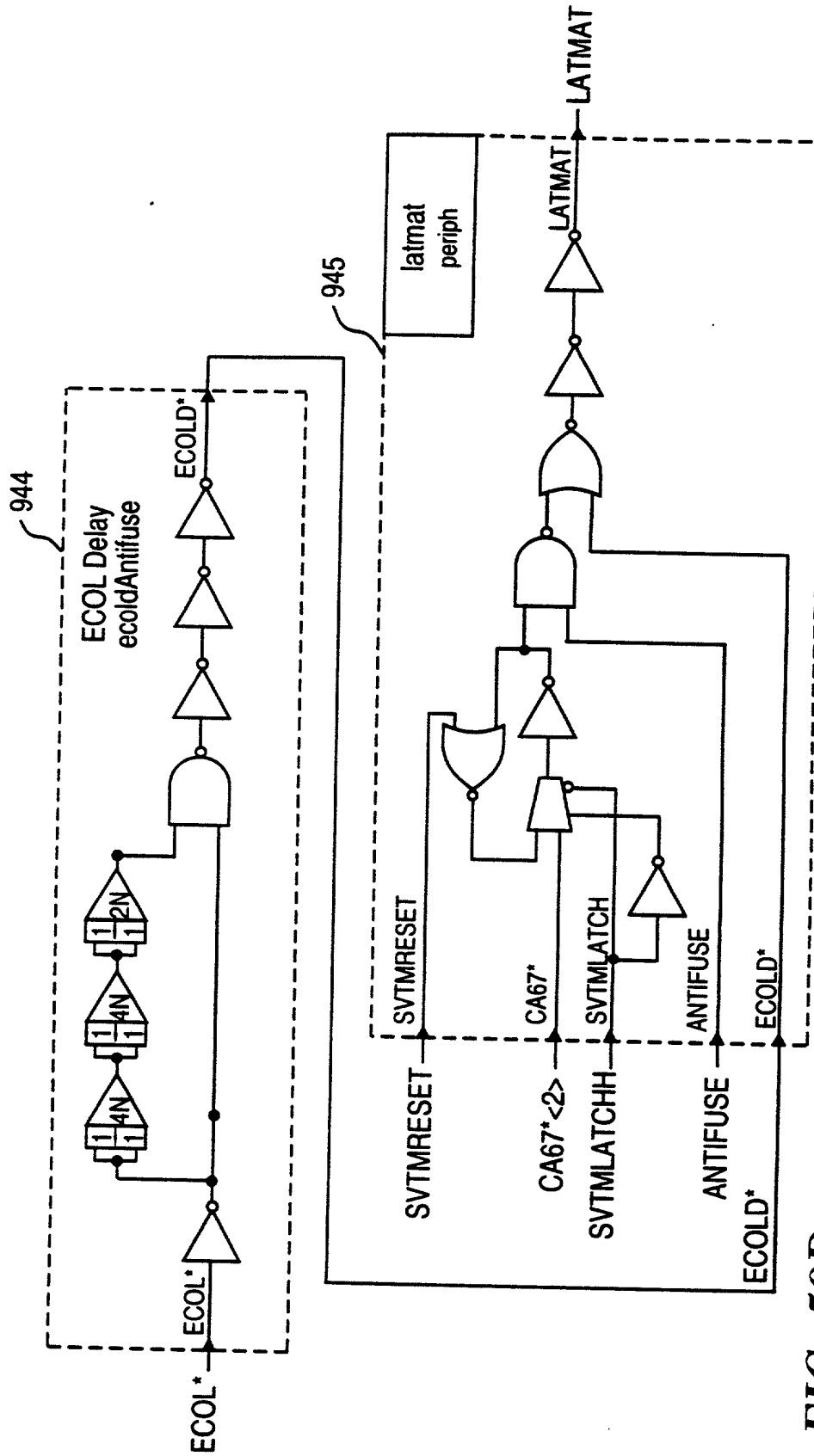


FIG. 59D

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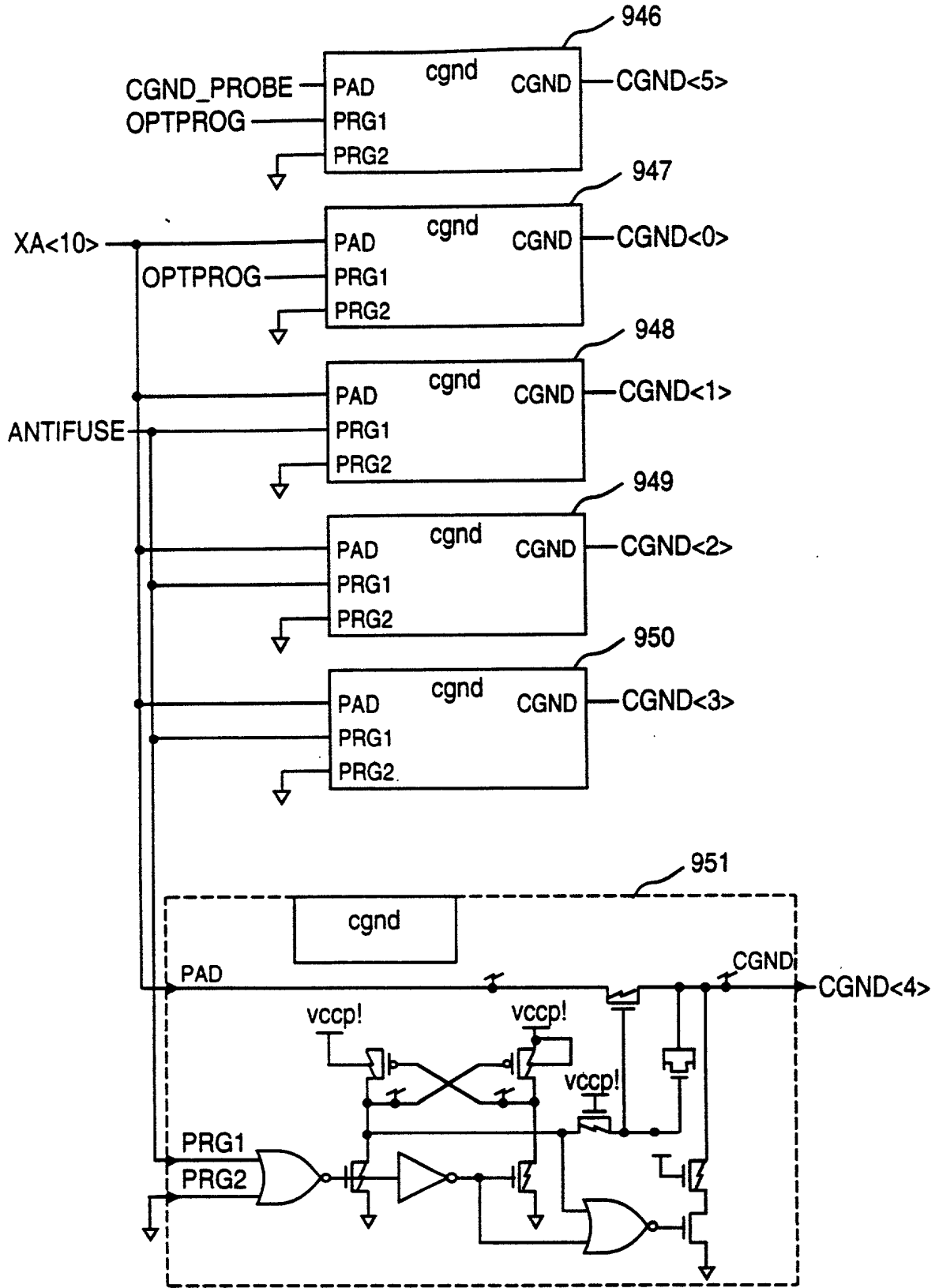


FIG. 59E

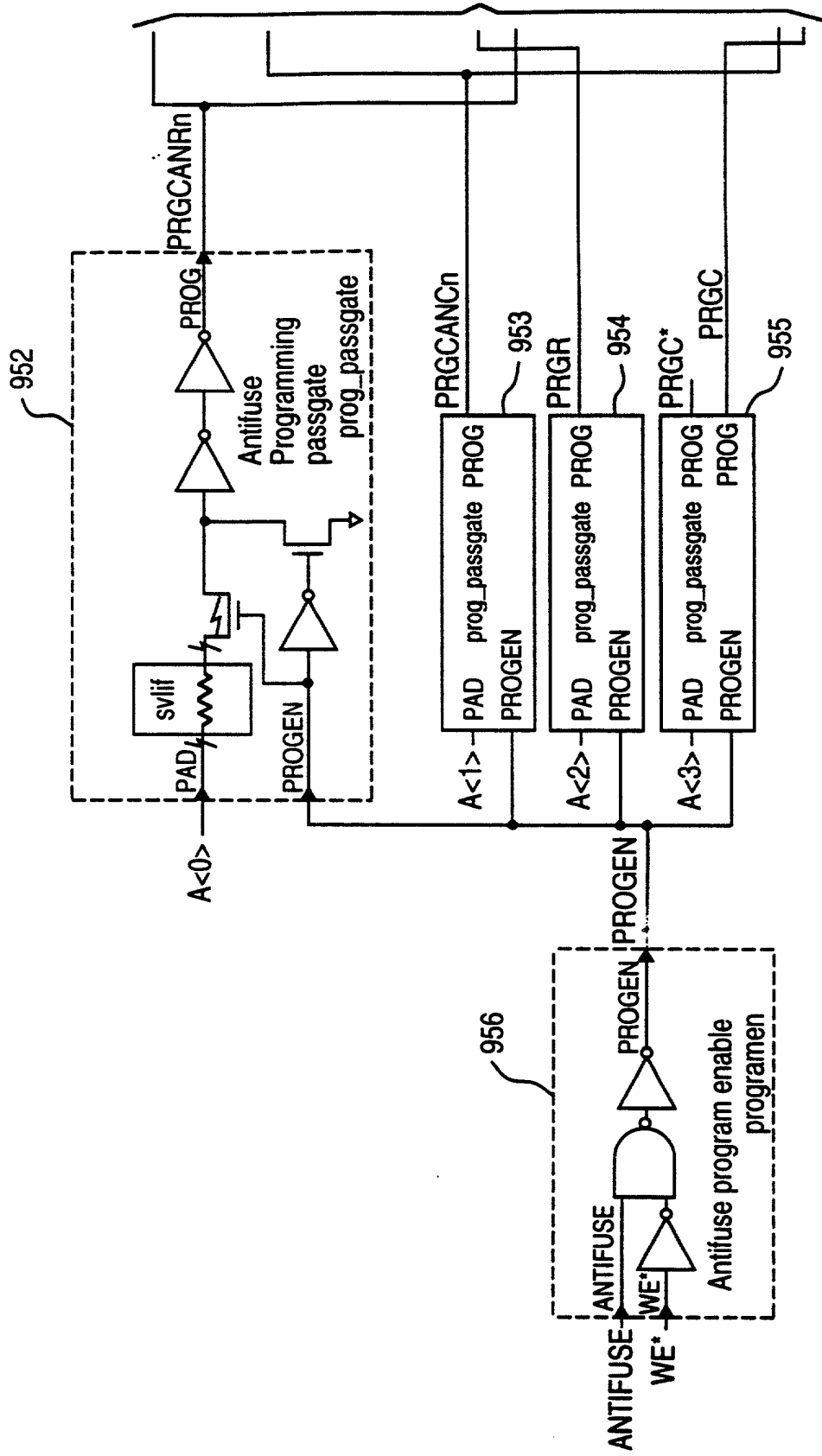


FIG. 59F-1

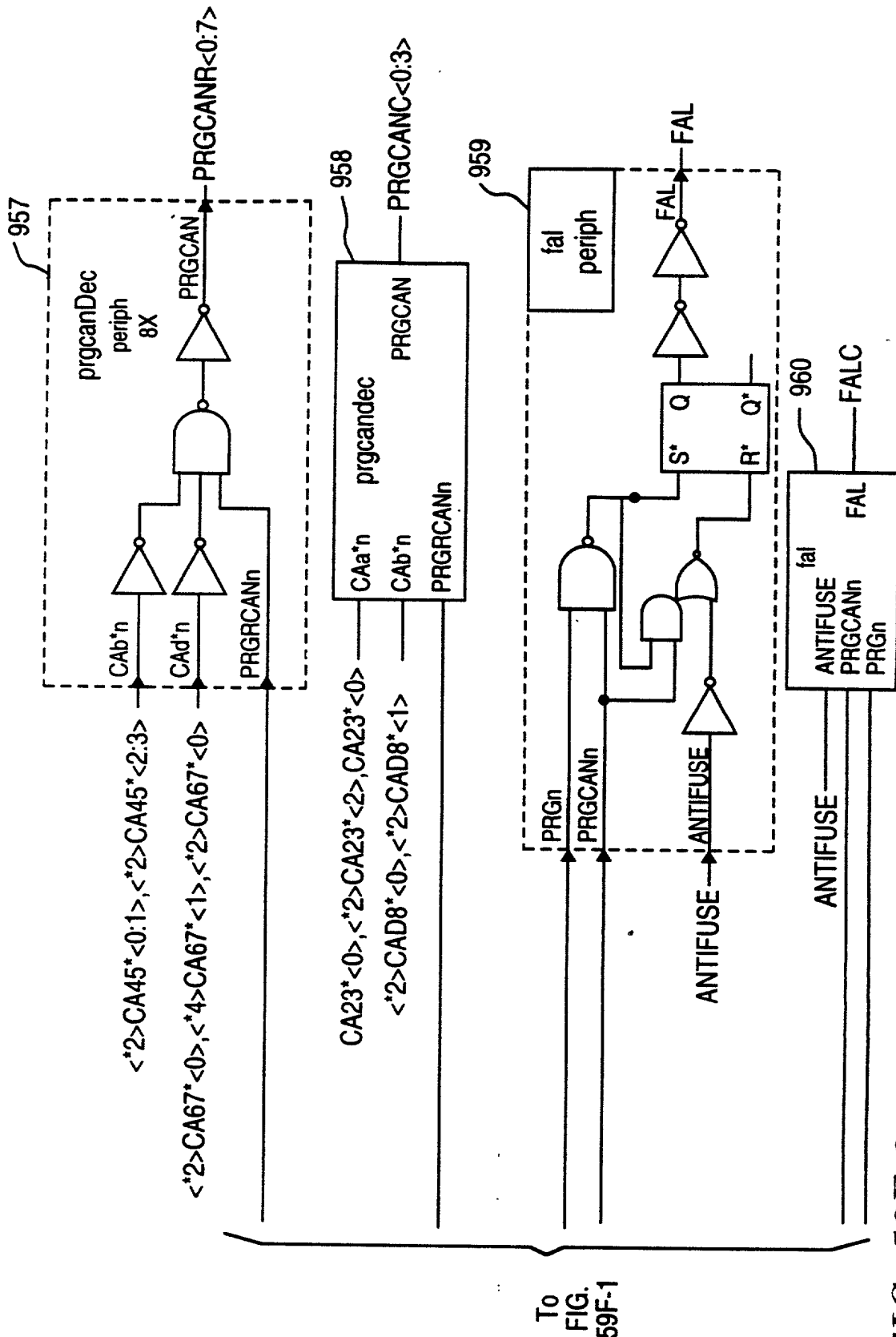


FIG. 59F-2

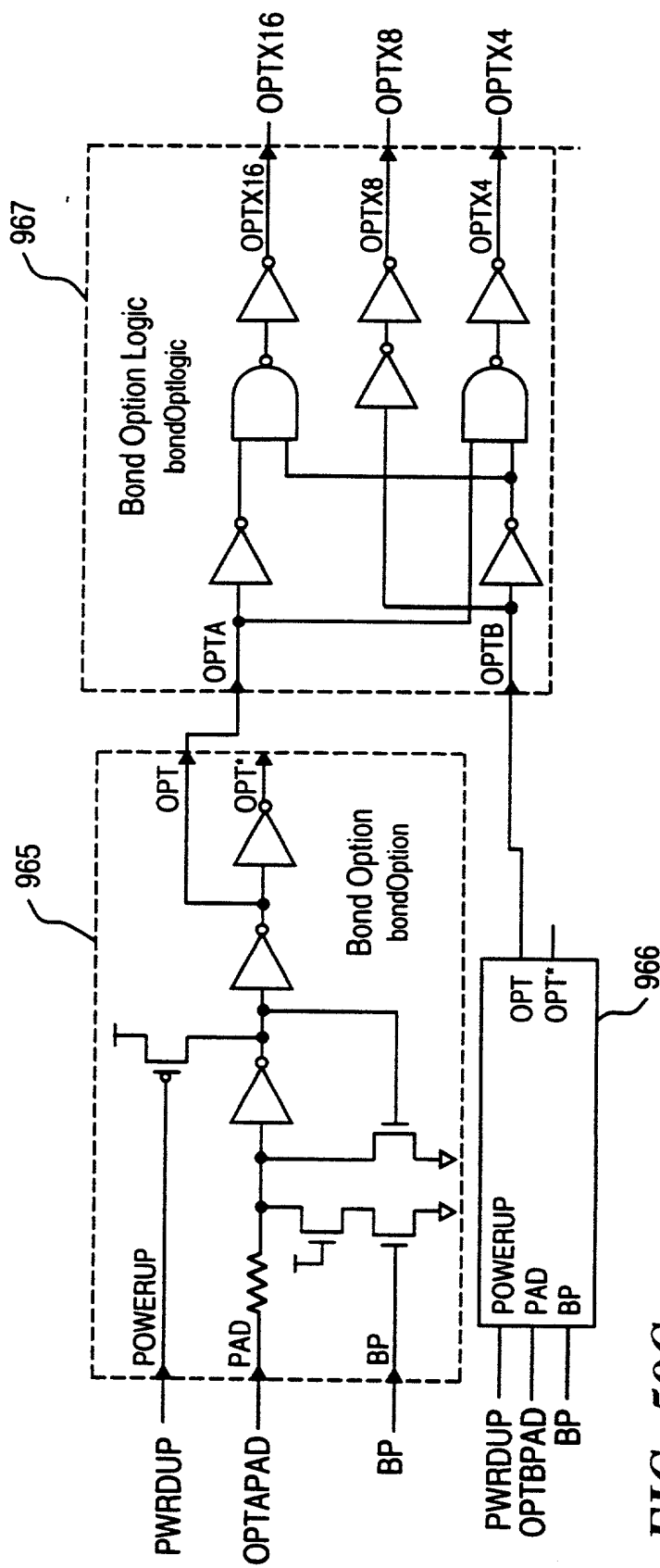


FIG. 59G

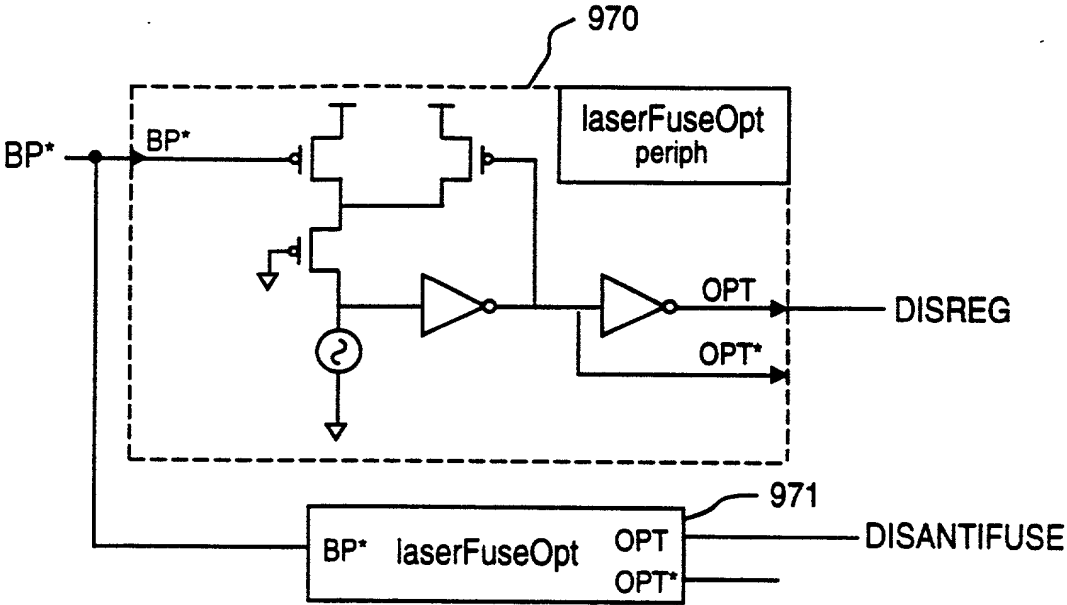


FIG. 59H

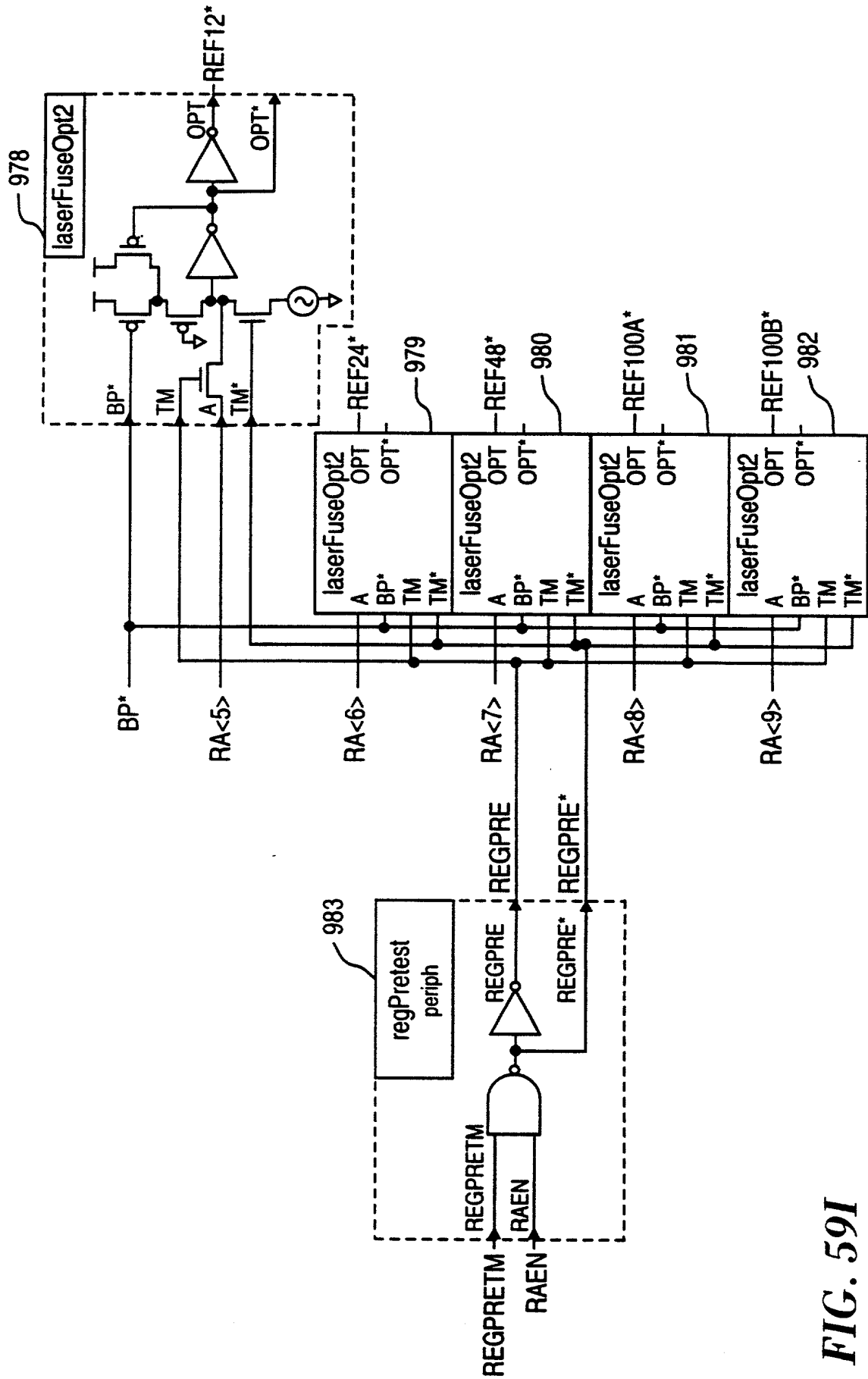
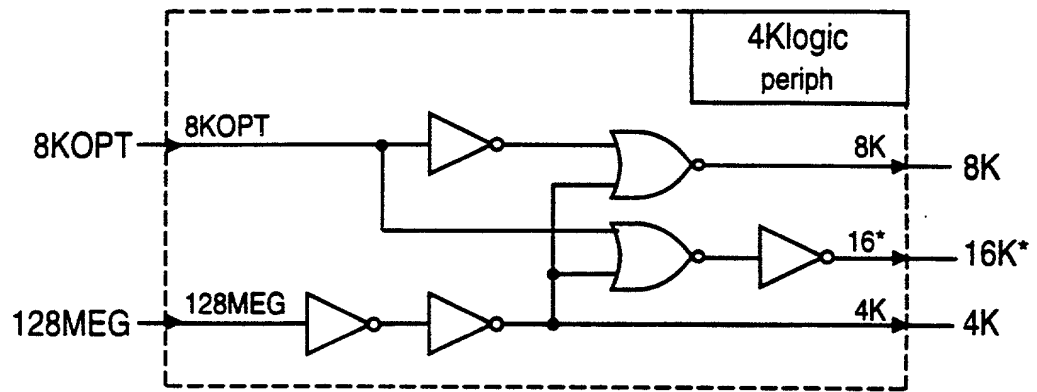
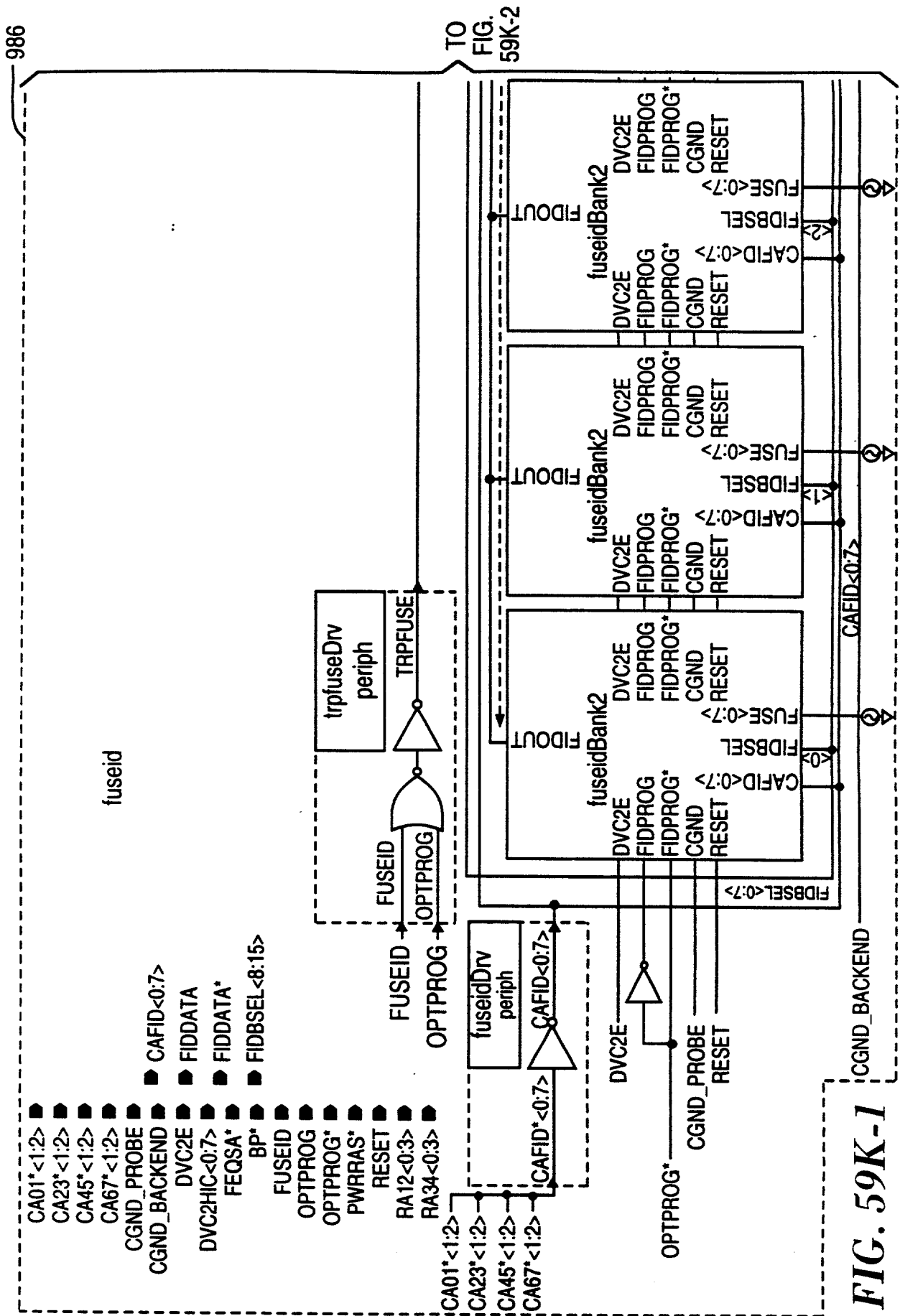
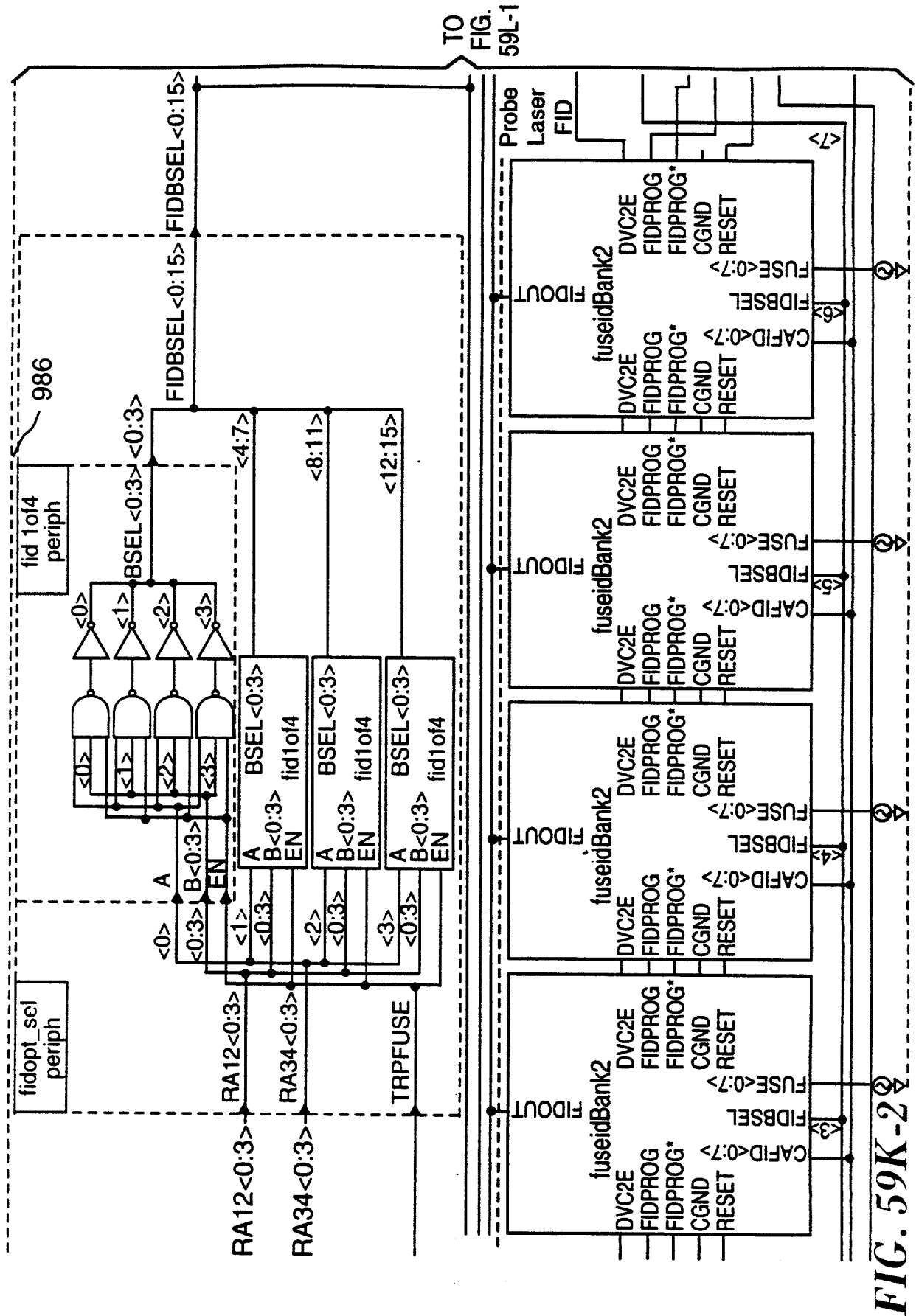


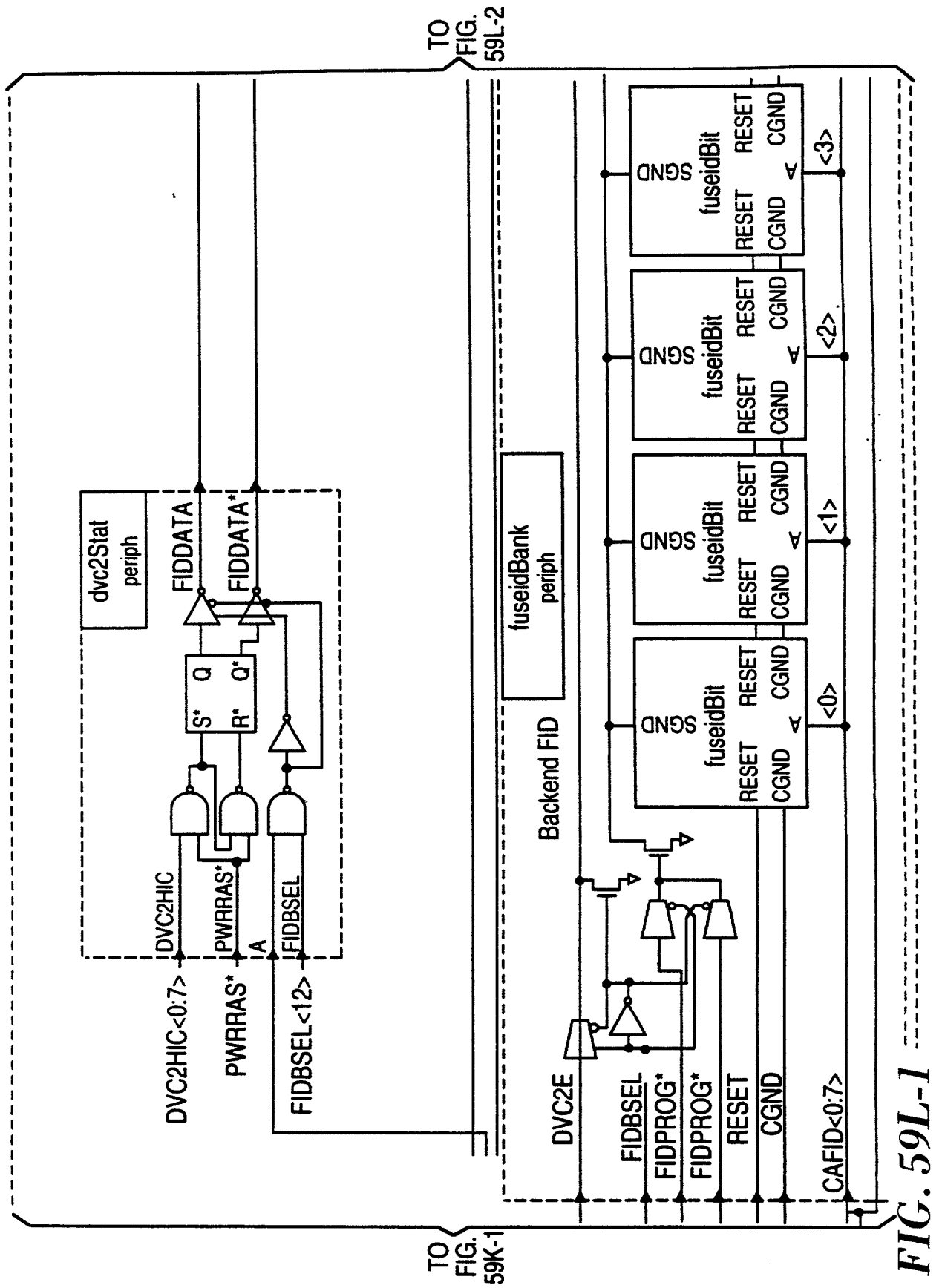
FIG. 59I

**FIG. 59J**









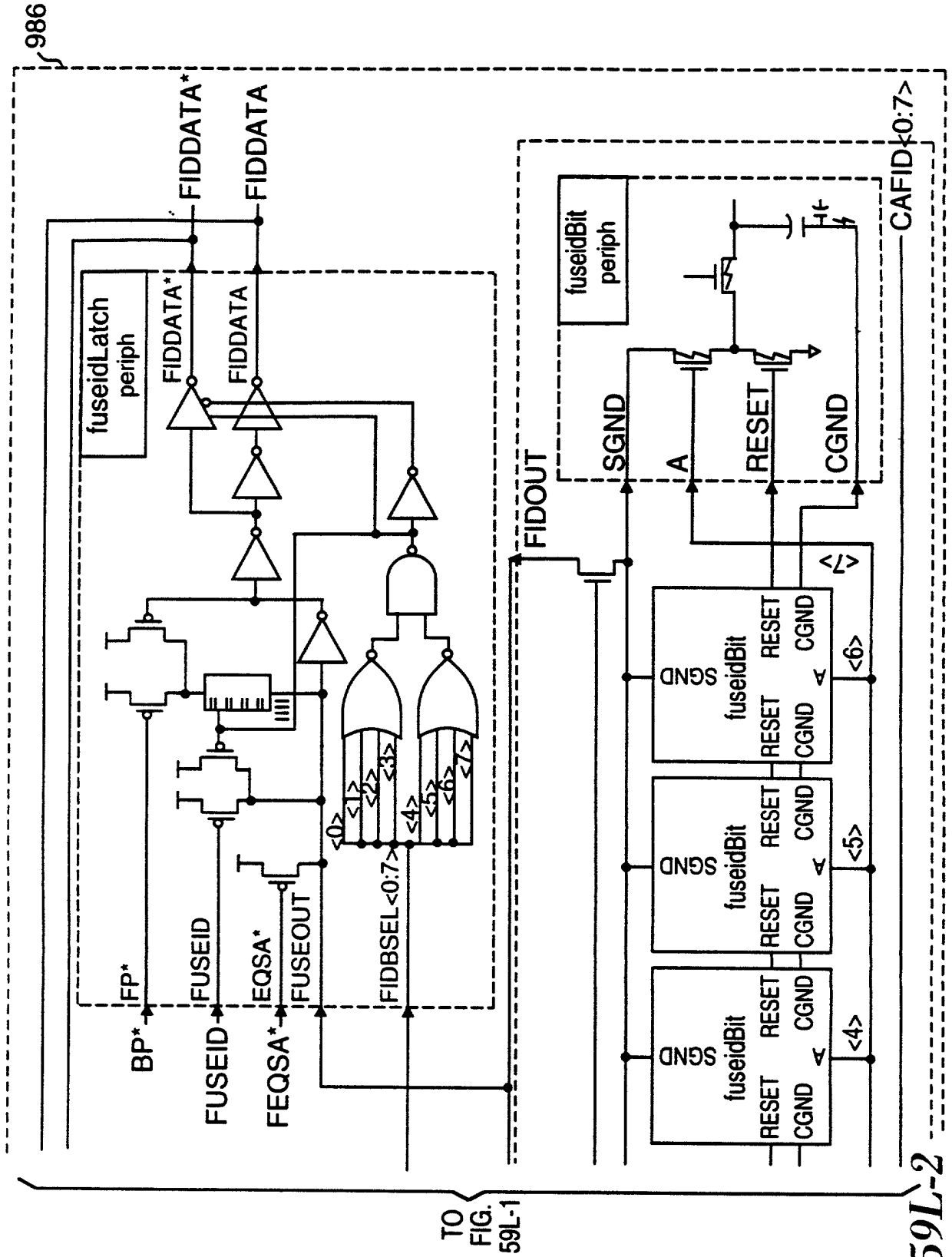
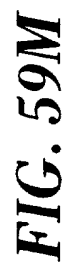
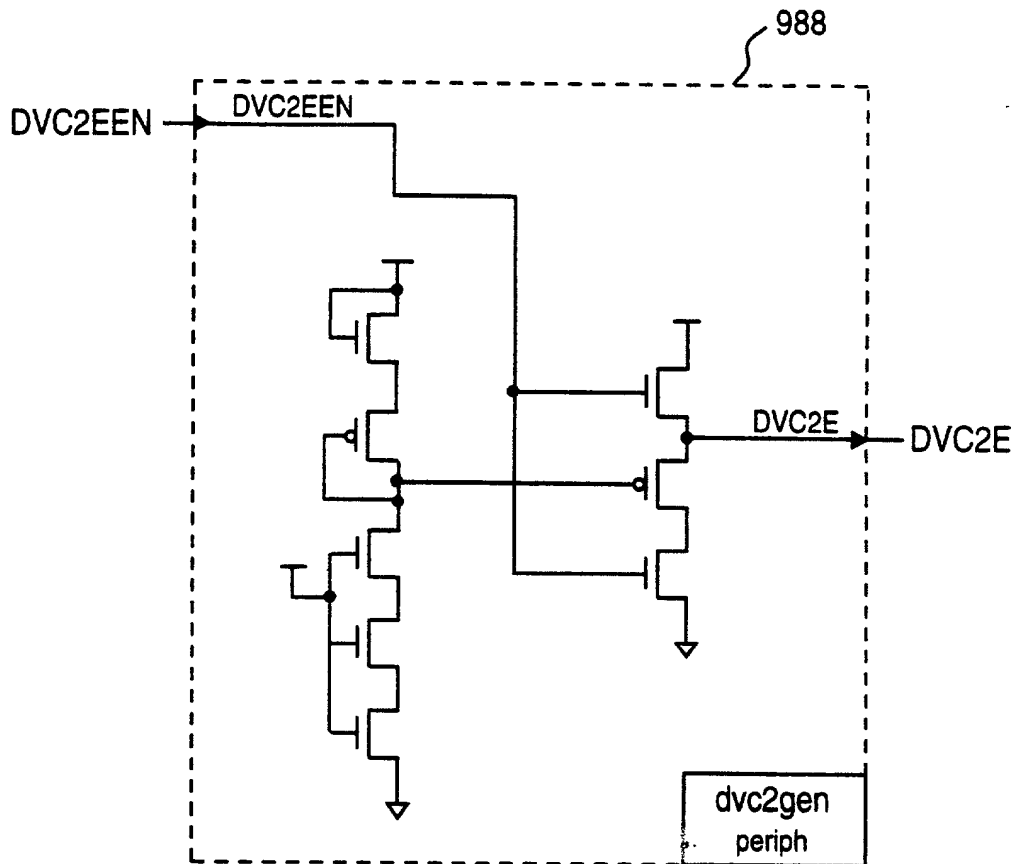


FIG. 59L-2



**FIG. 59M**

**FIG. 59N**

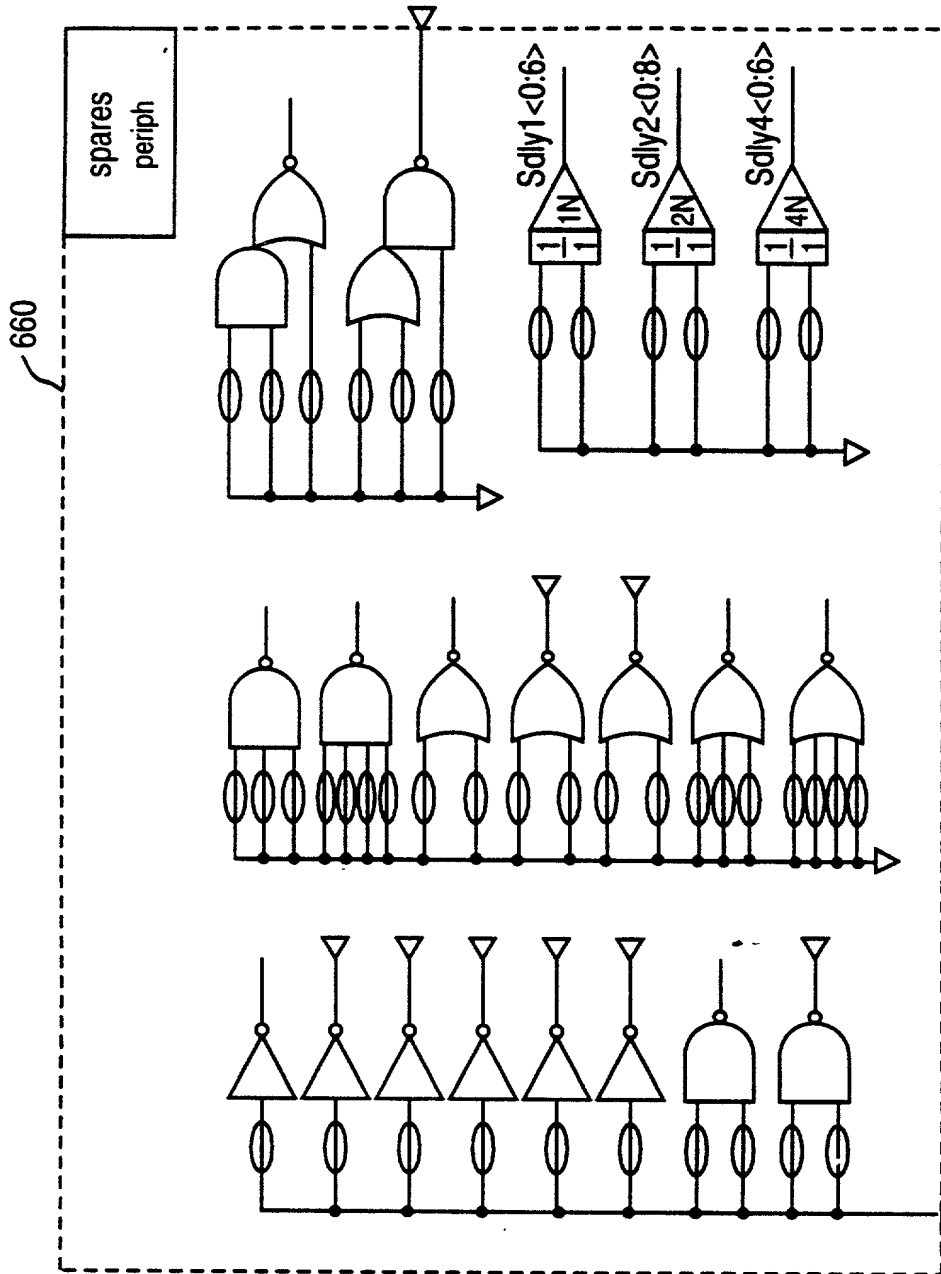


FIG. 590

FIG. 590







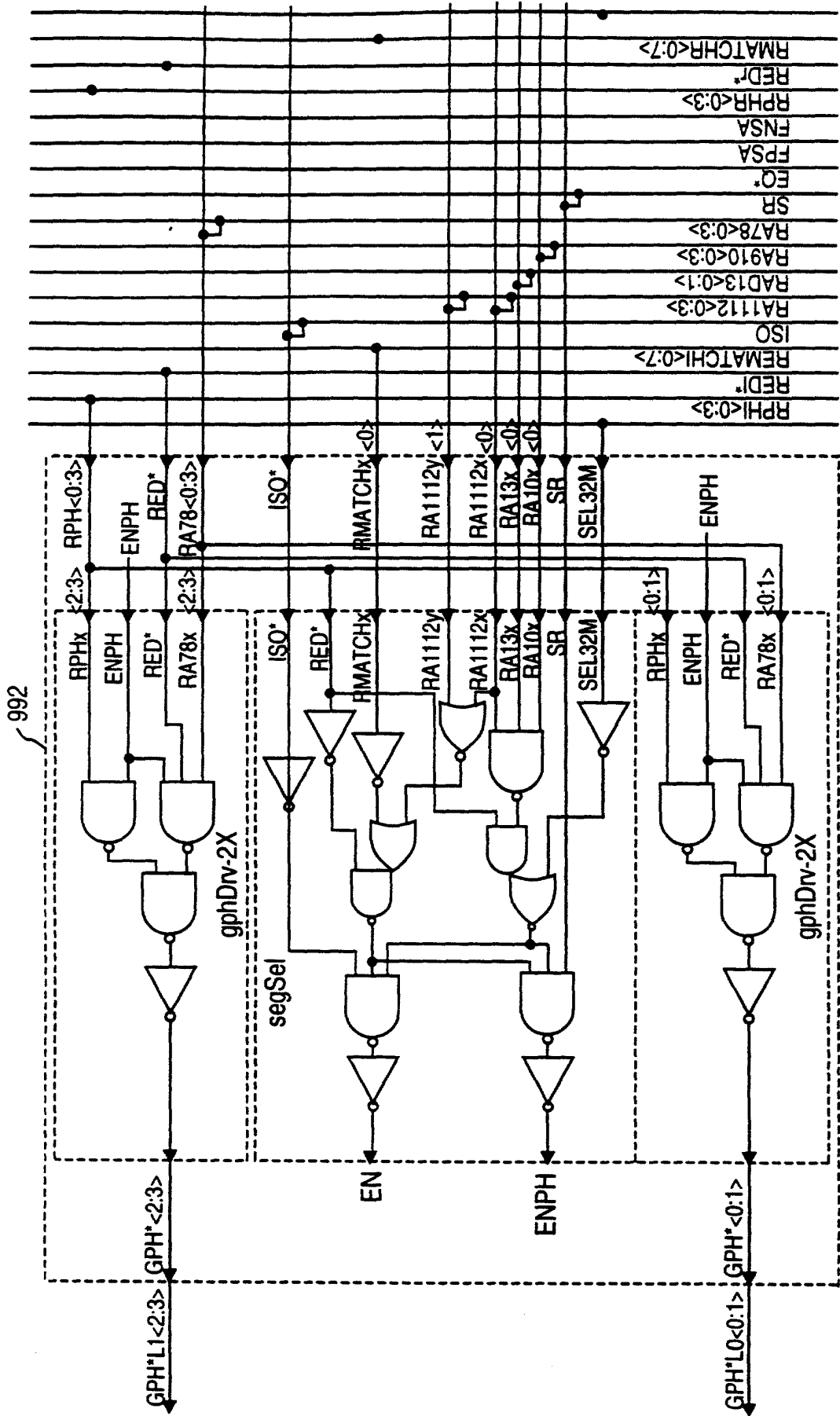


FIG. 61

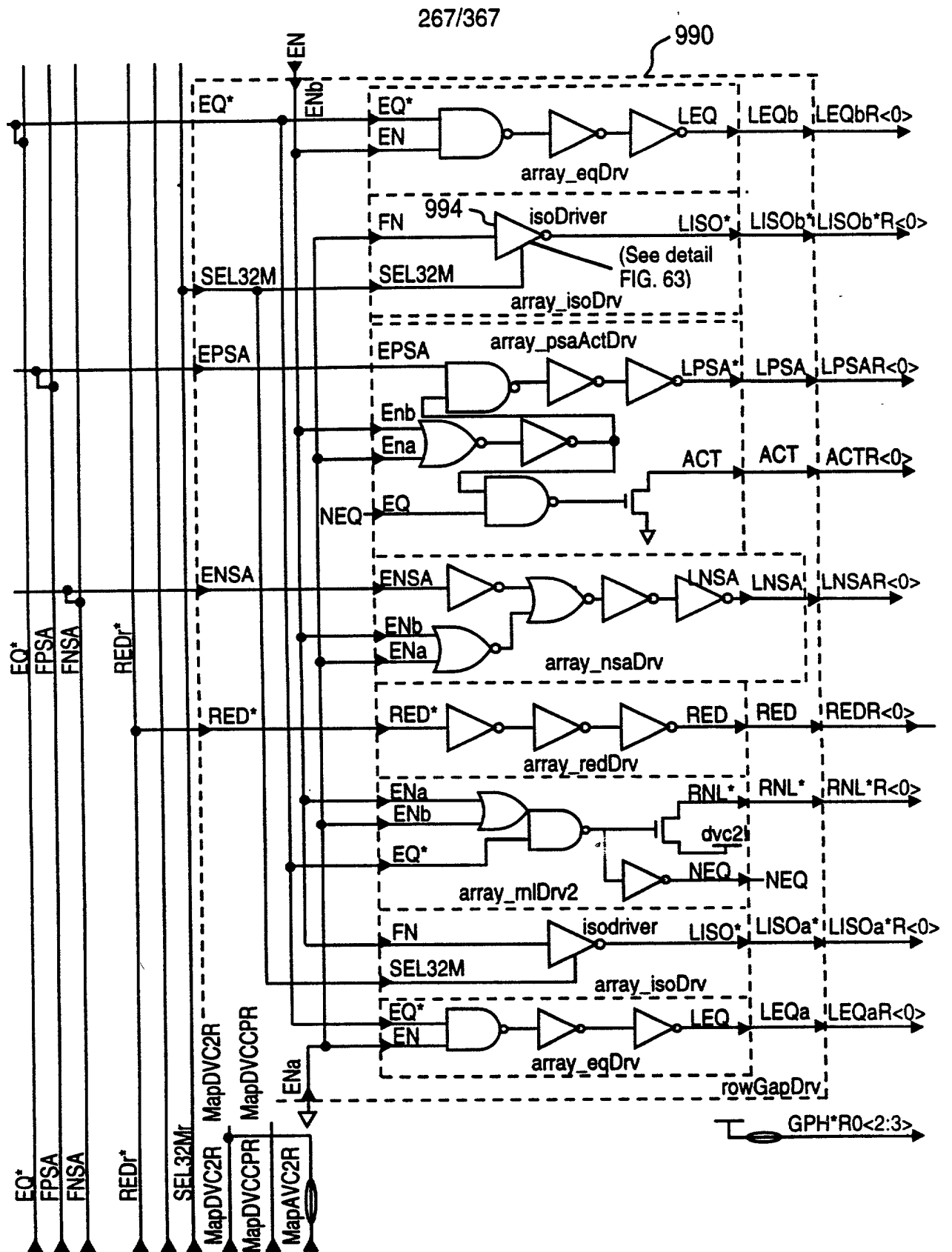


FIG. 62

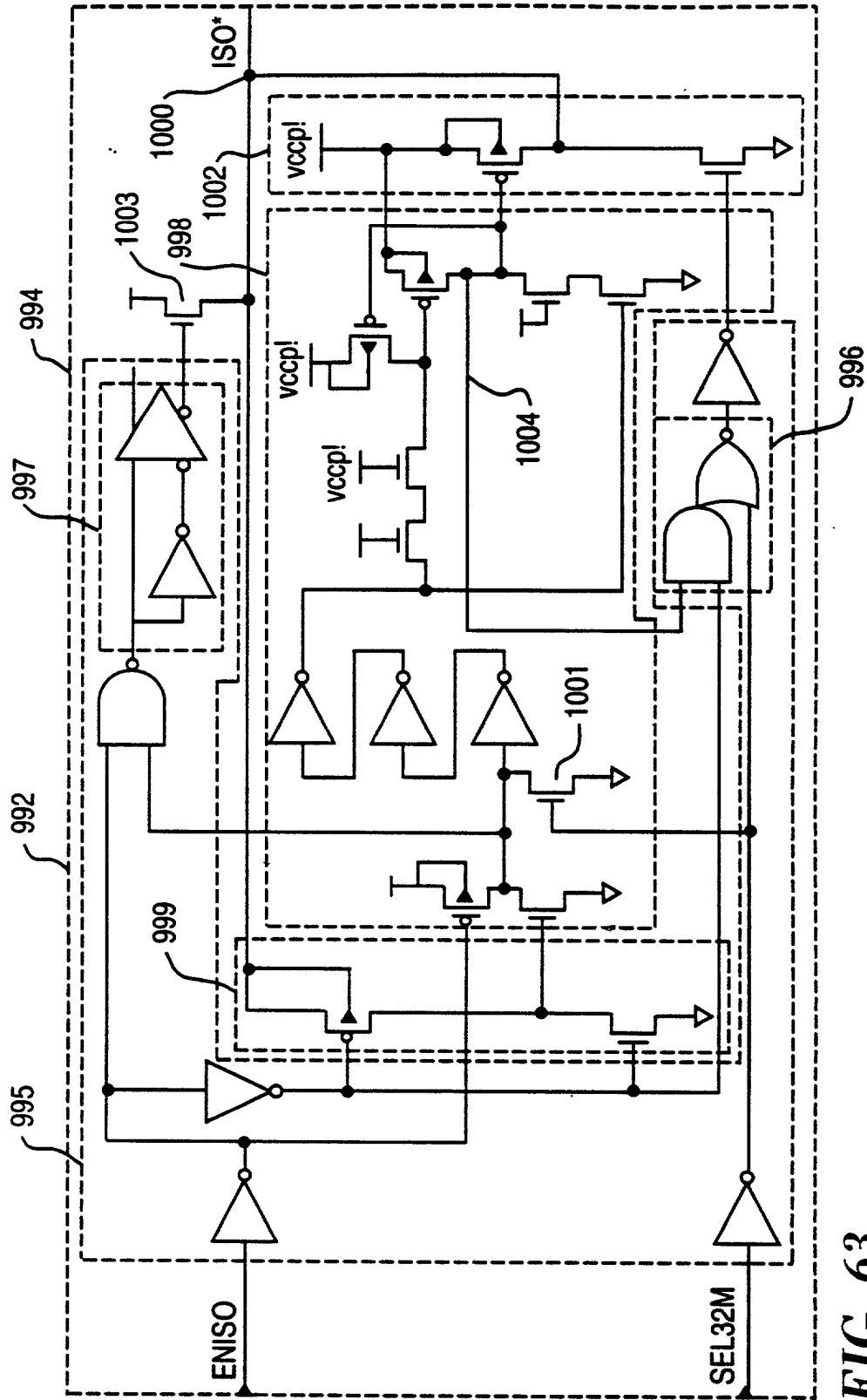


FIG. 63

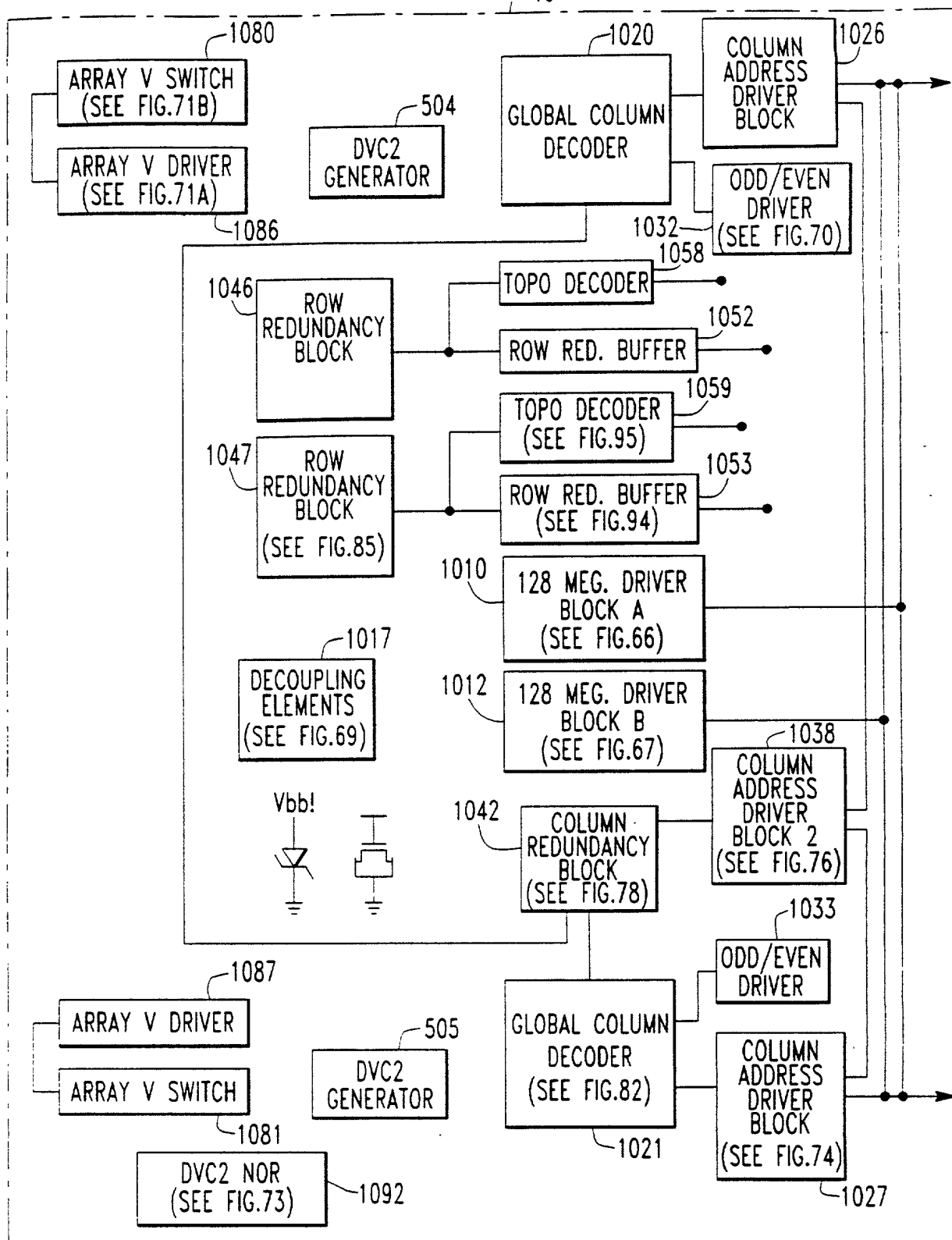


FIG. 64A

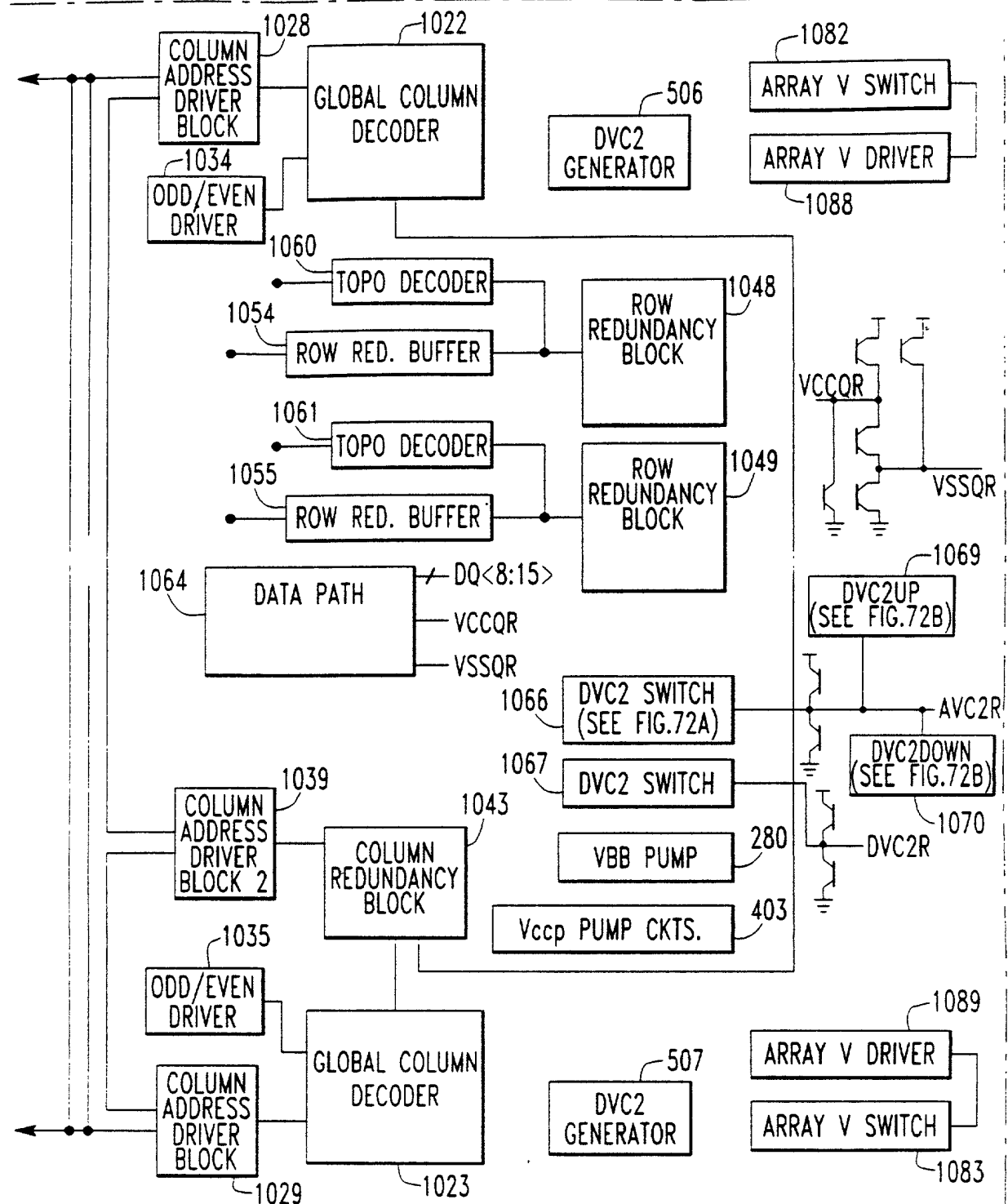


FIG. 64B

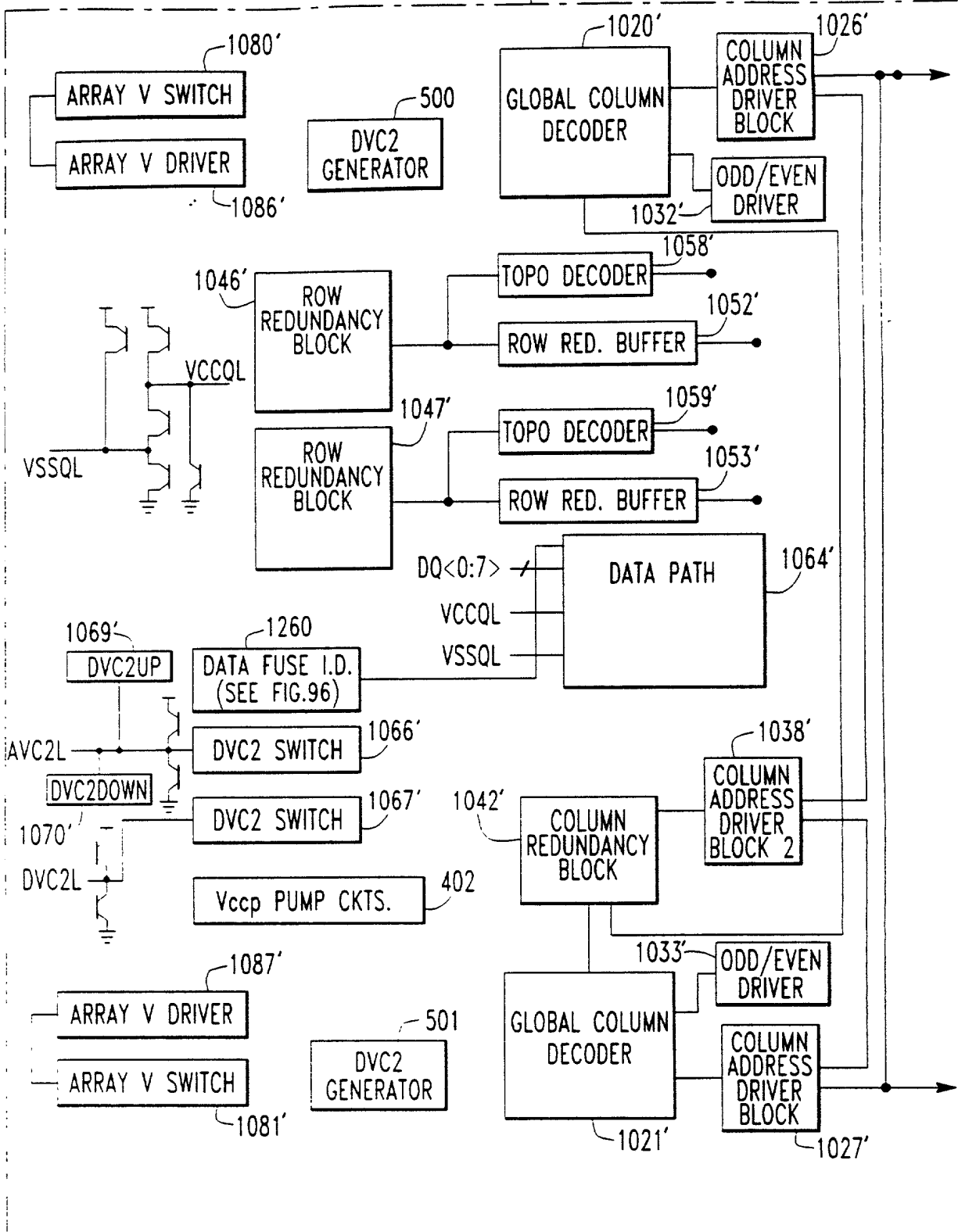


FIG. 65A

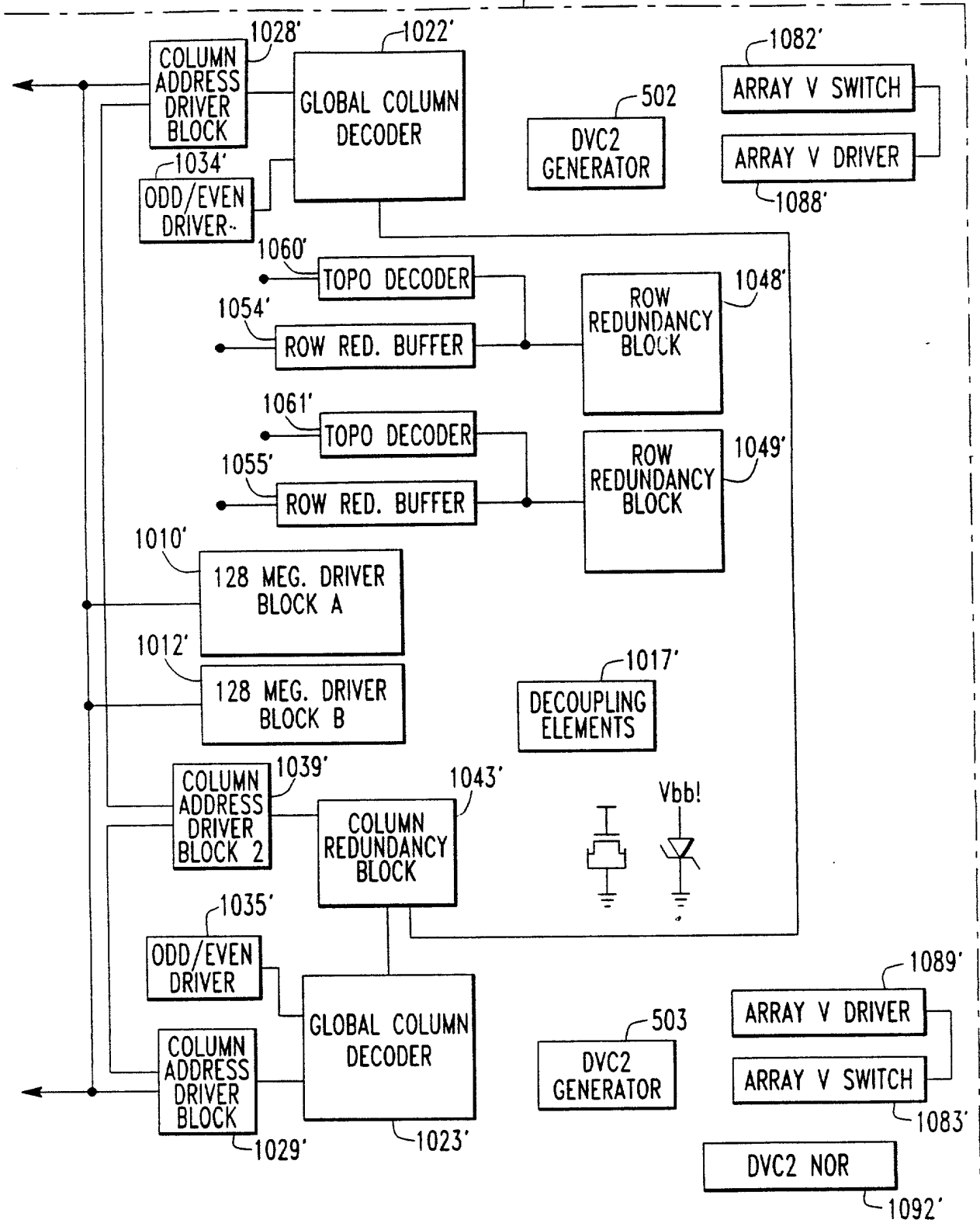


FIG. 65B



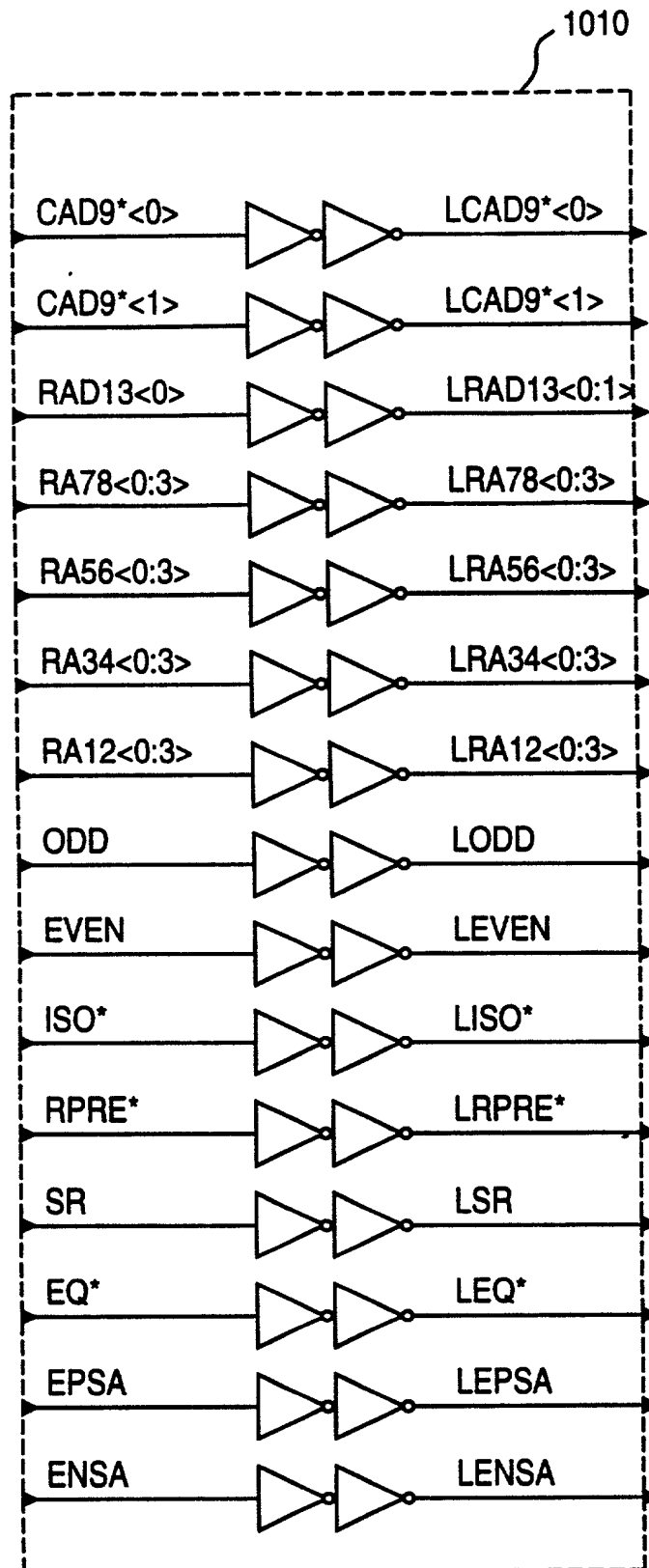


FIG. 66

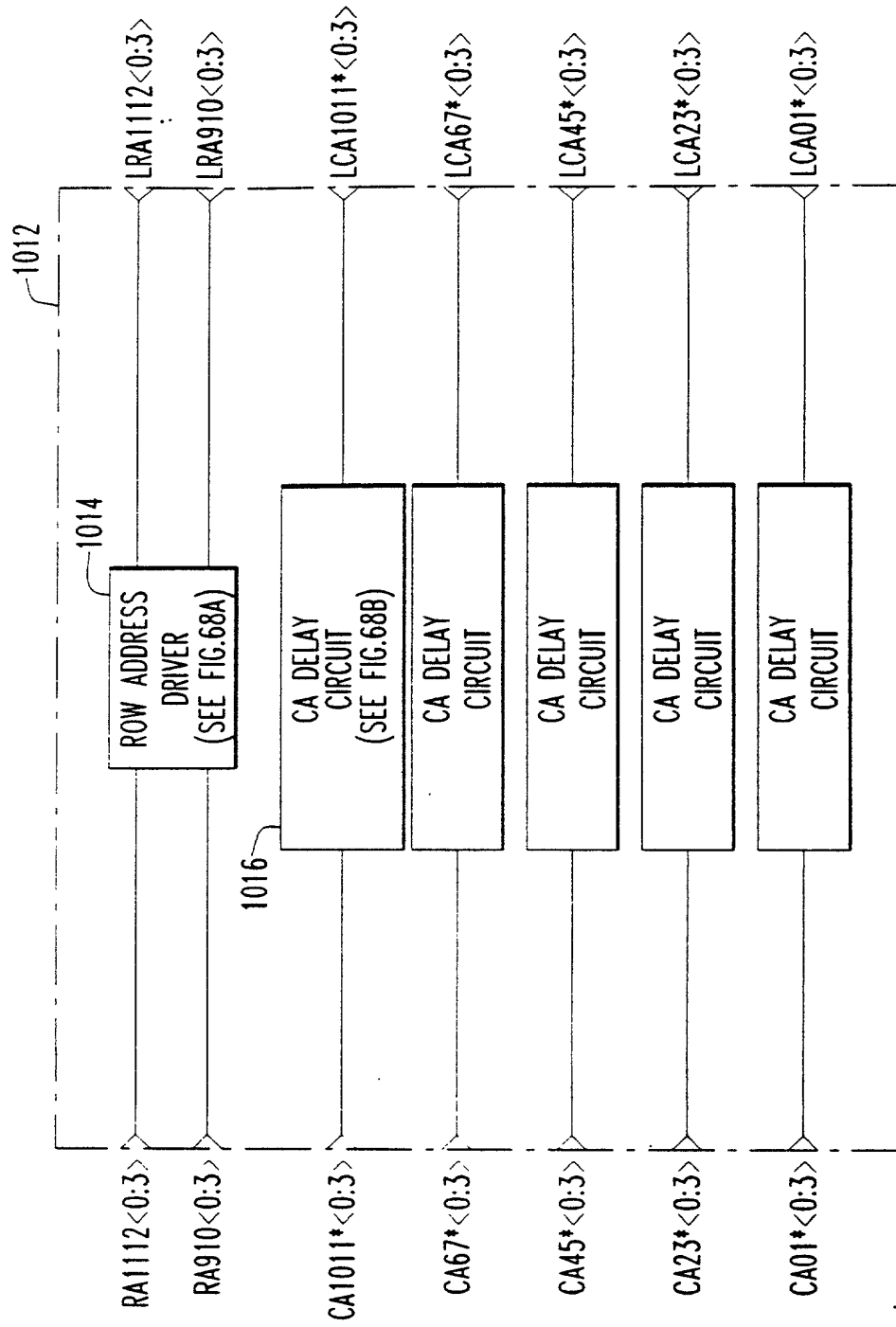
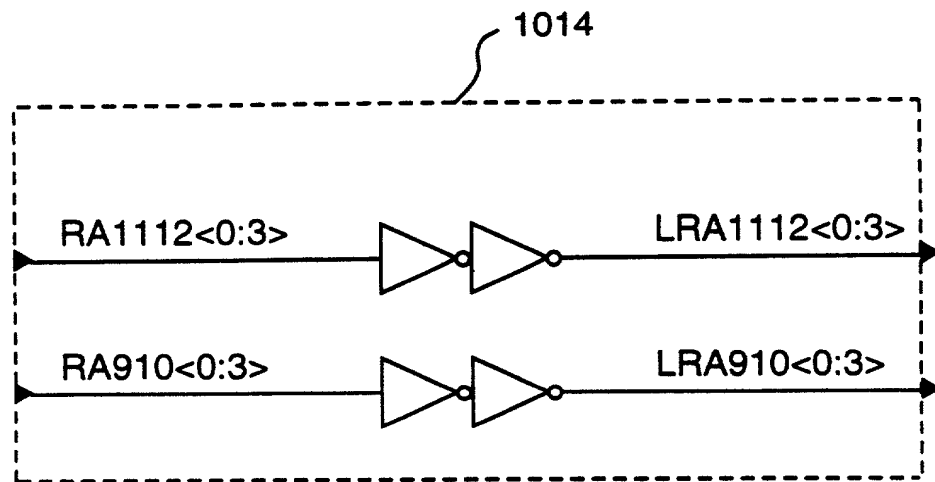
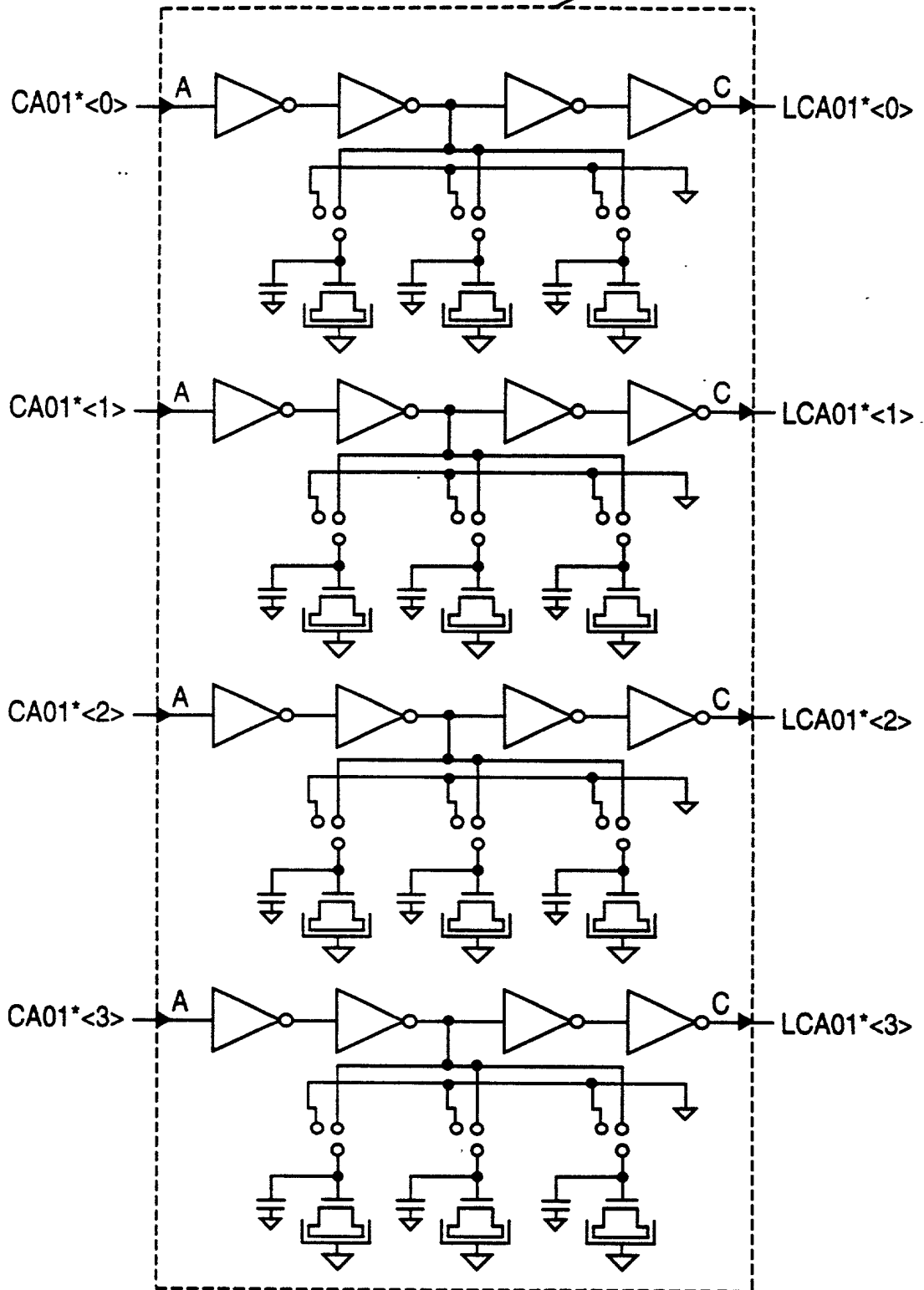
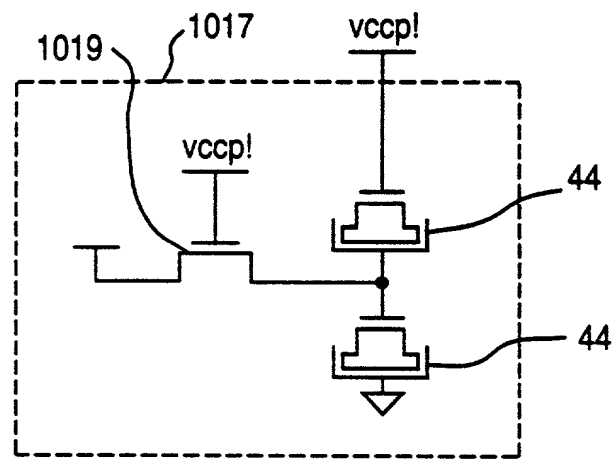


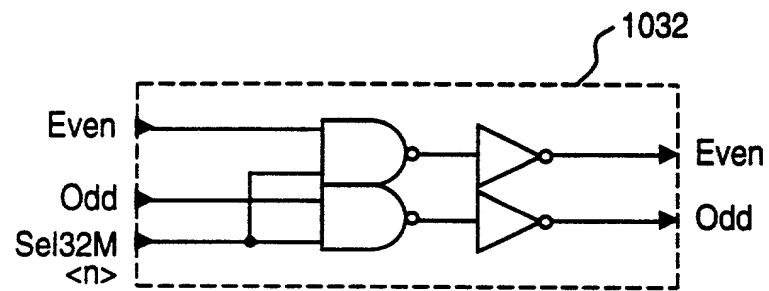
FIG. 67

**FIG. 68A**

**FIG. 68B**



**FIG. 69**



**FIG. 70**

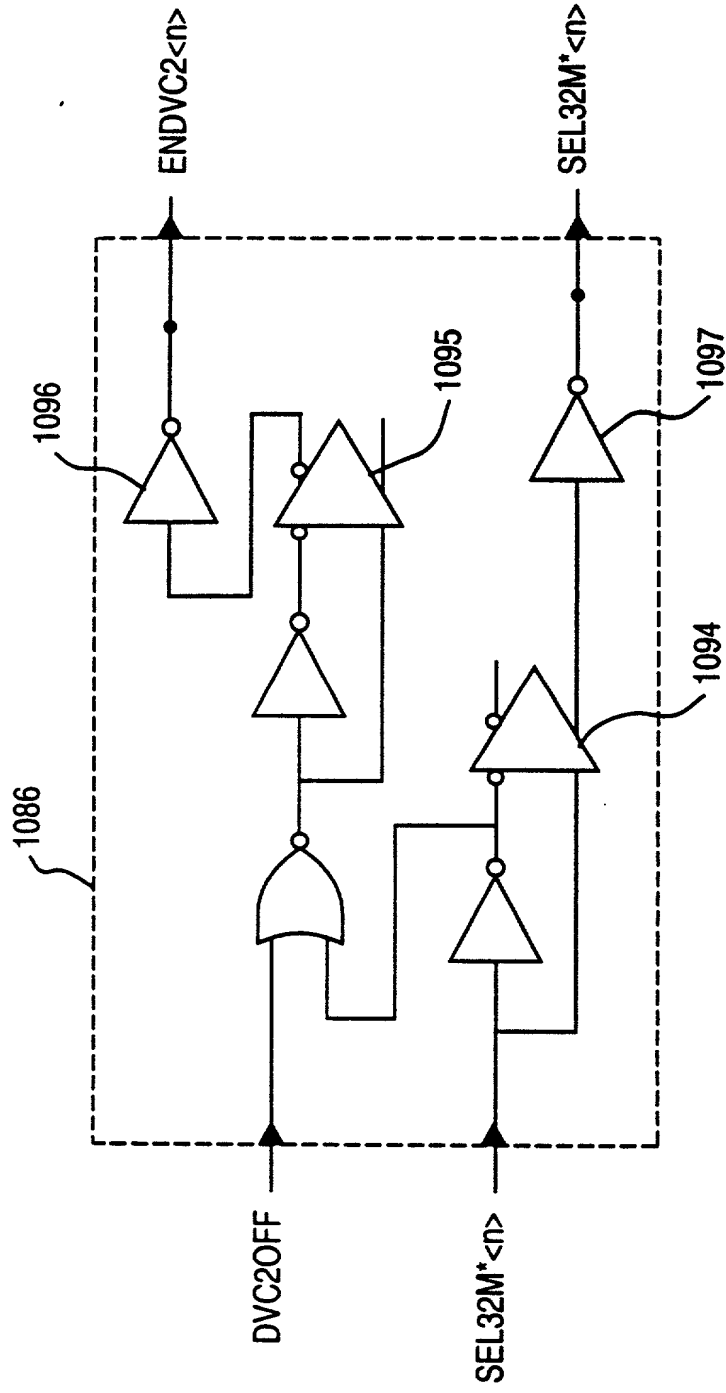
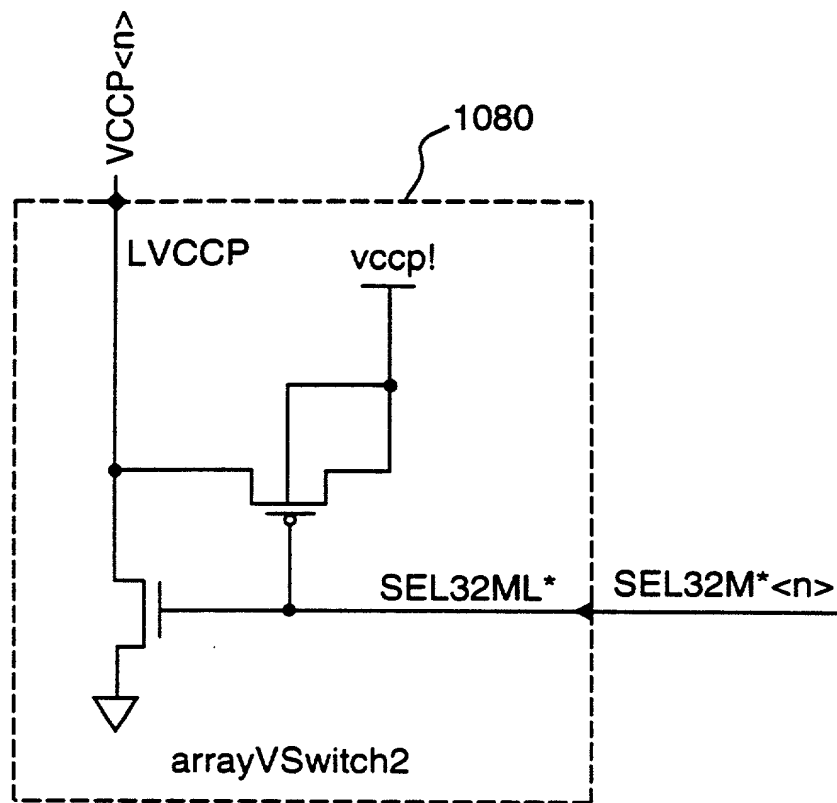


FIG. 71A



**FIG. 71B**



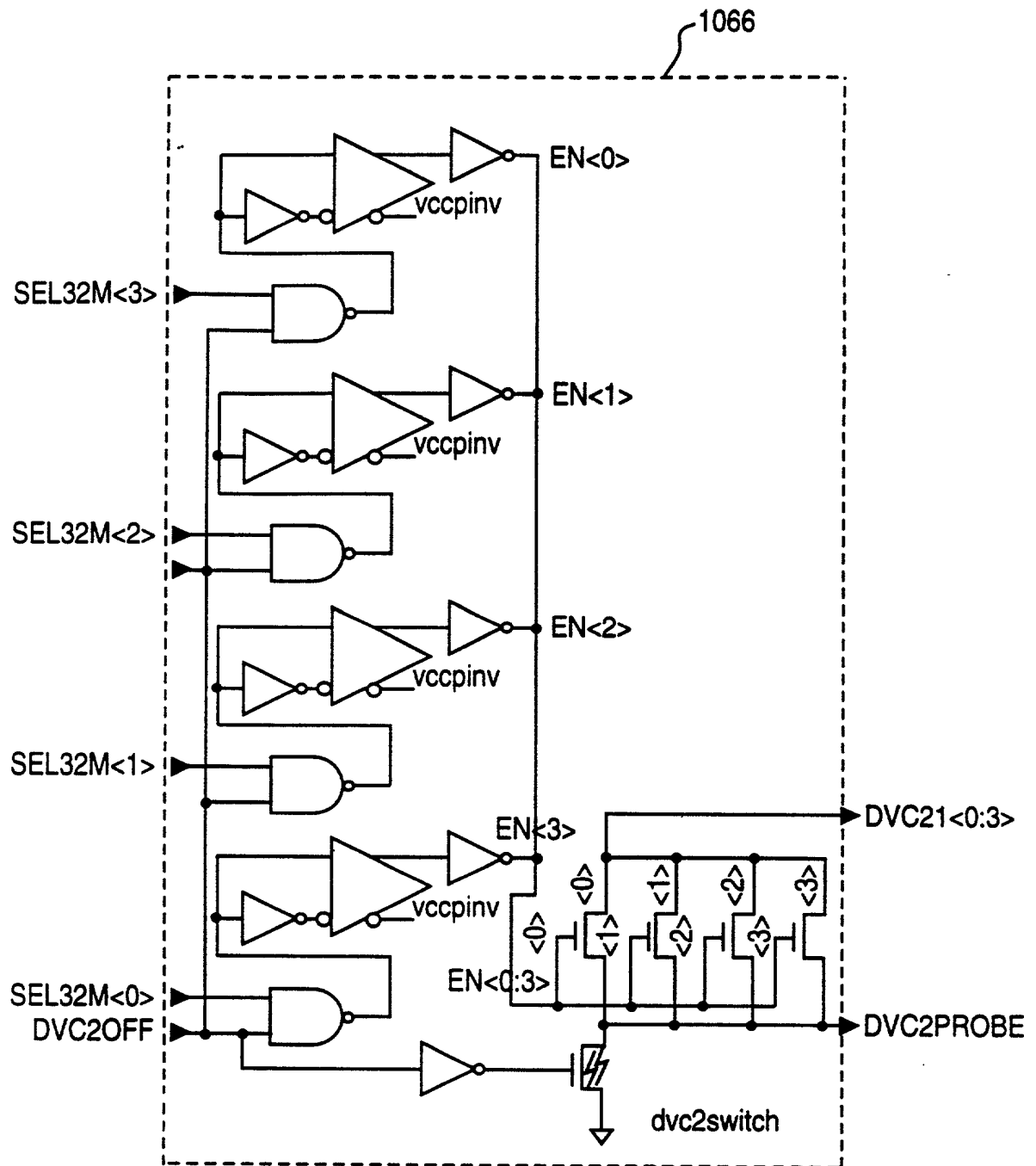
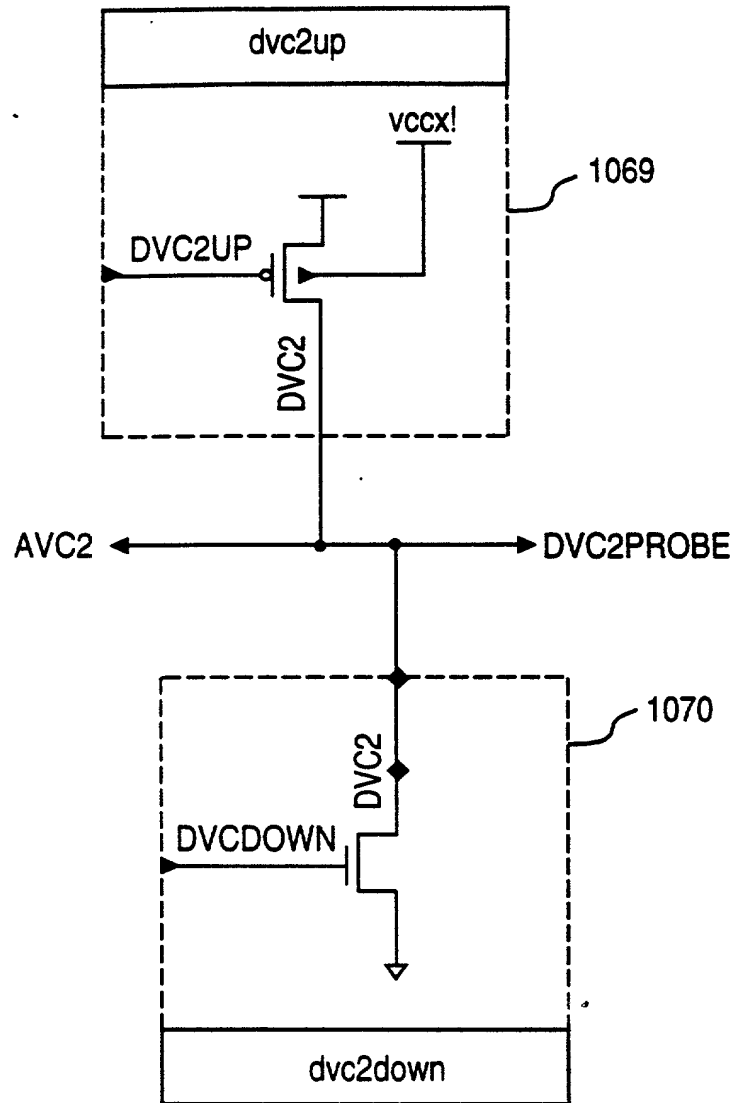
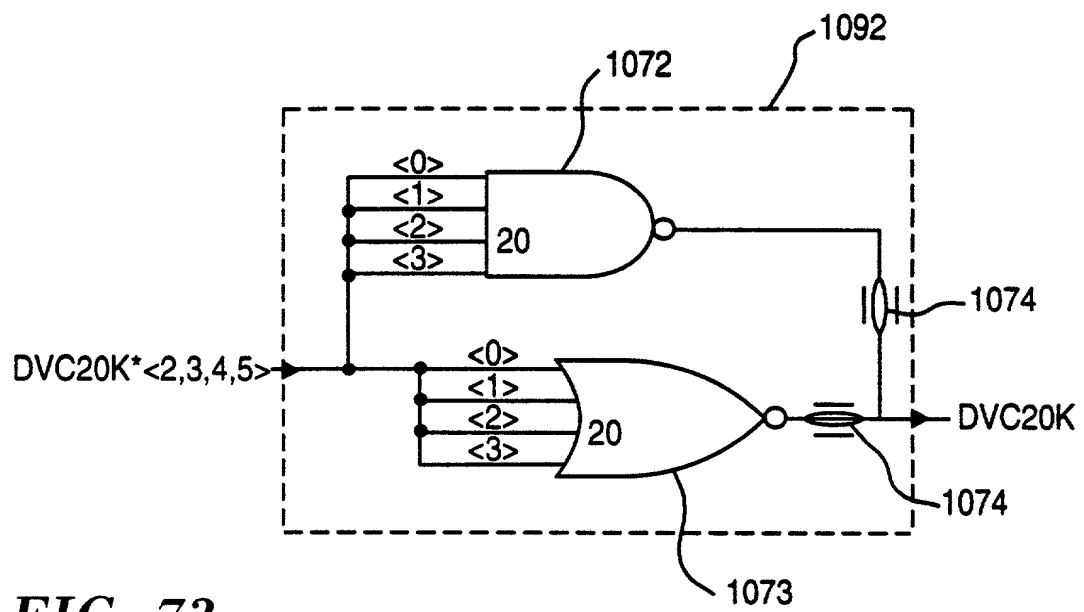


FIG. 72A

**FIG. 72B**

**FIG. 73**

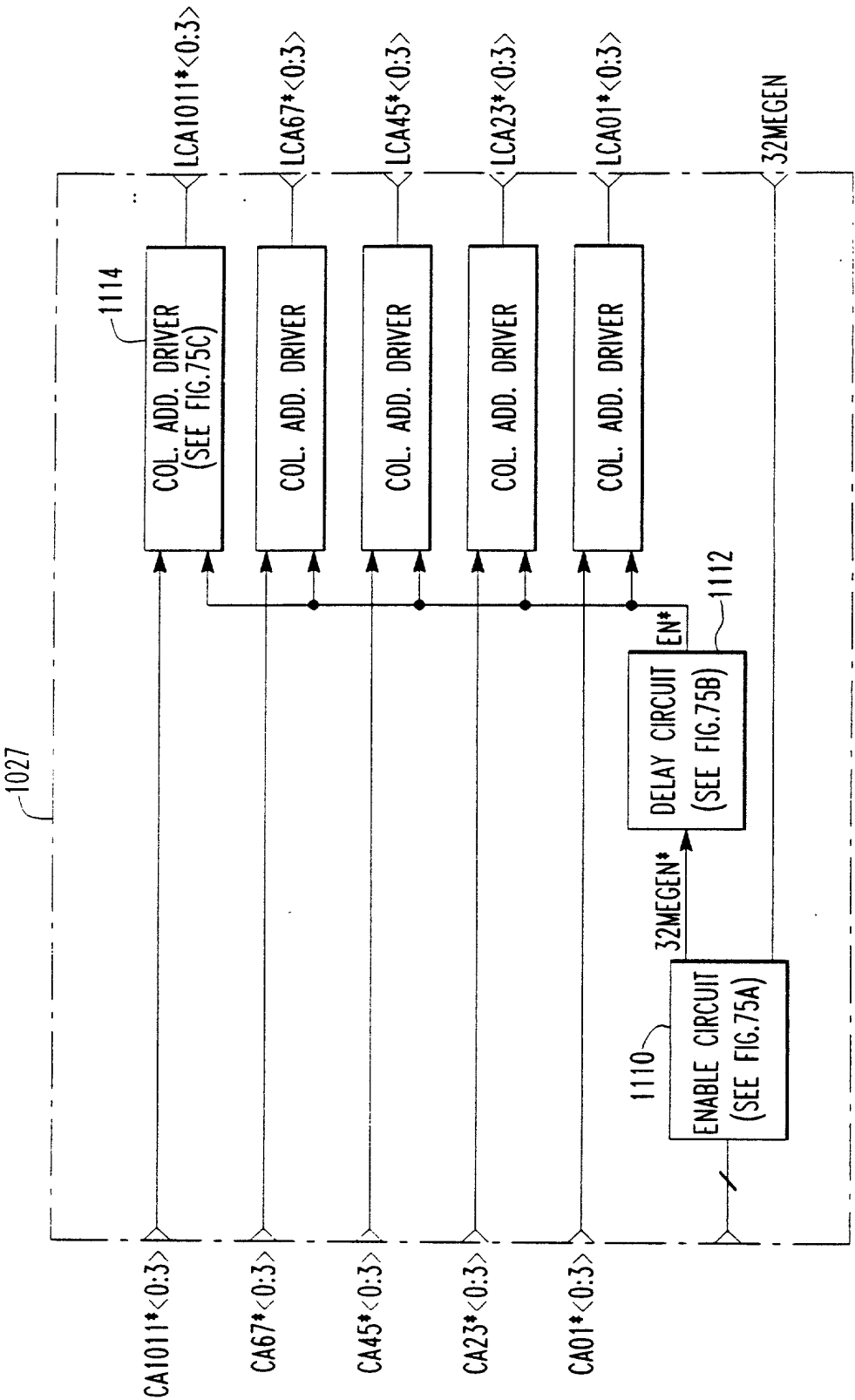
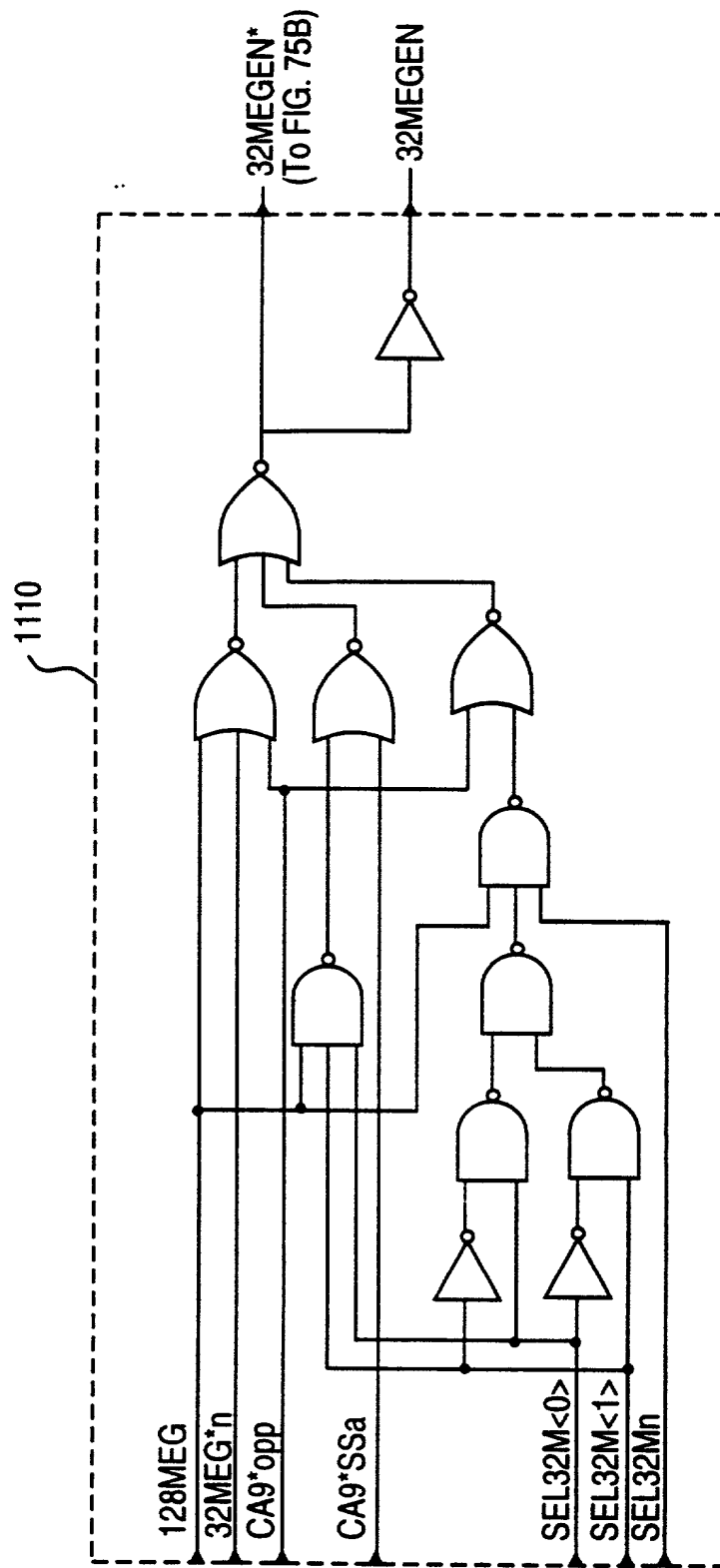


FIG. 74



**FIG. 75A**

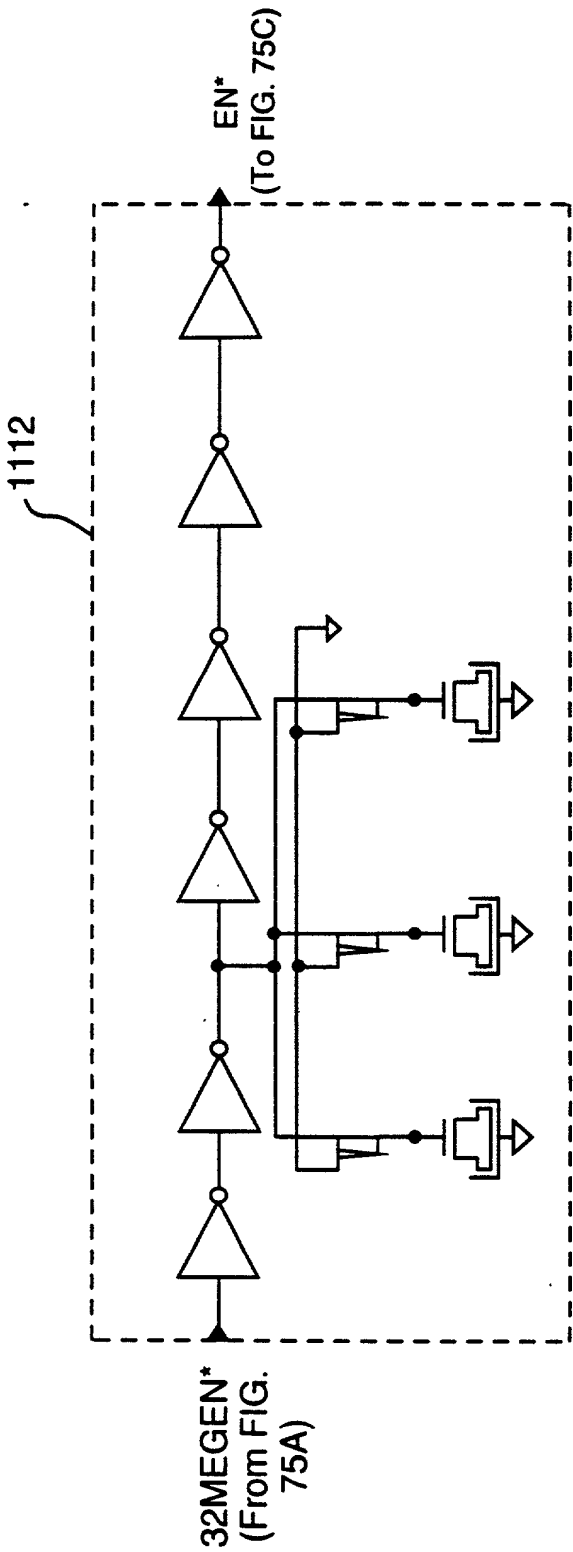


FIG. 75B

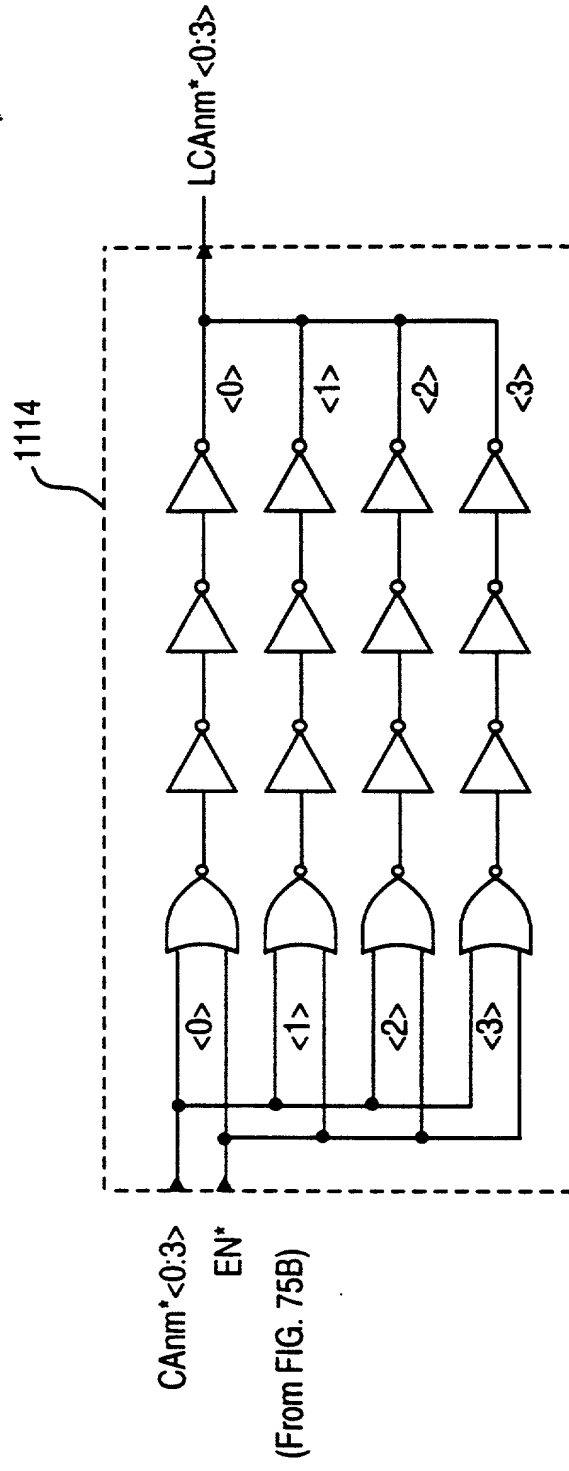


FIG. 75C

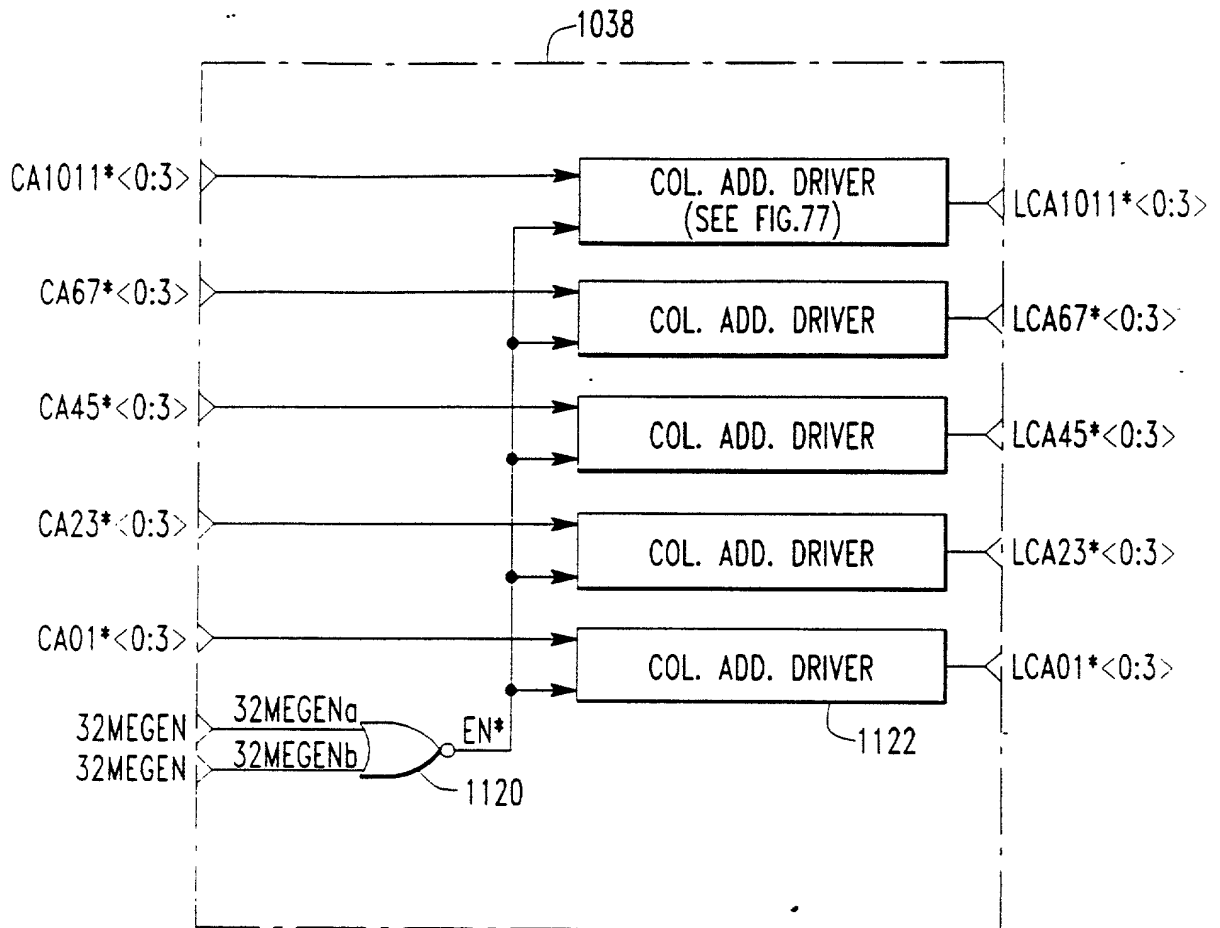


FIG. 76



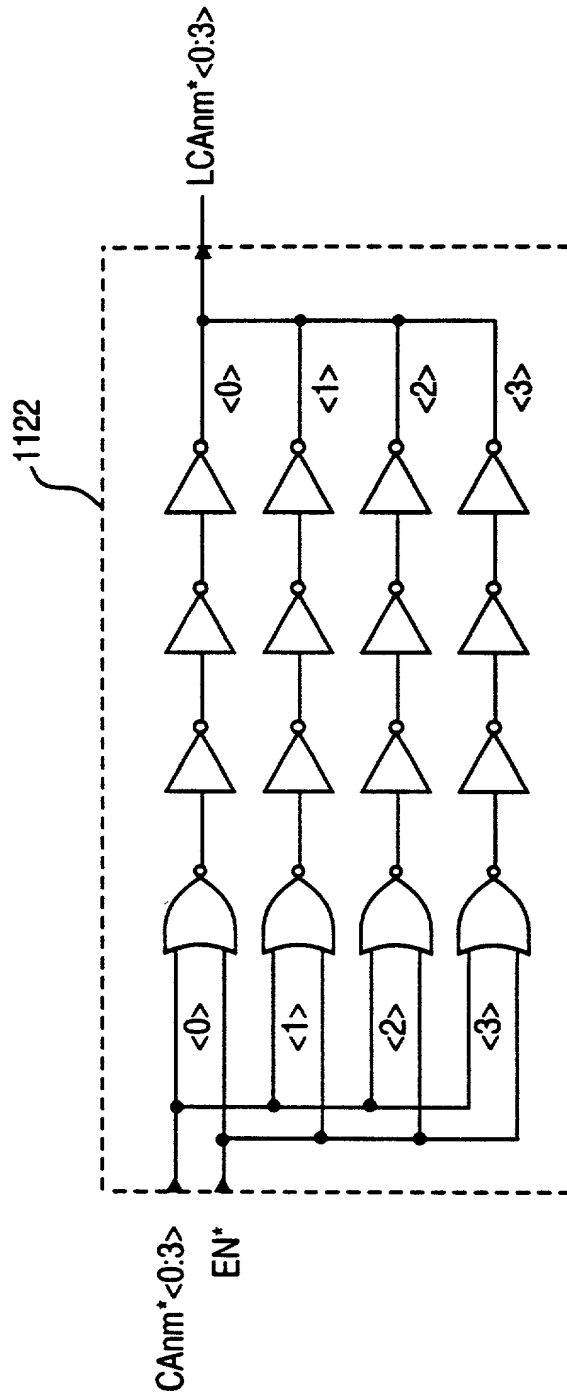


FIG. 77

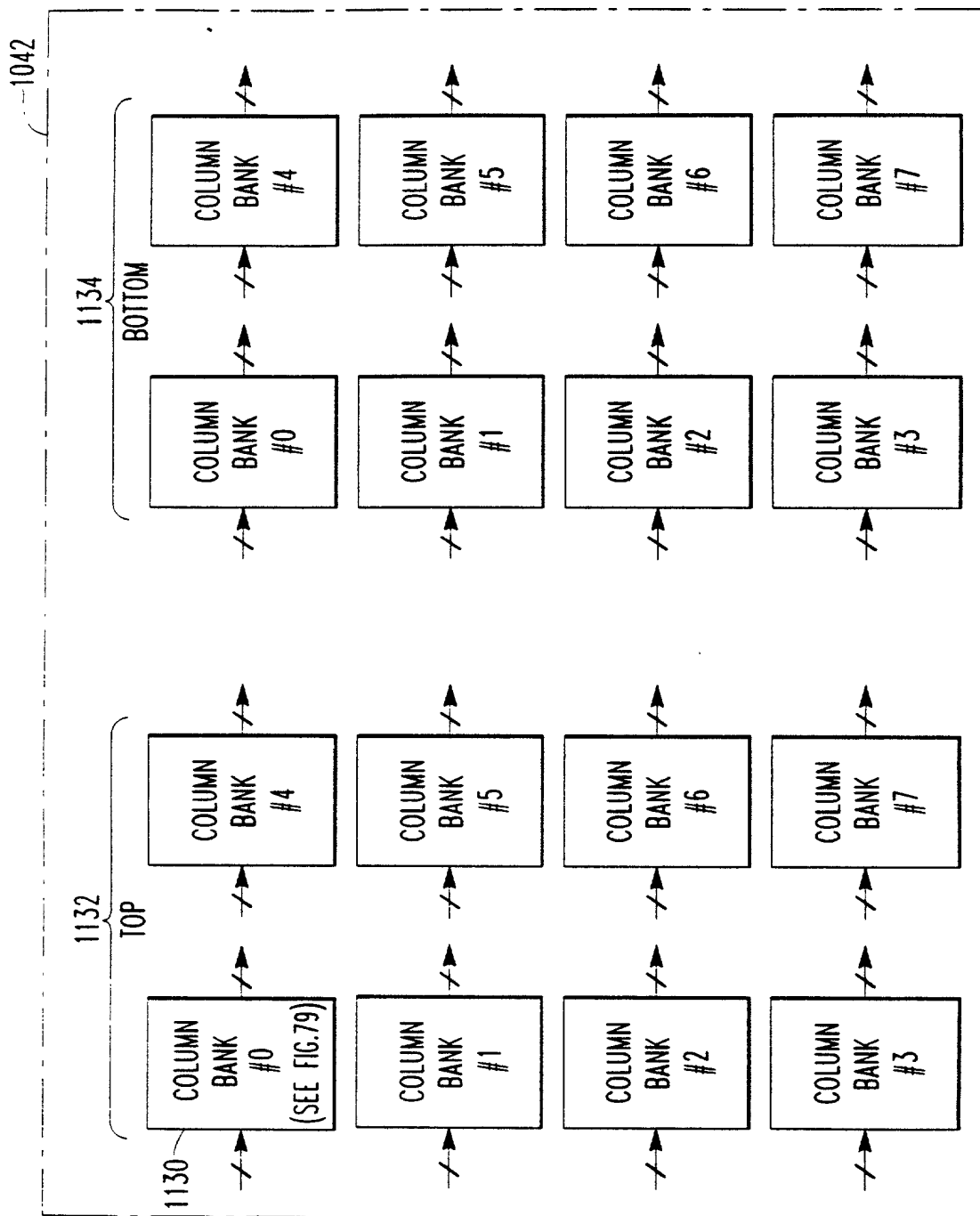
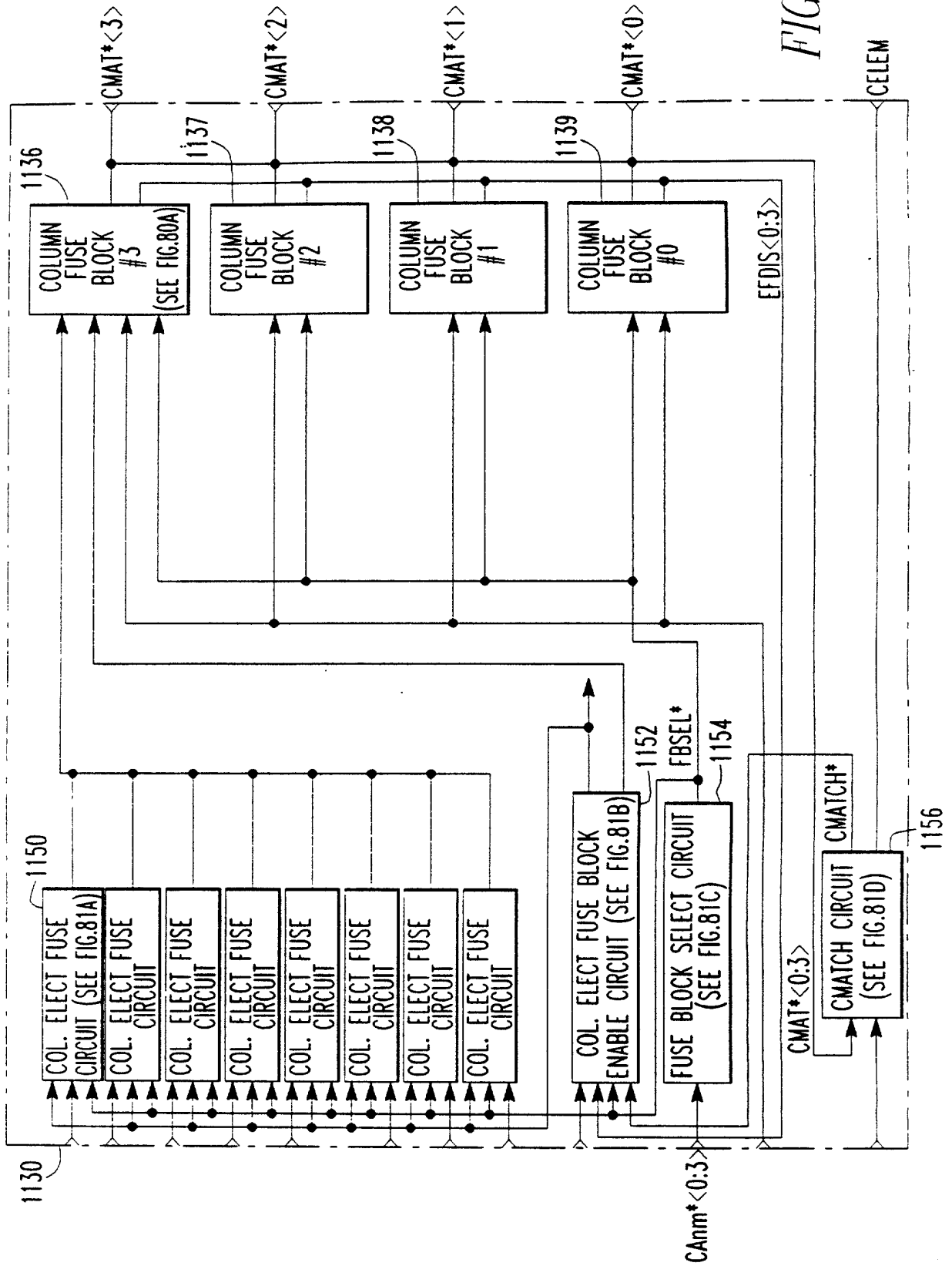


FIG. 78

FIG. 79



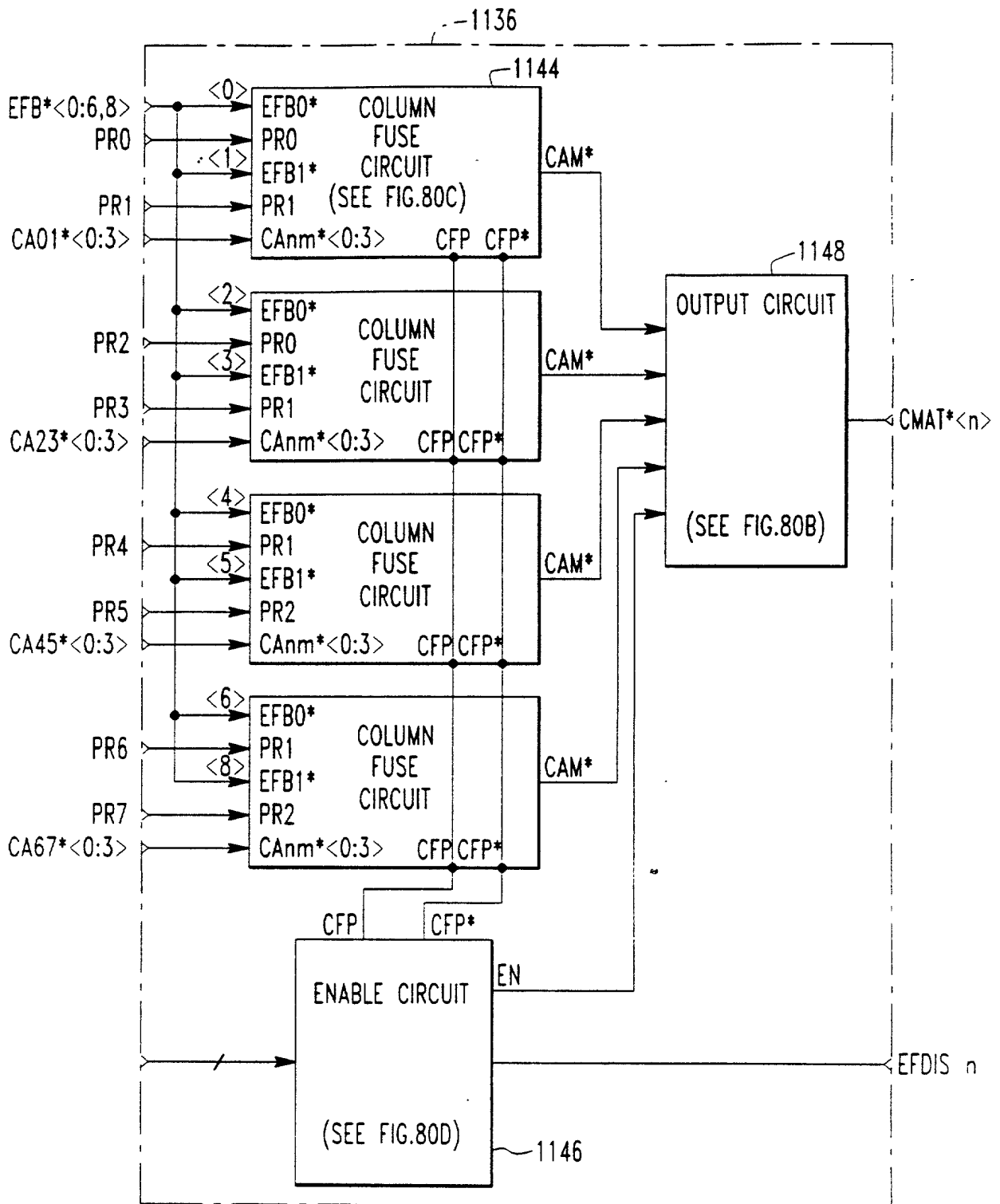
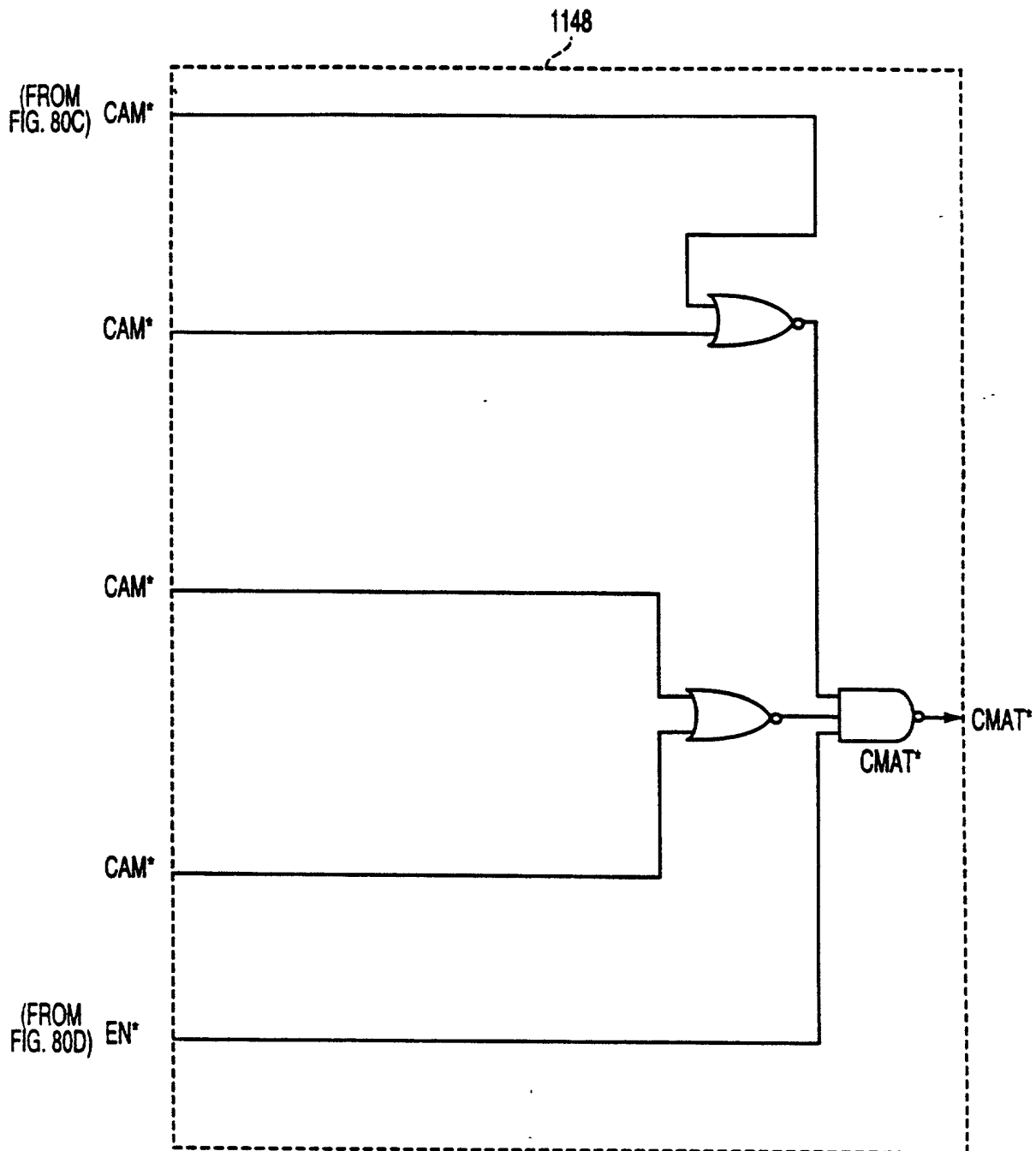


FIG. 80A

**FIG. 80B**

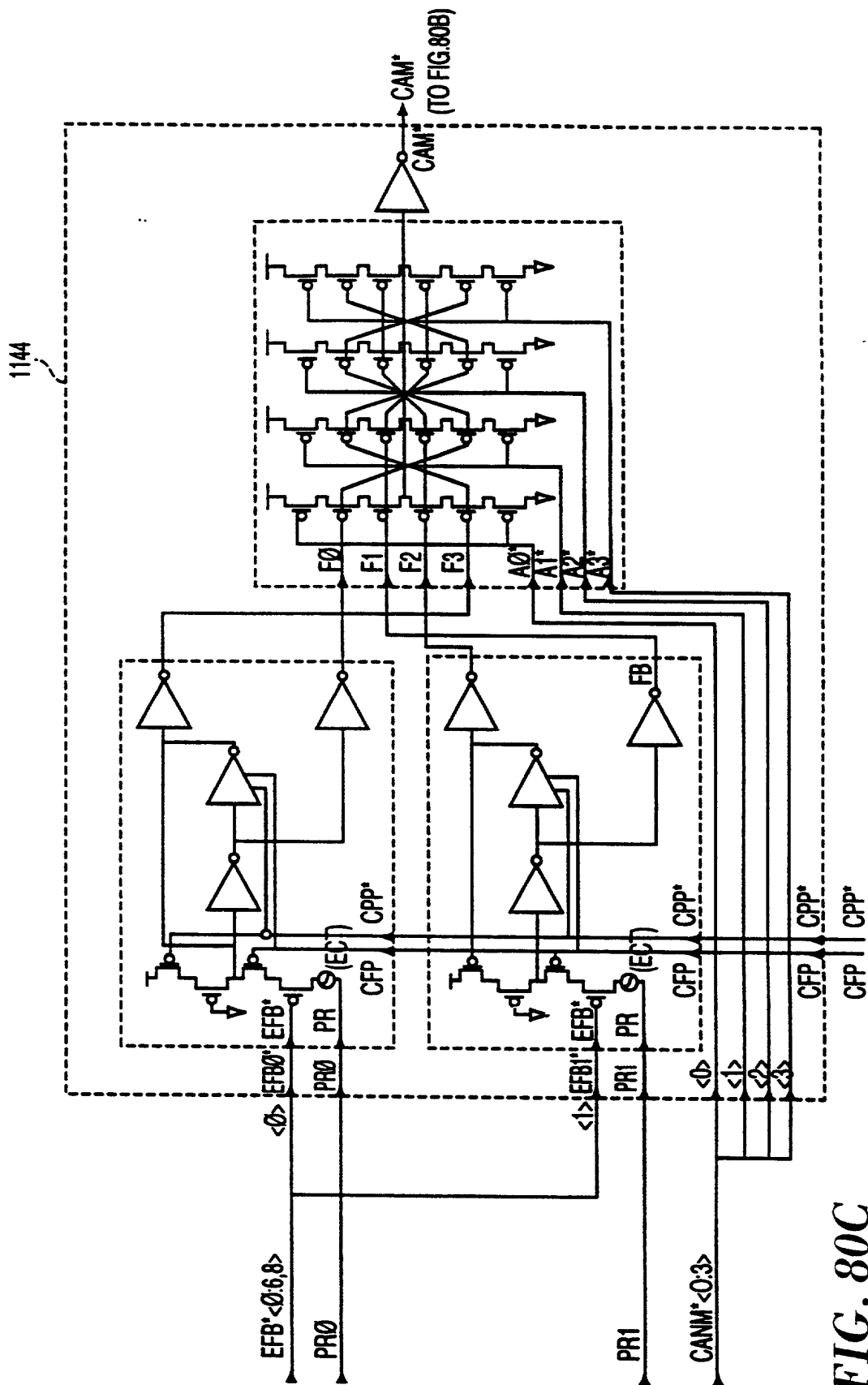
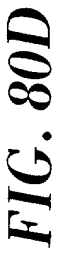


FIG. 80C



(TO  
FIG. 808)

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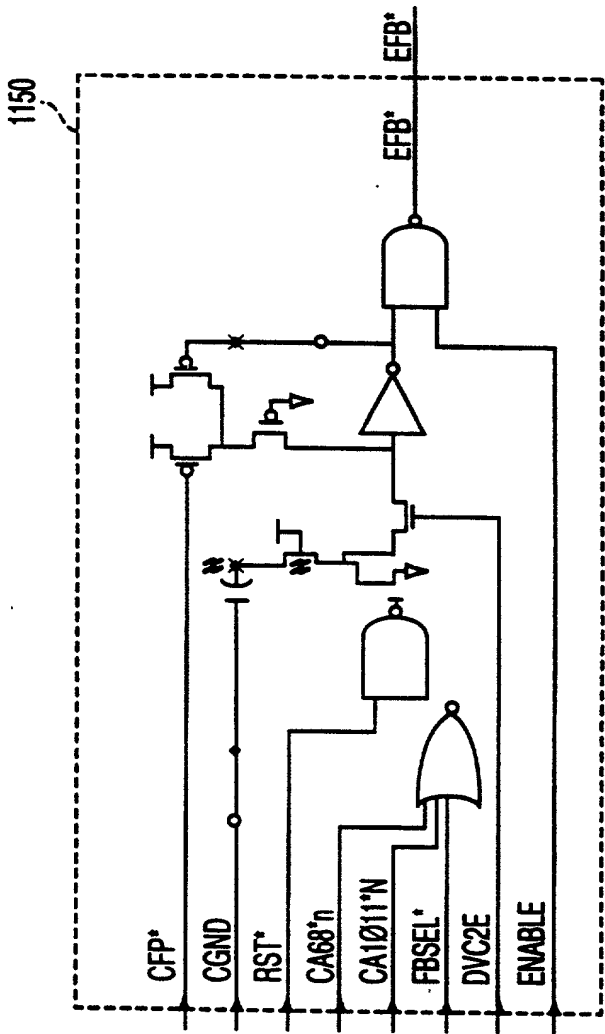


FIG. 81A



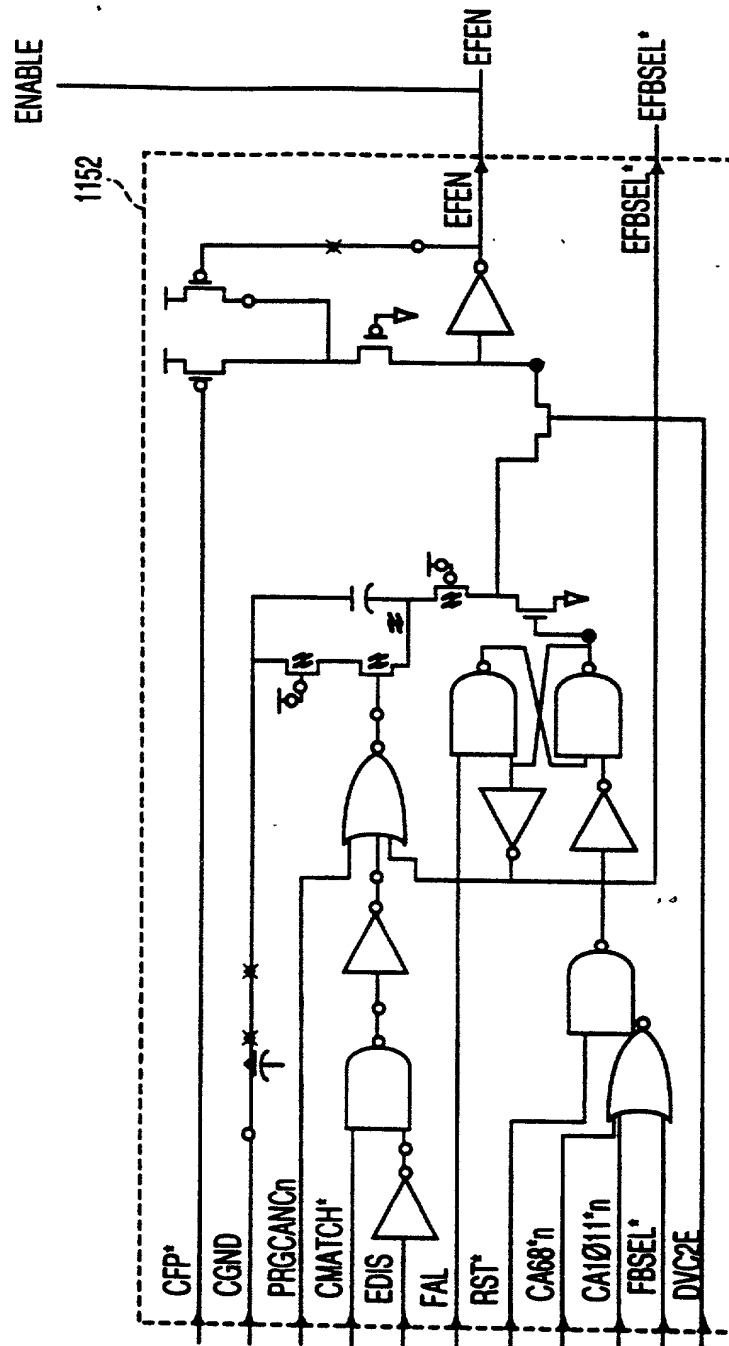


FIG. 81B

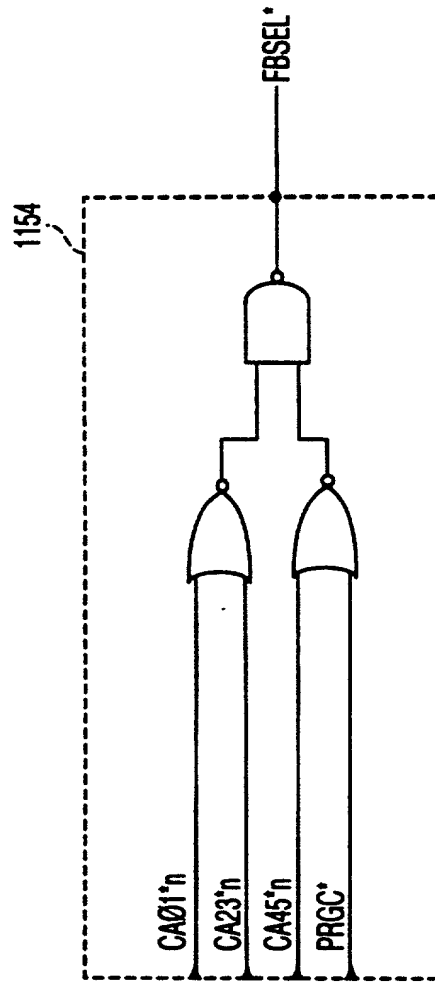


FIG. 81C

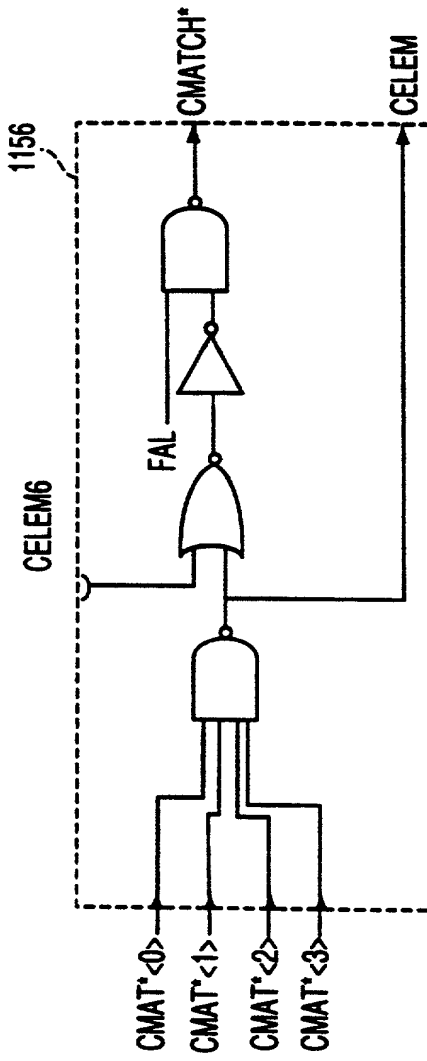
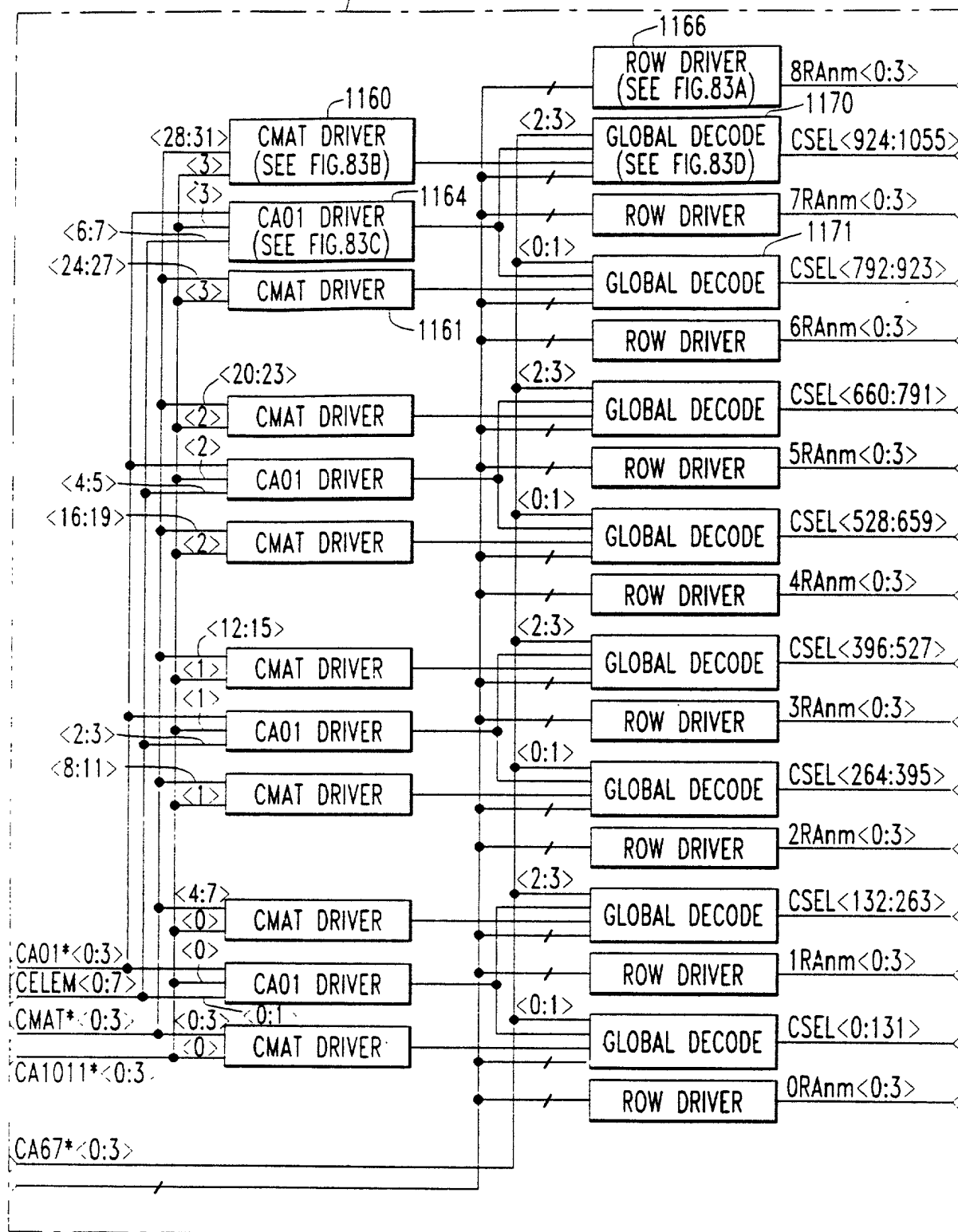


FIG. 81D



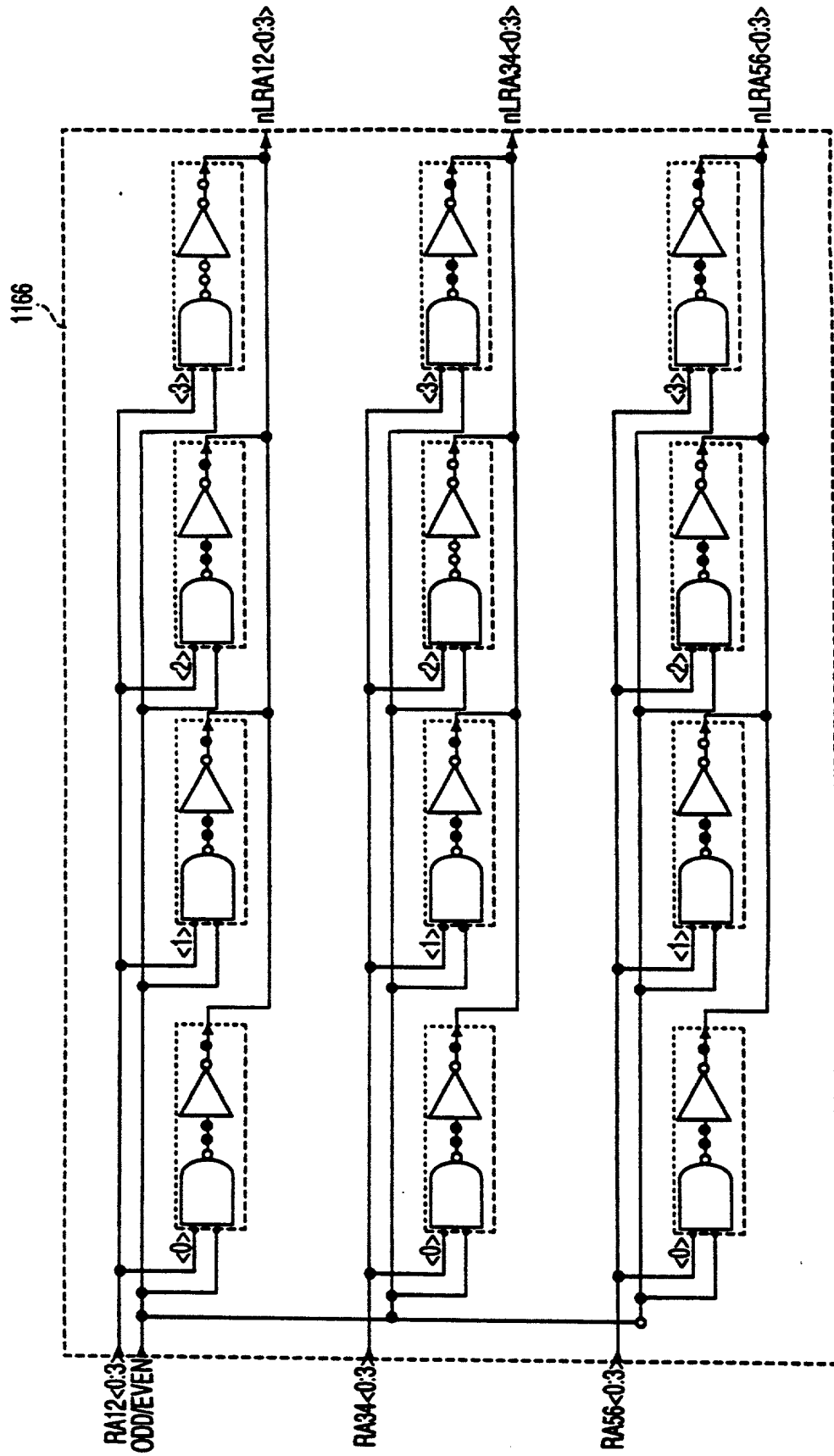


FIG. 83A

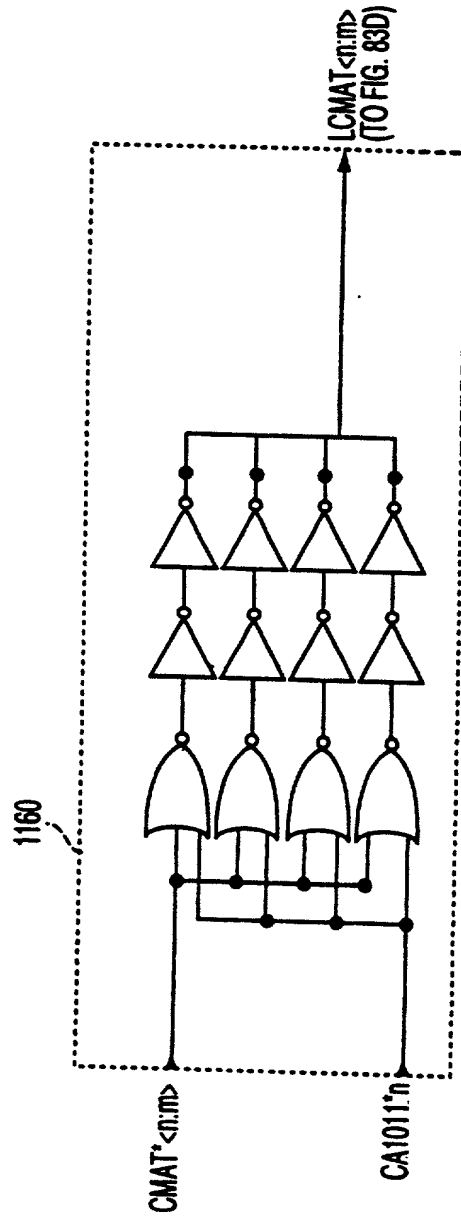


FIG. 83B

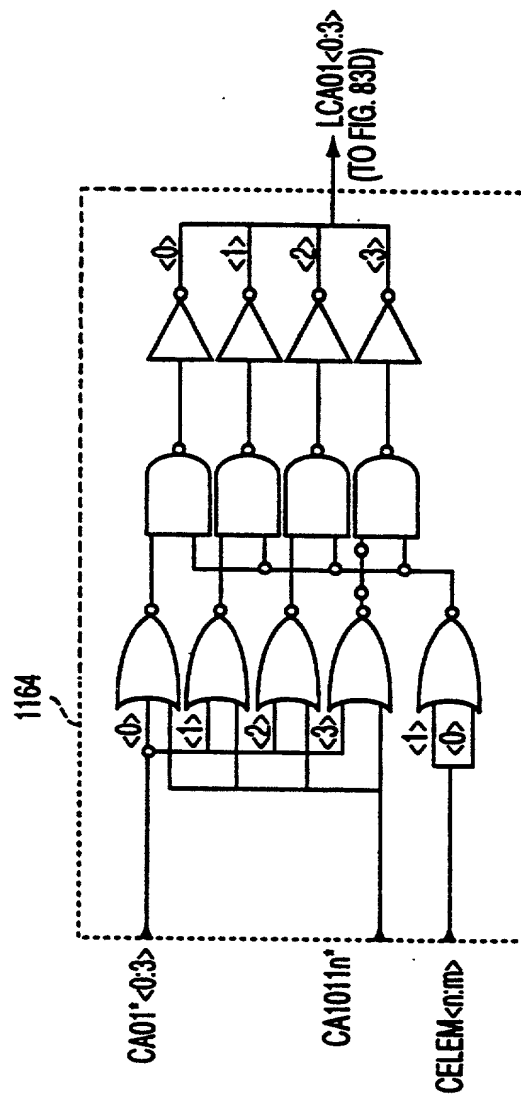


FIG. 83C





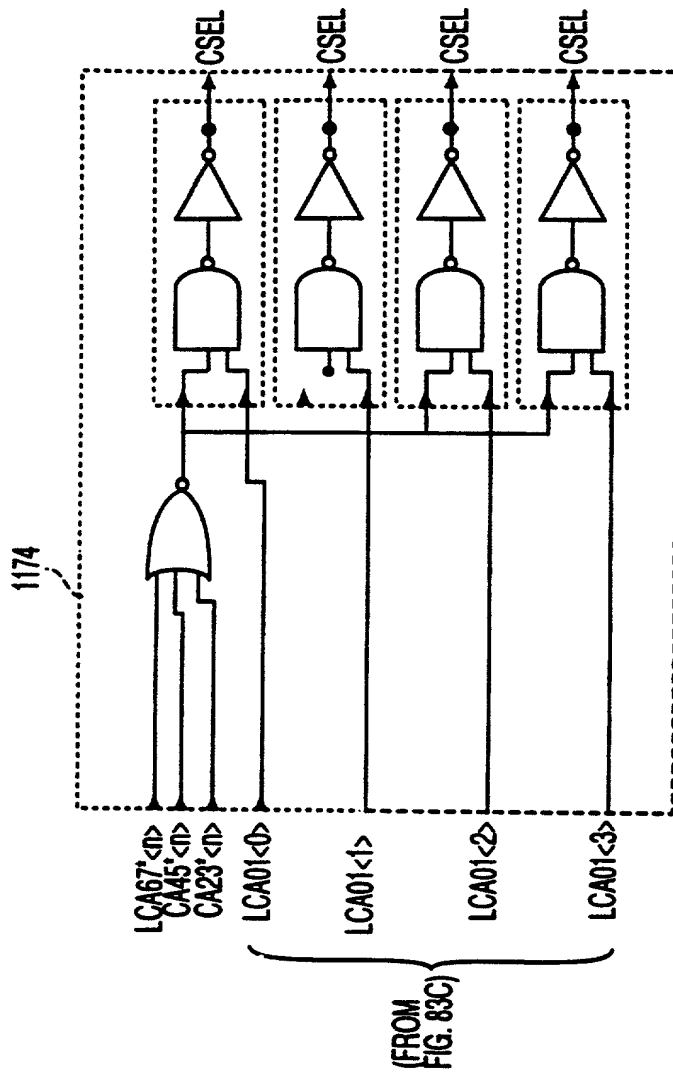
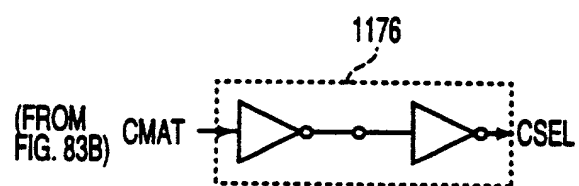


FIG. 84A

**FIG. 84B**

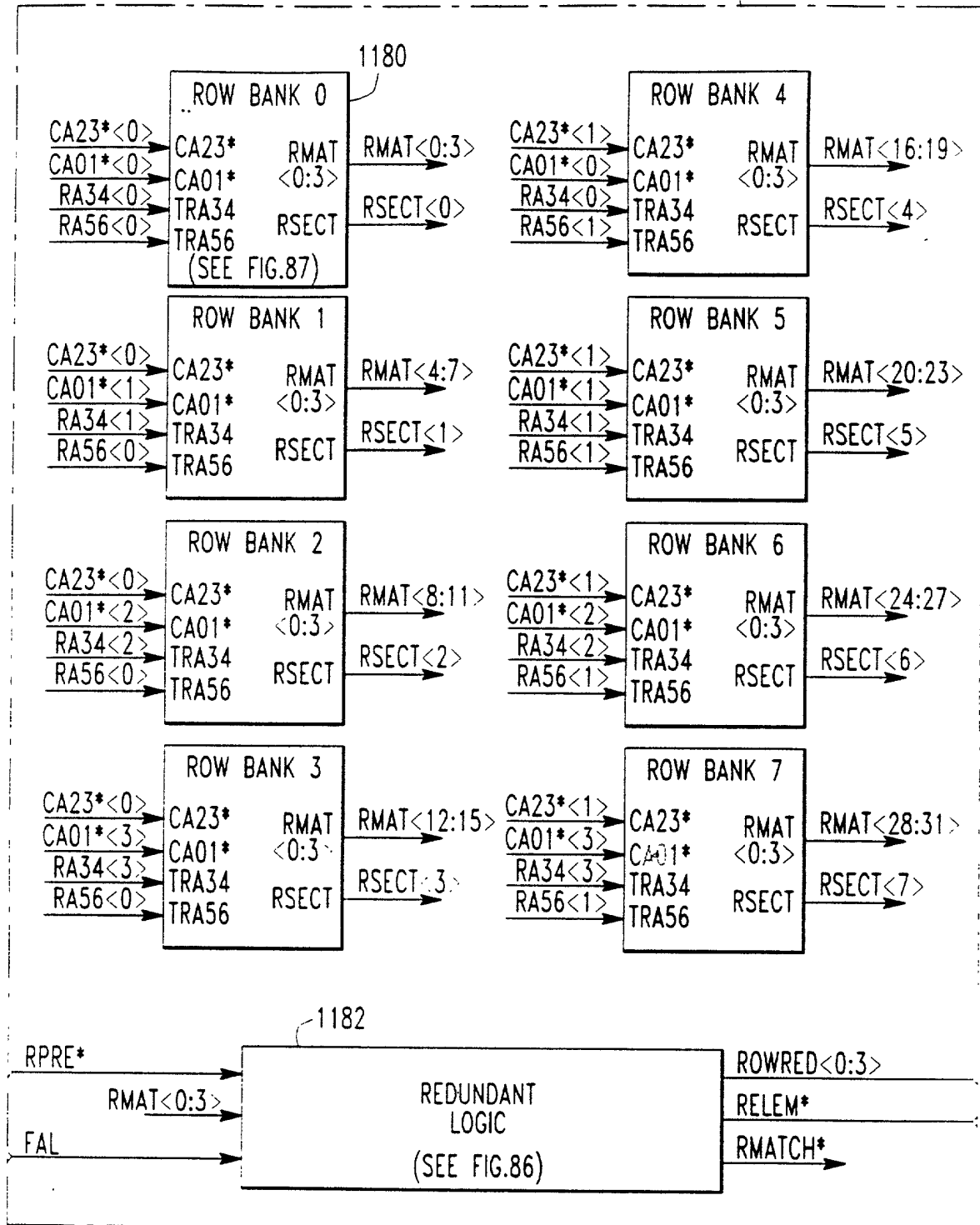


FIG. 85



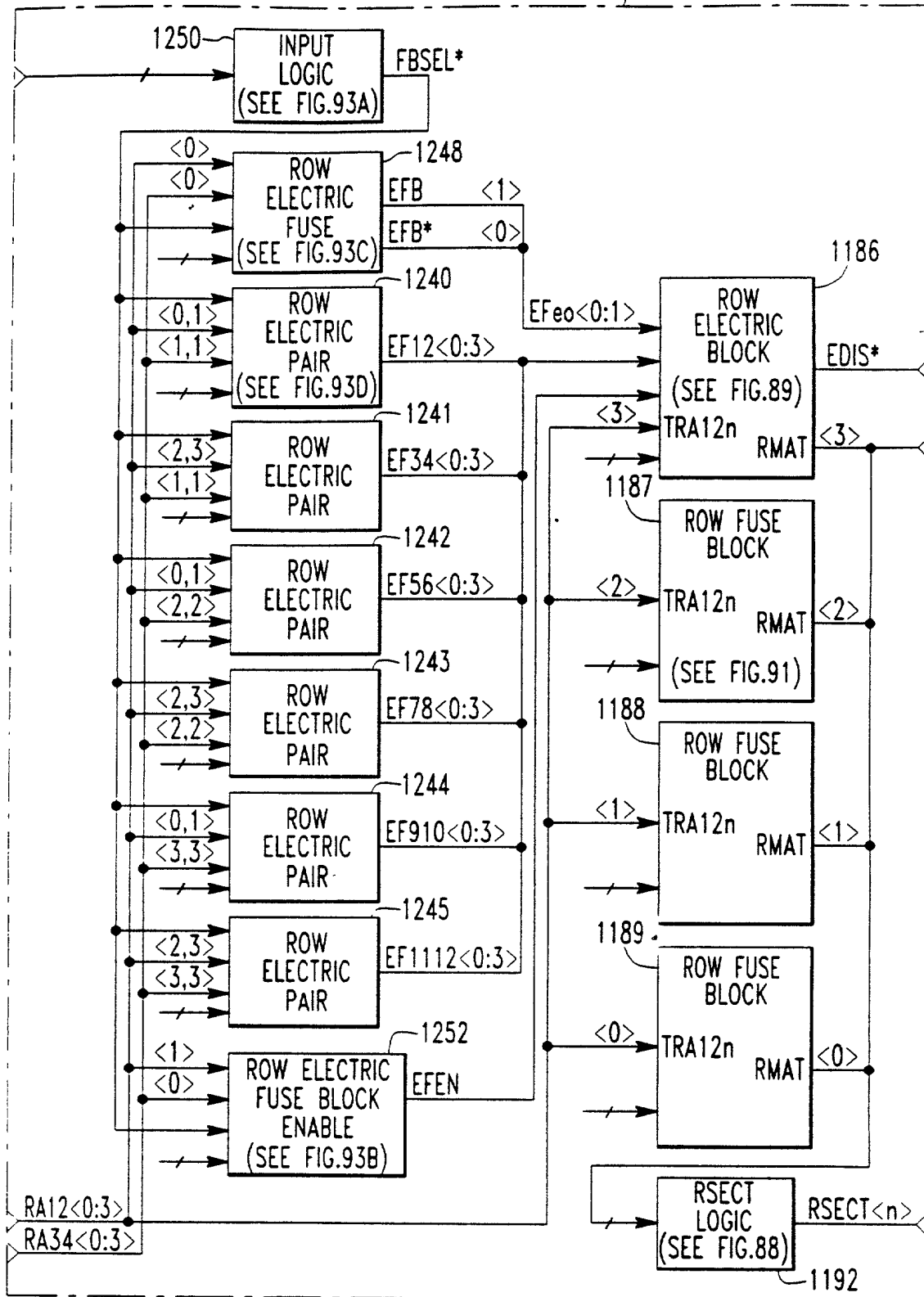
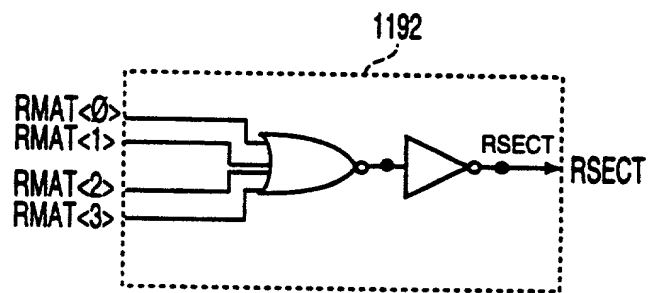


FIG. 87

**FIG. 88**

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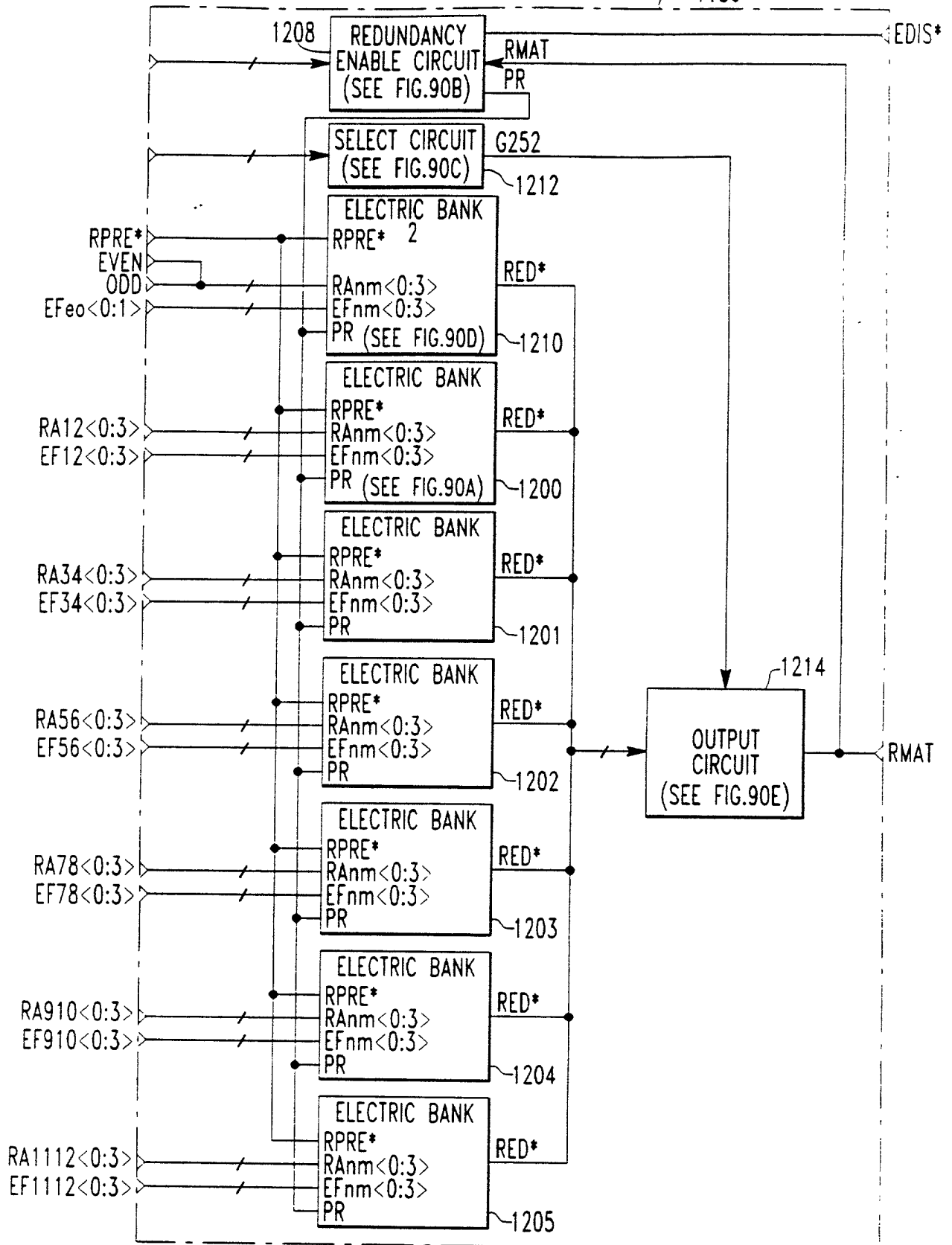


FIG. 89

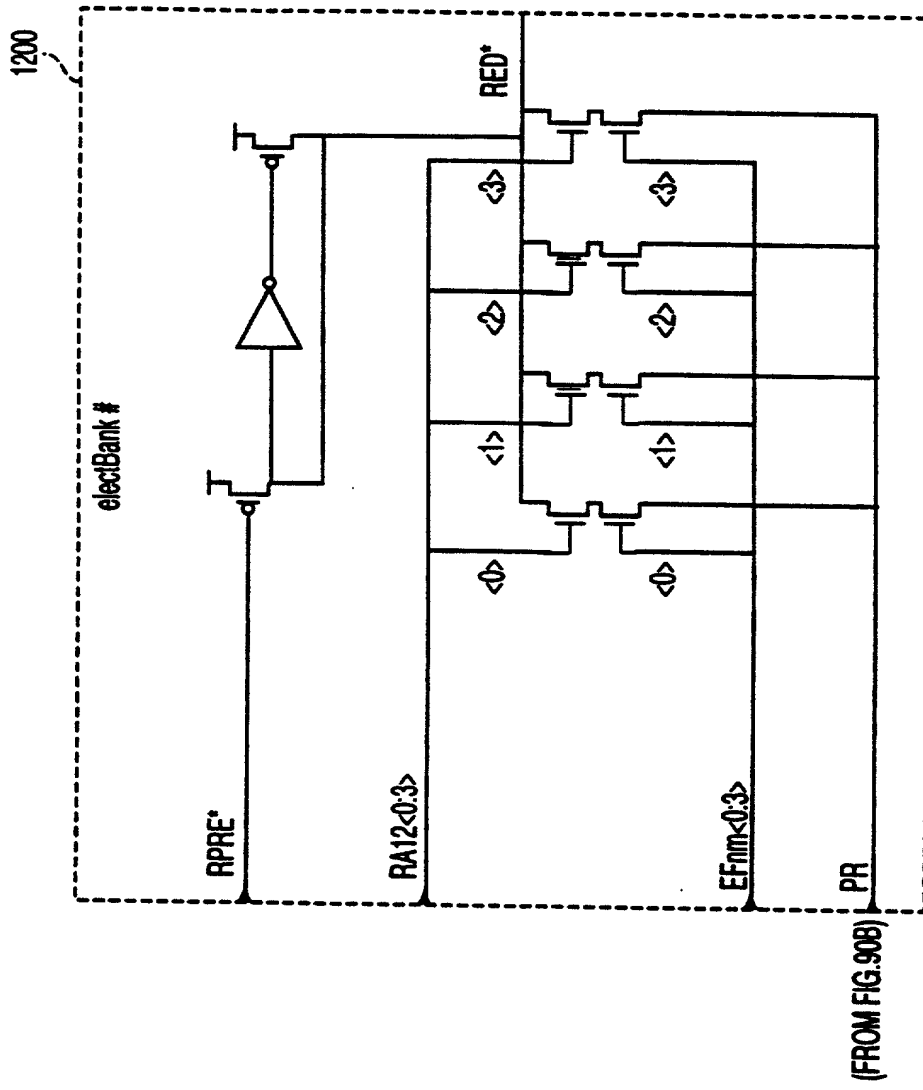


FIG. 90A



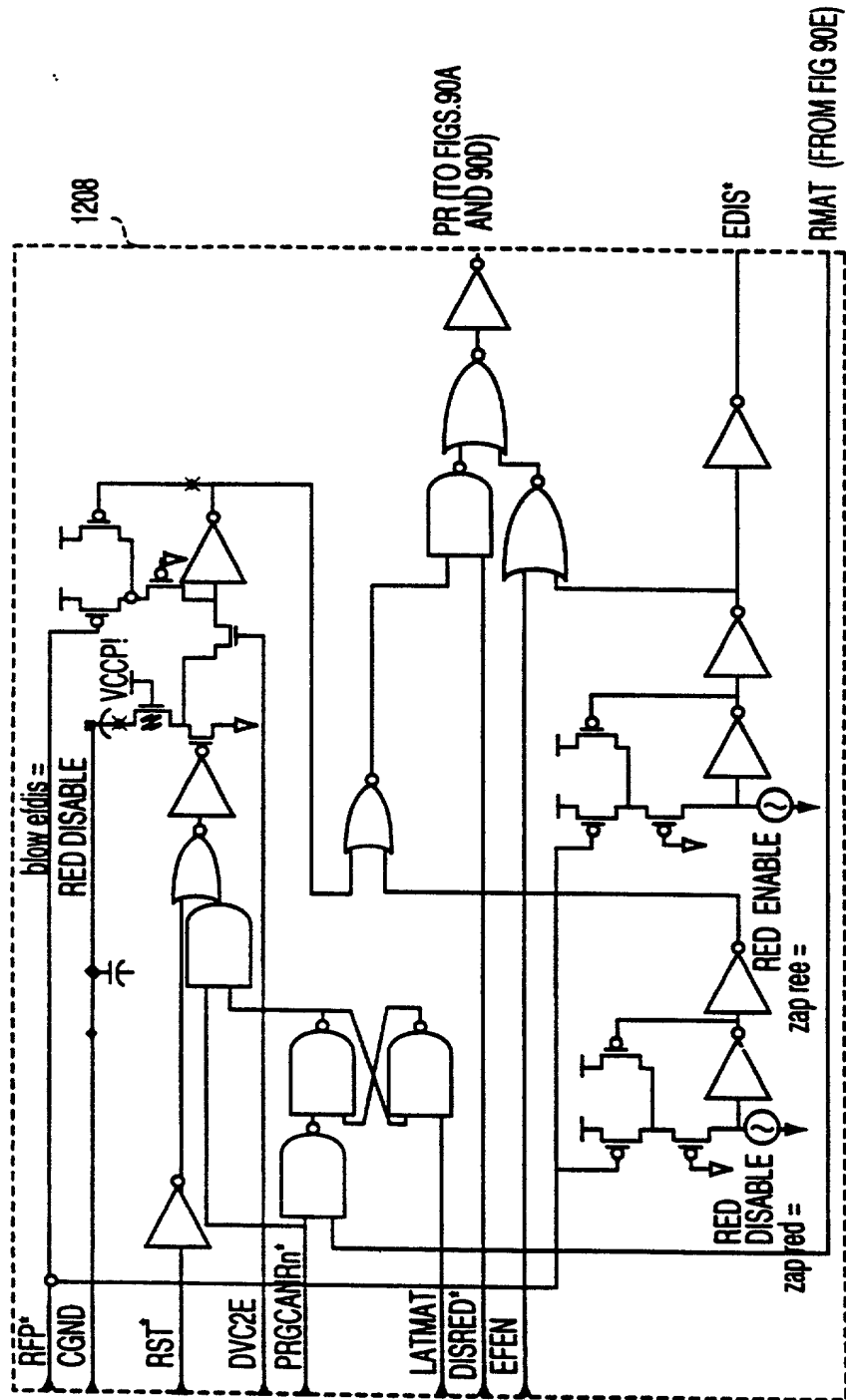


FIG. 90B

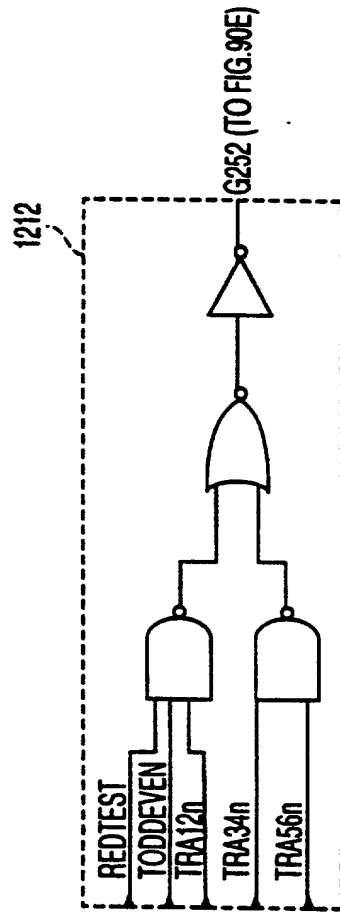


FIG. 90C



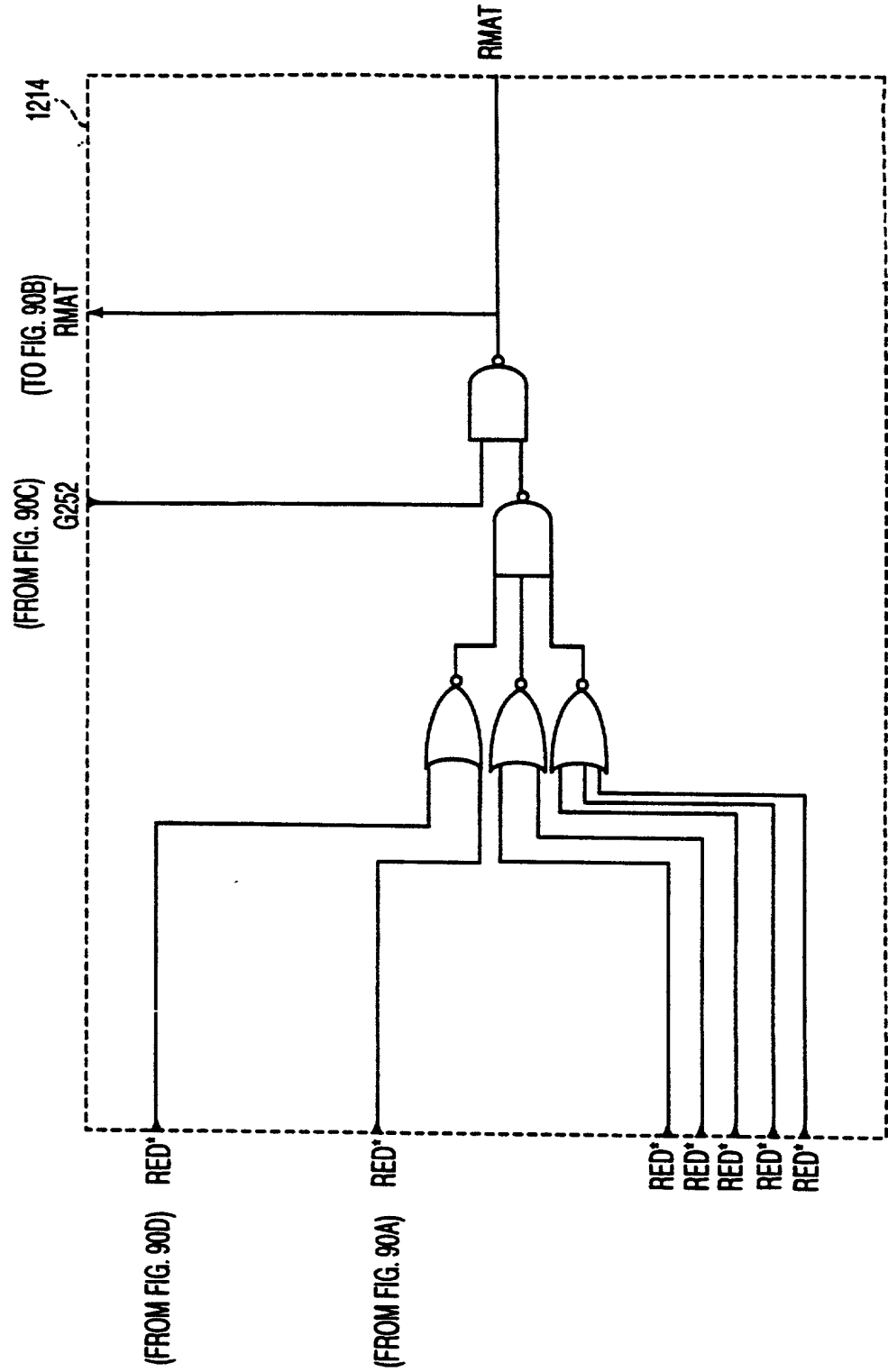


FIG. 90E

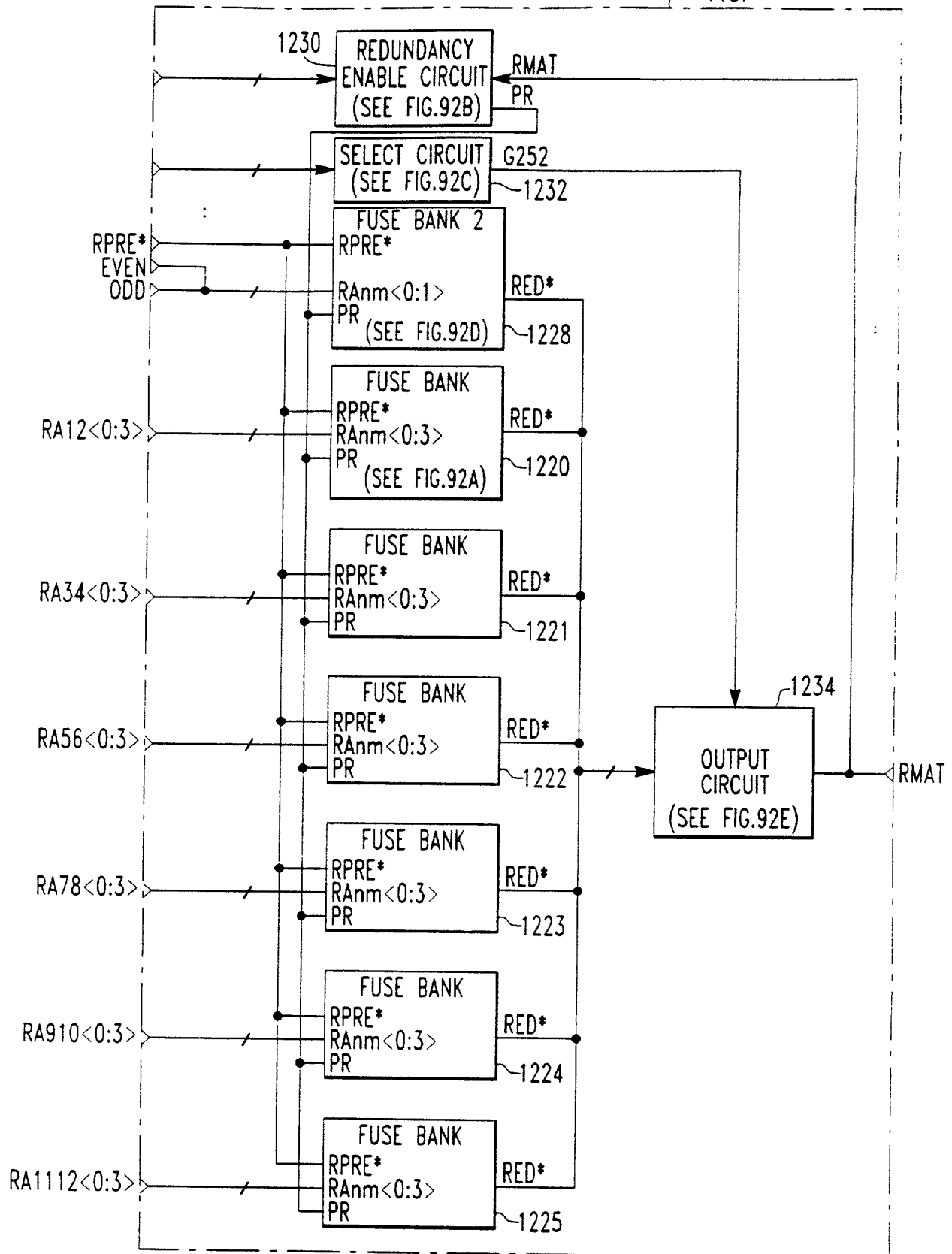


FIG. 91

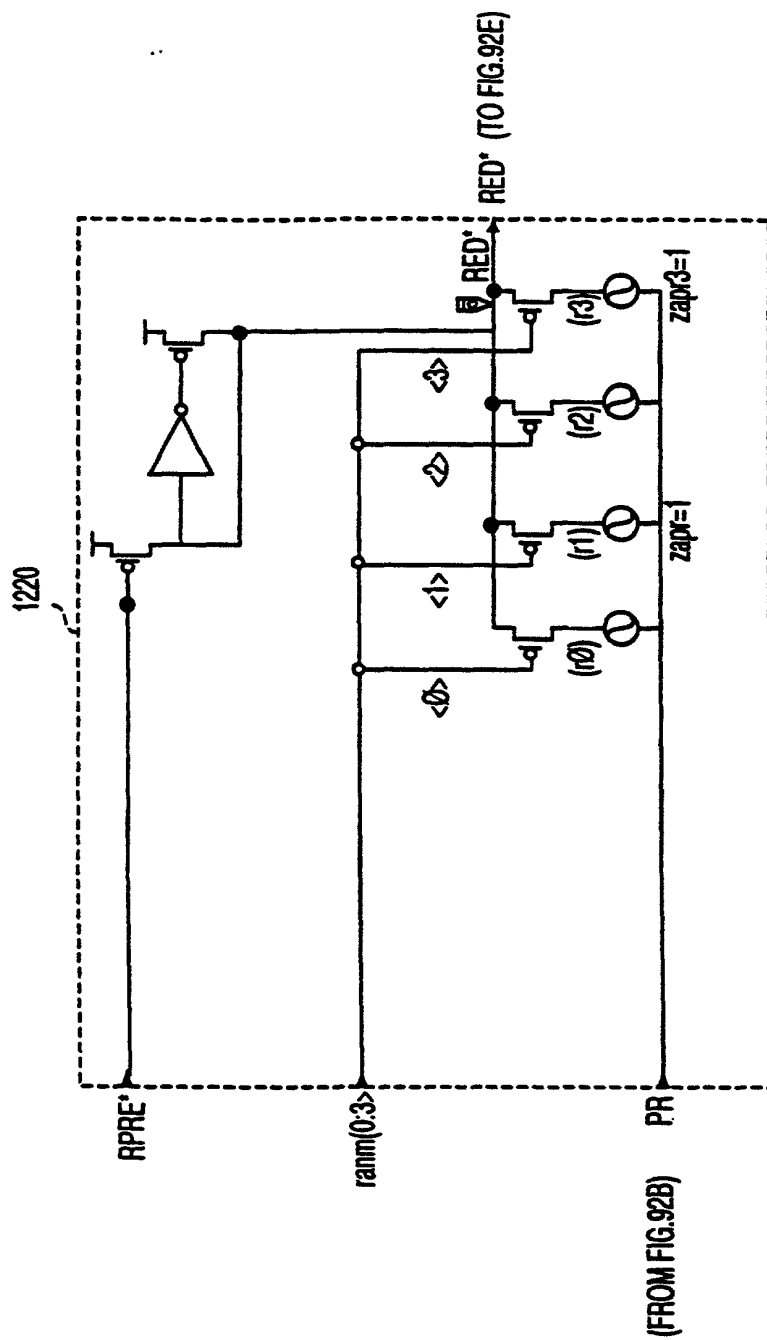
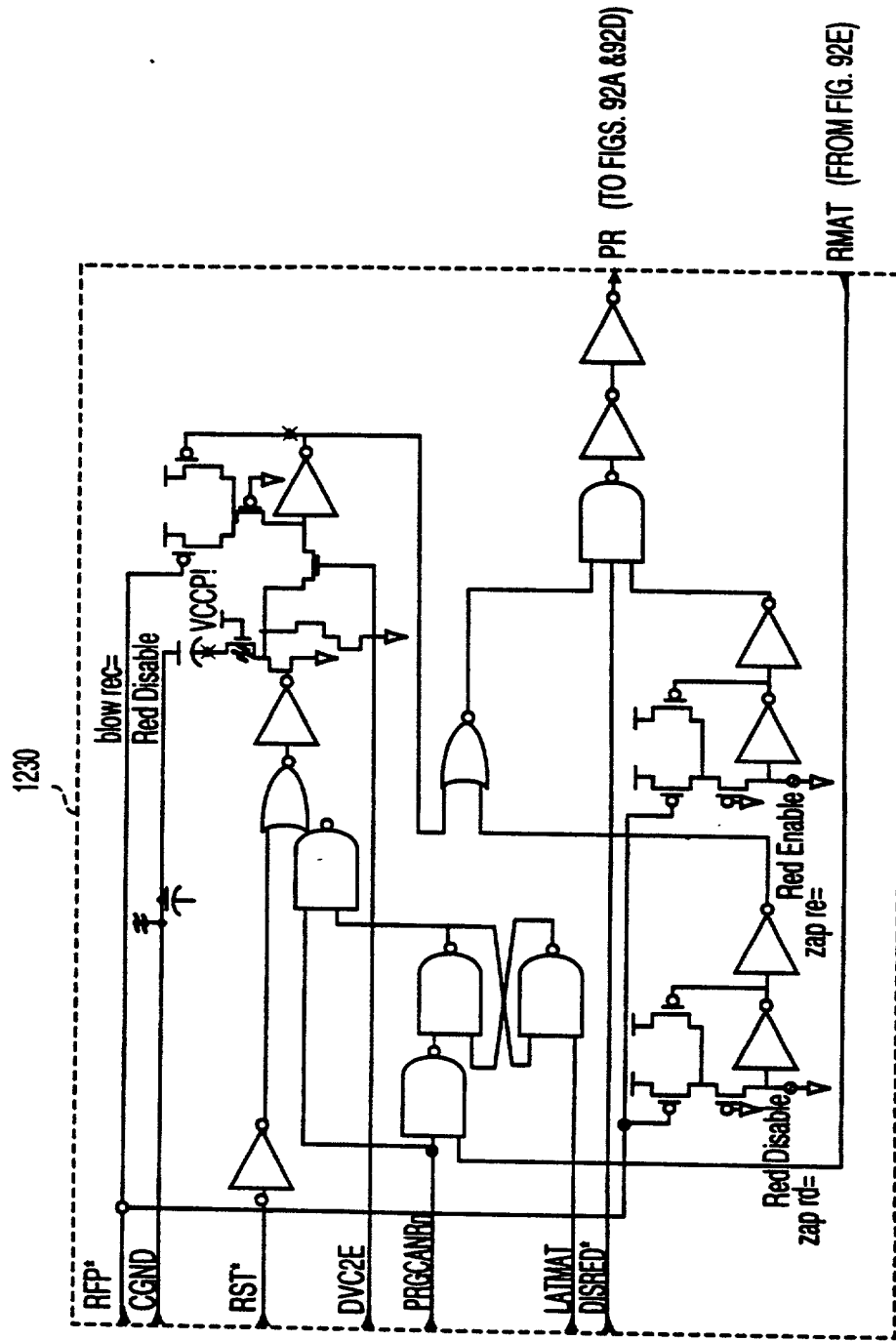


FIG. 92A



**FIG. 92B**

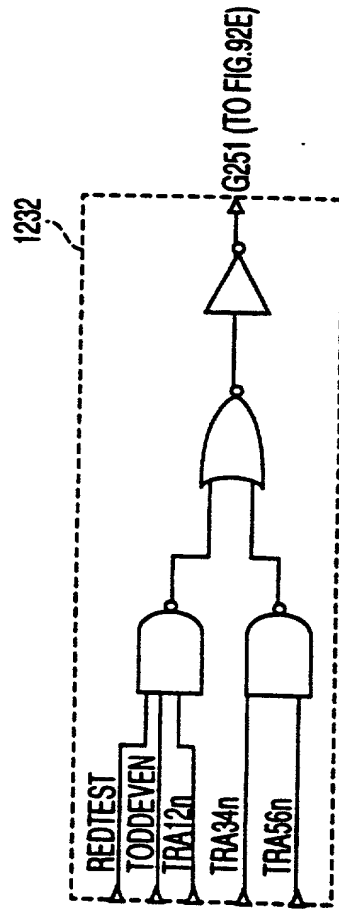


FIG. 92C



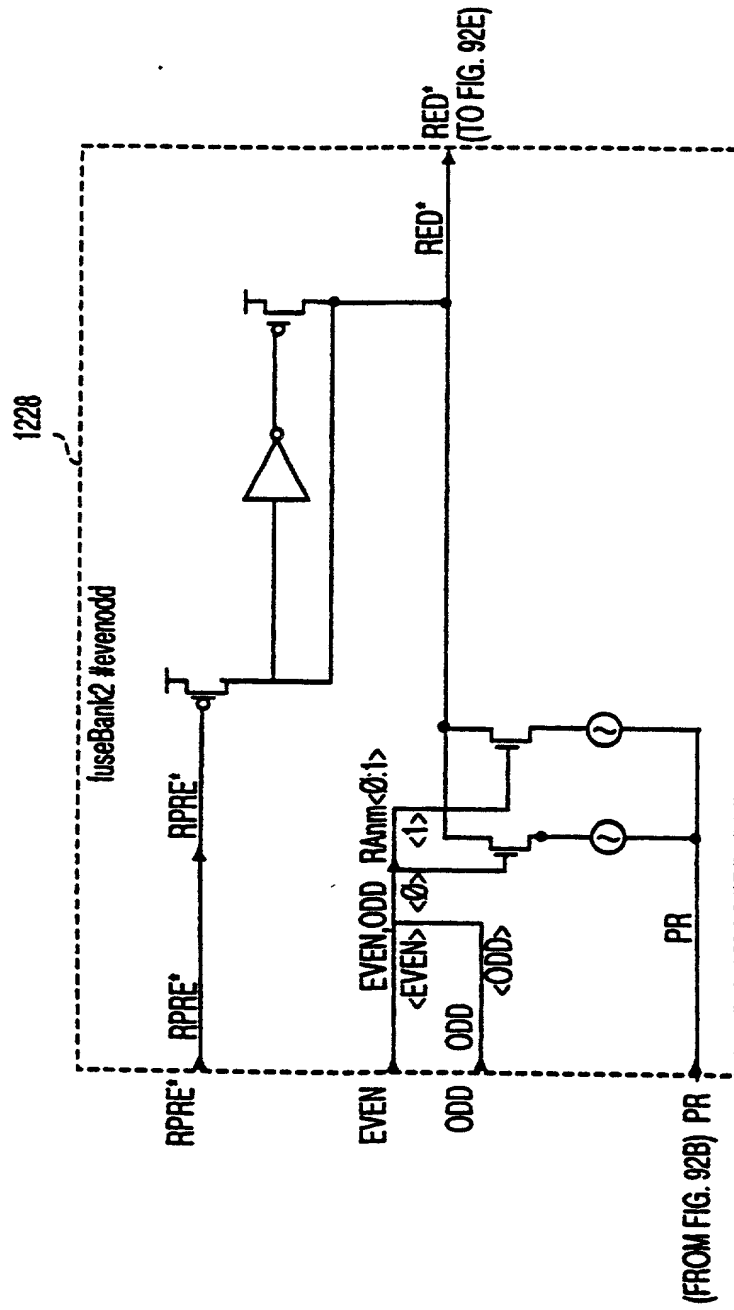


FIG. 92D

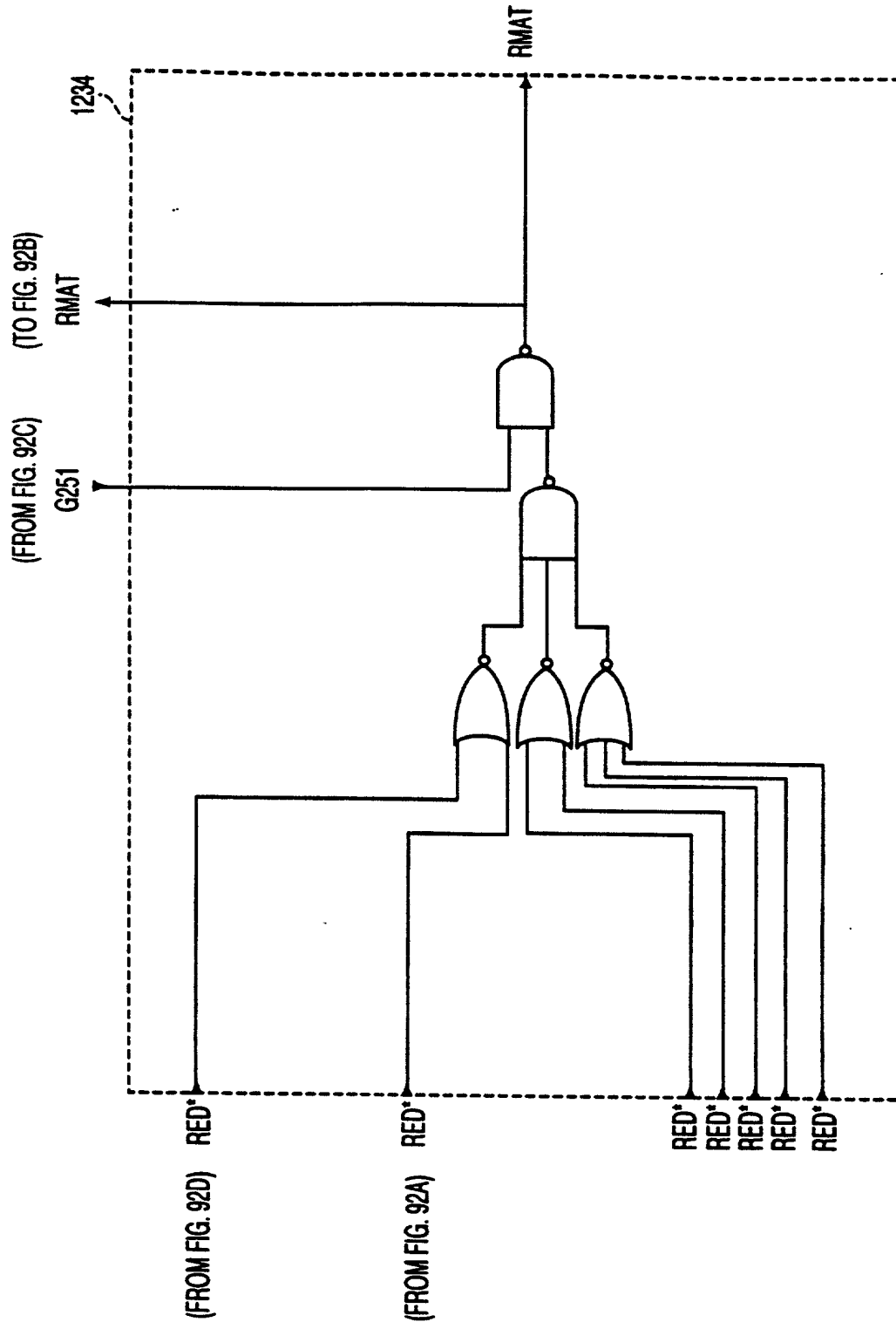
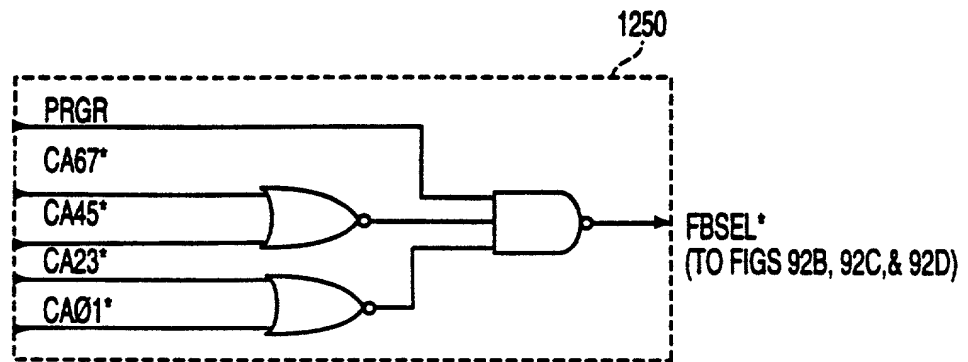


FIG. 92E



**FIG. 93A**



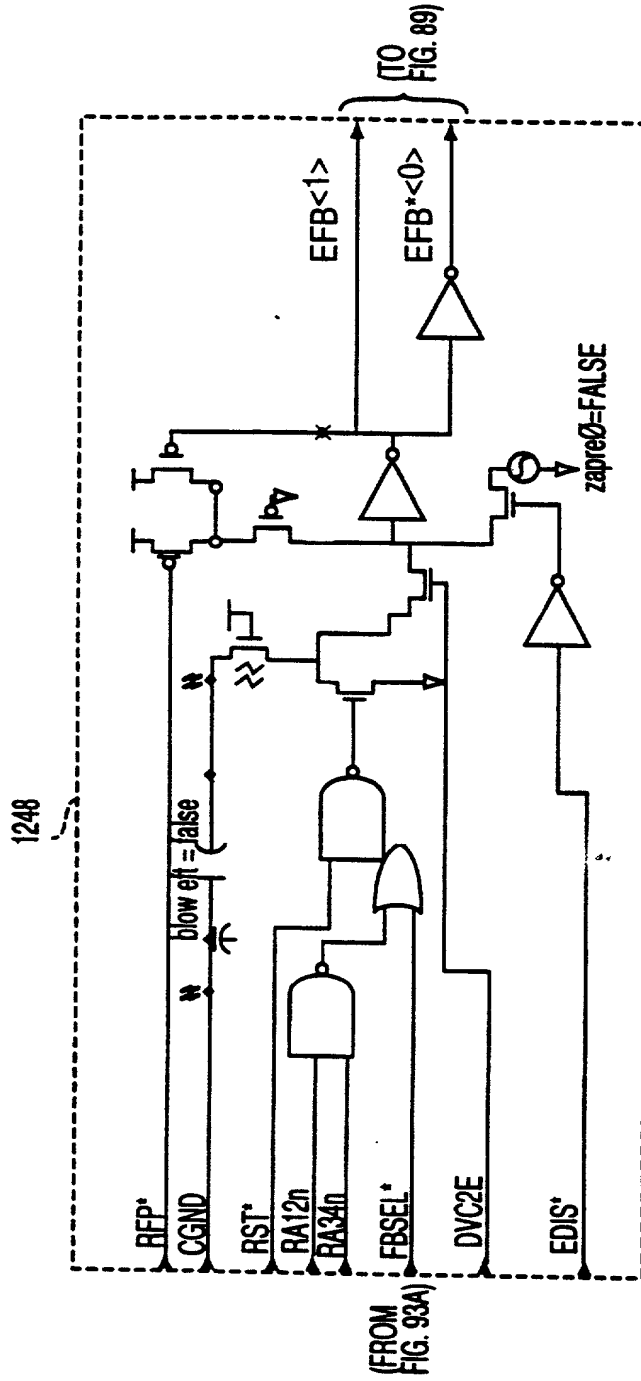


FIG. 93C

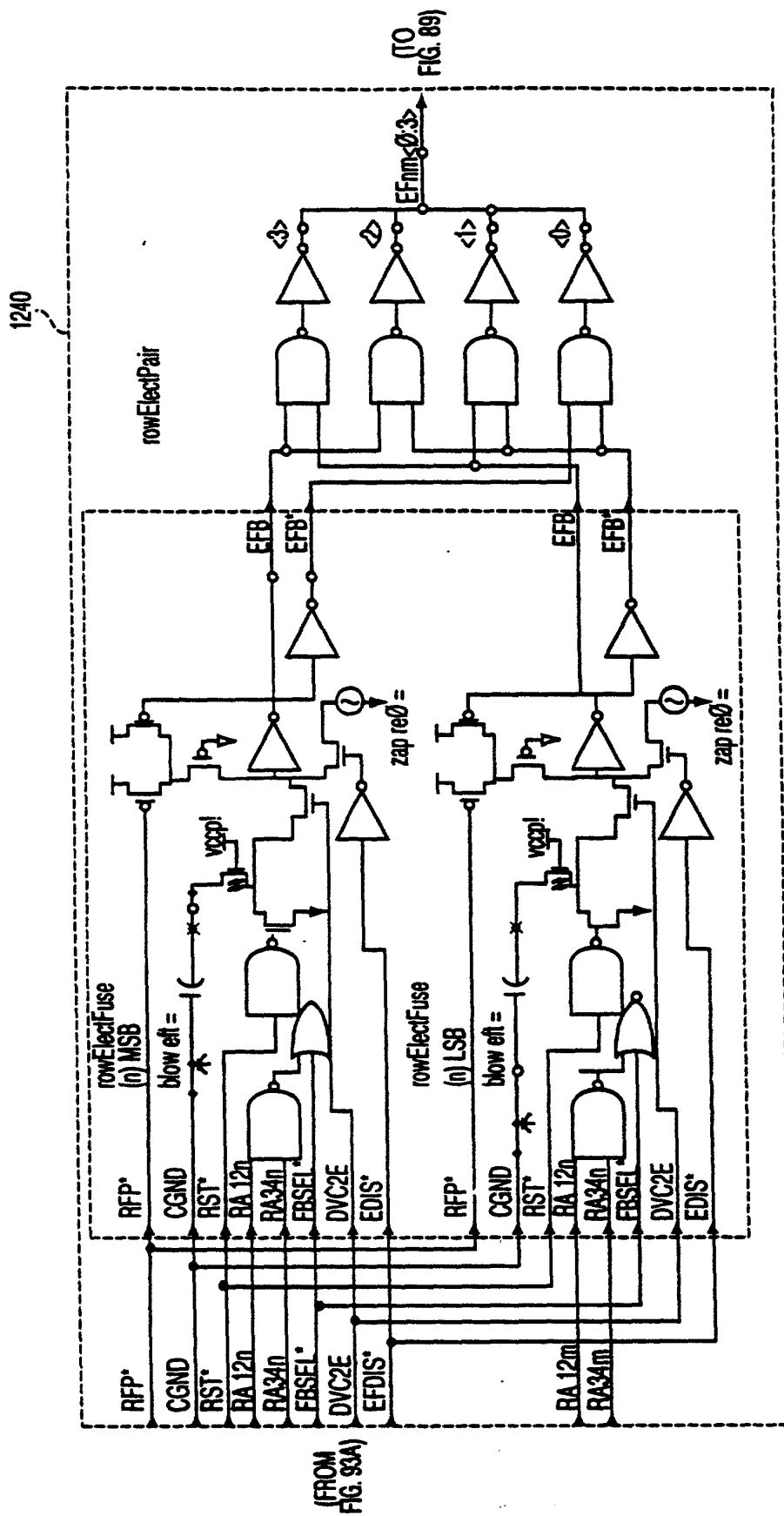
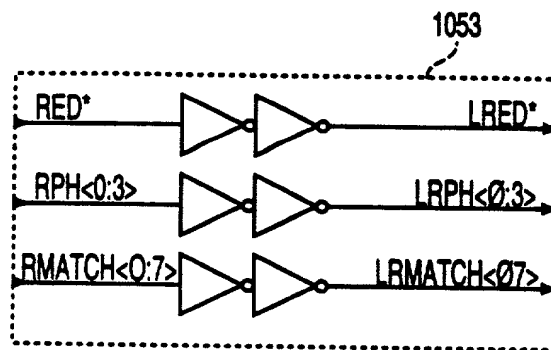


FIG. 93D

**FIG. 94**

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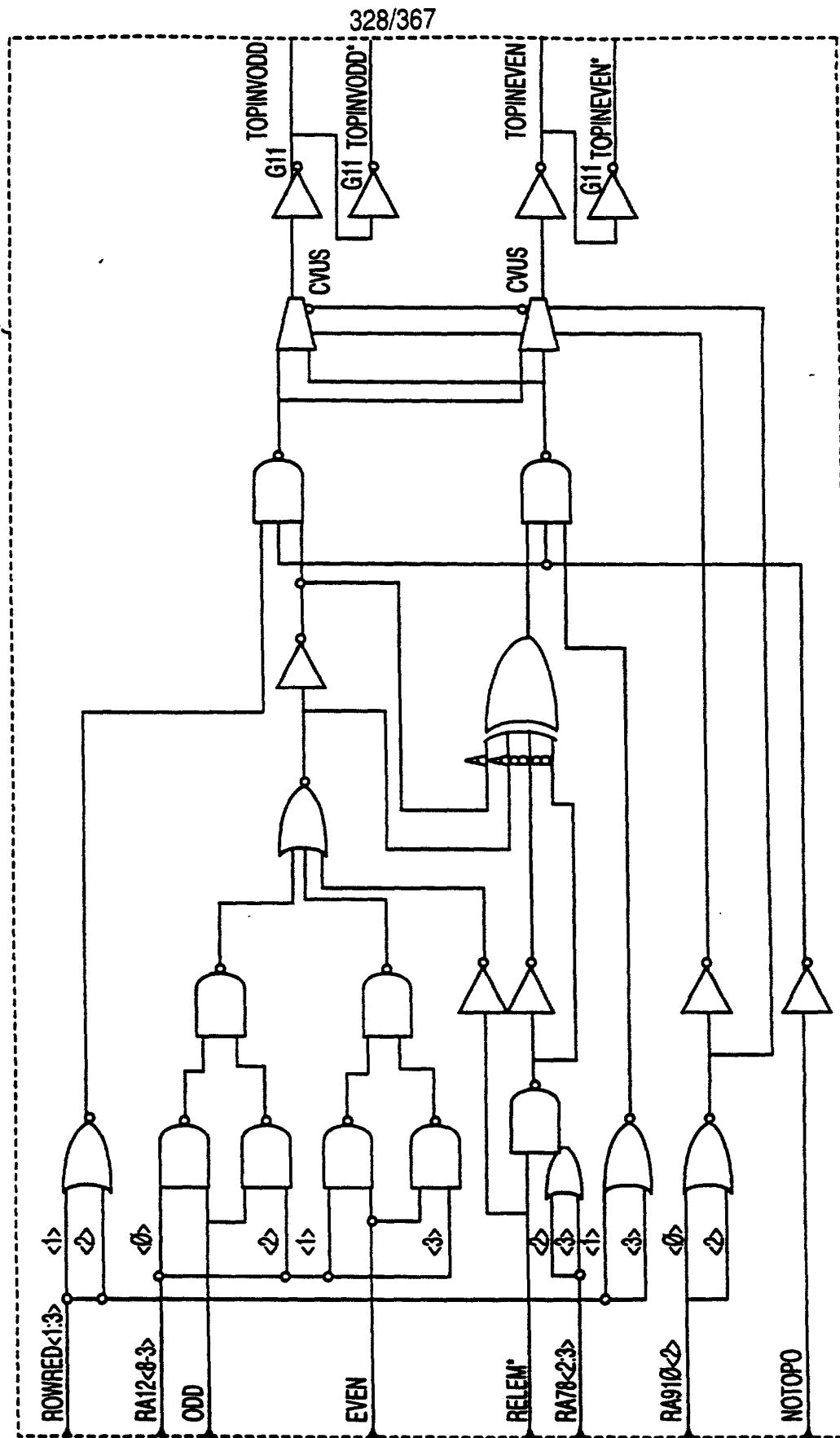
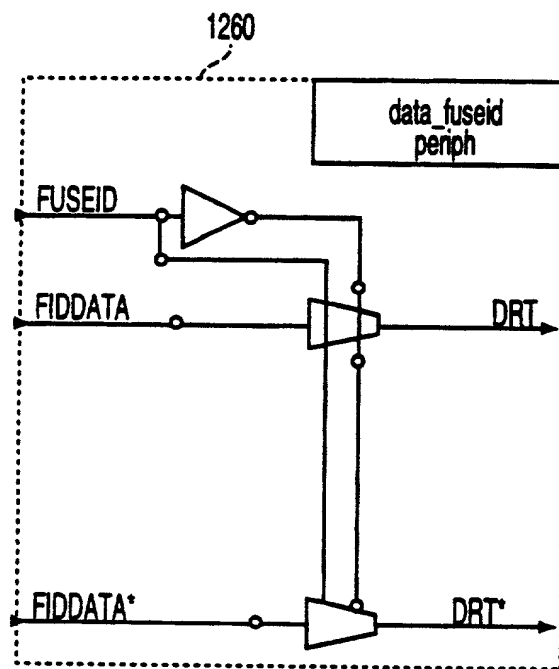


FIG. 95



**FIG. 96**



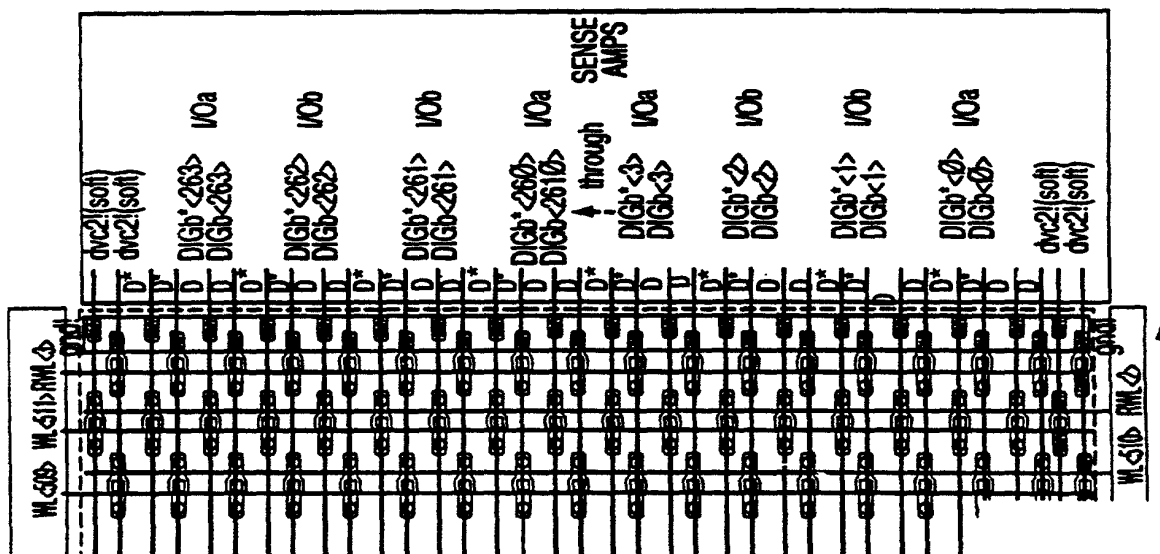
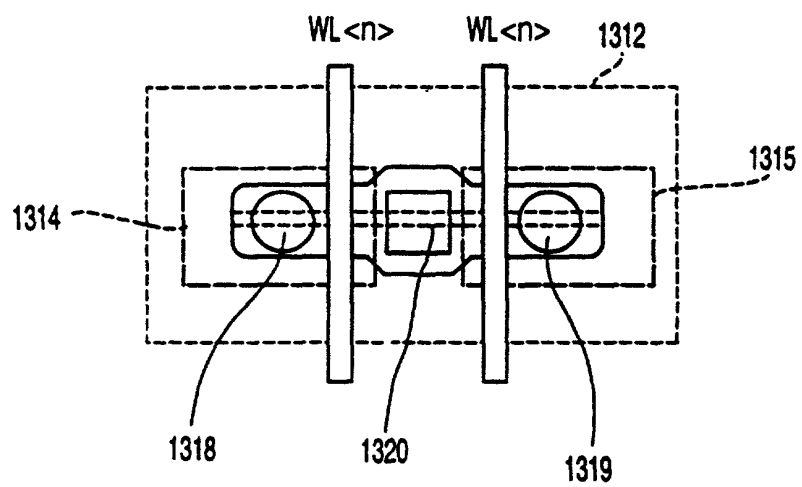


FIG. 97-1 FIG. 97-2

FIG. 97-2

**FIG. 98**

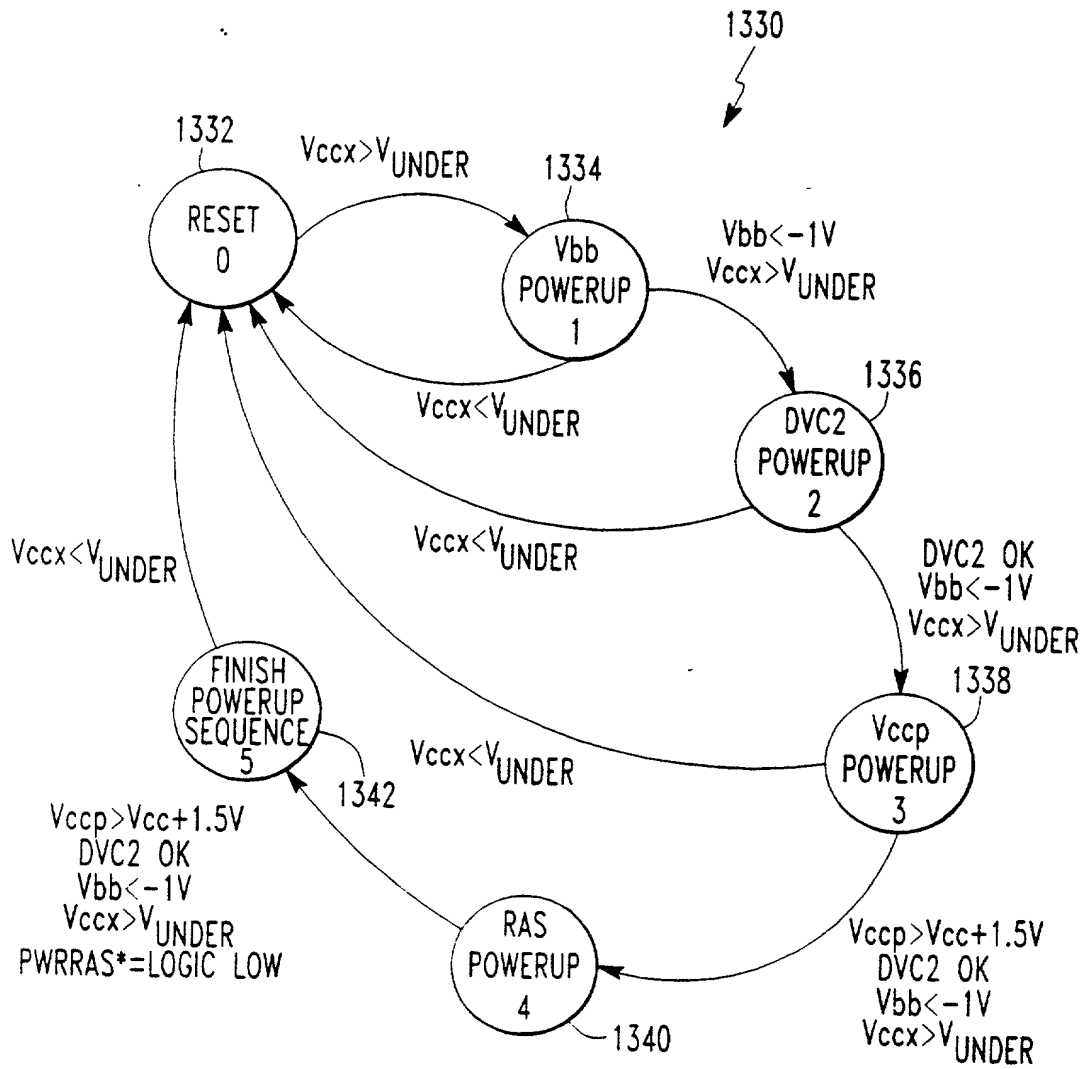


FIG. 99

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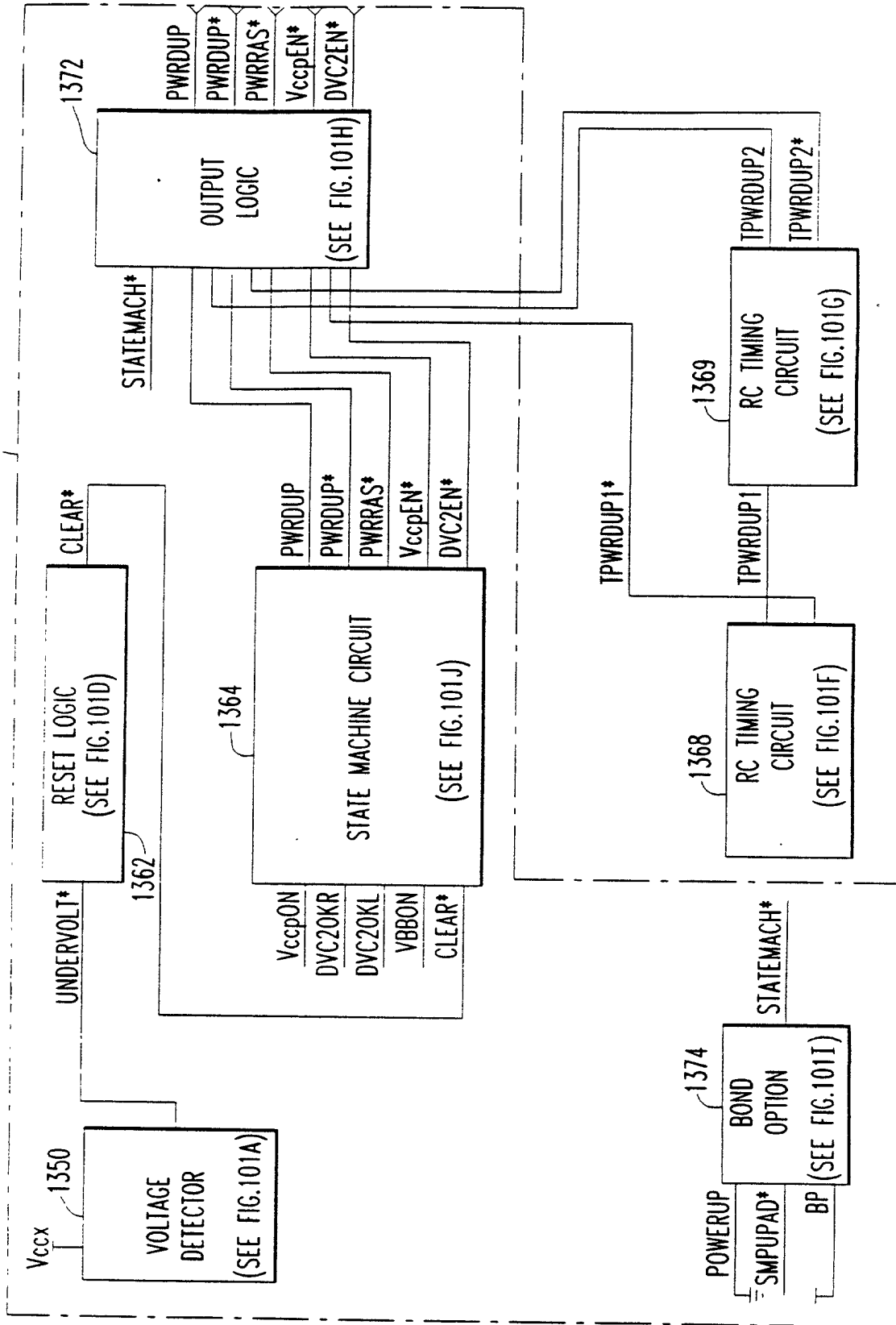
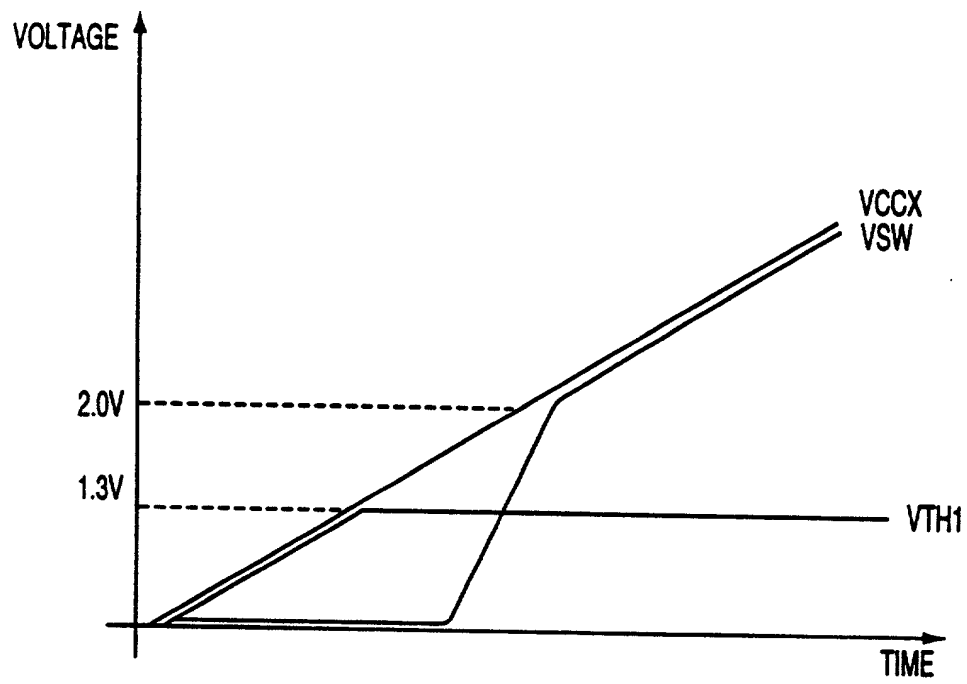
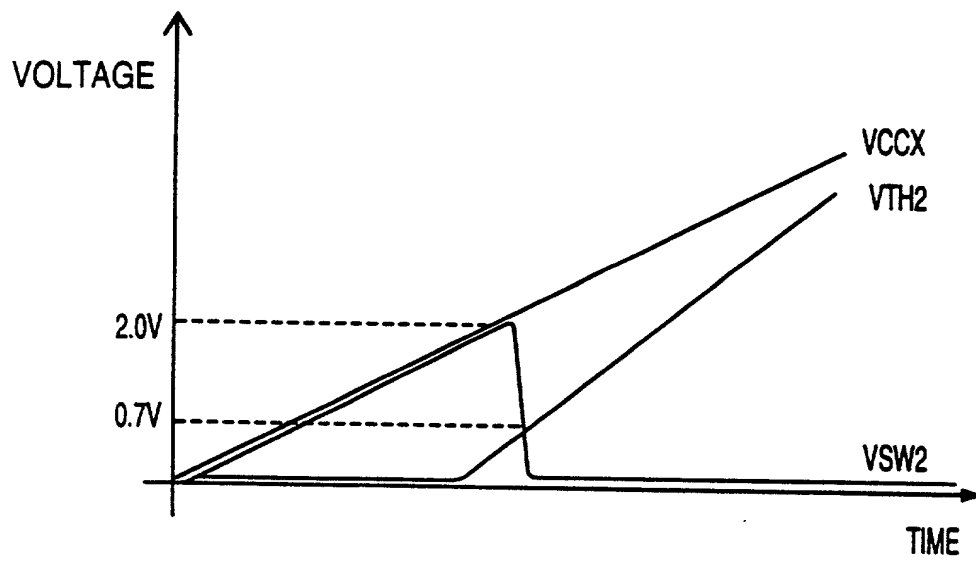


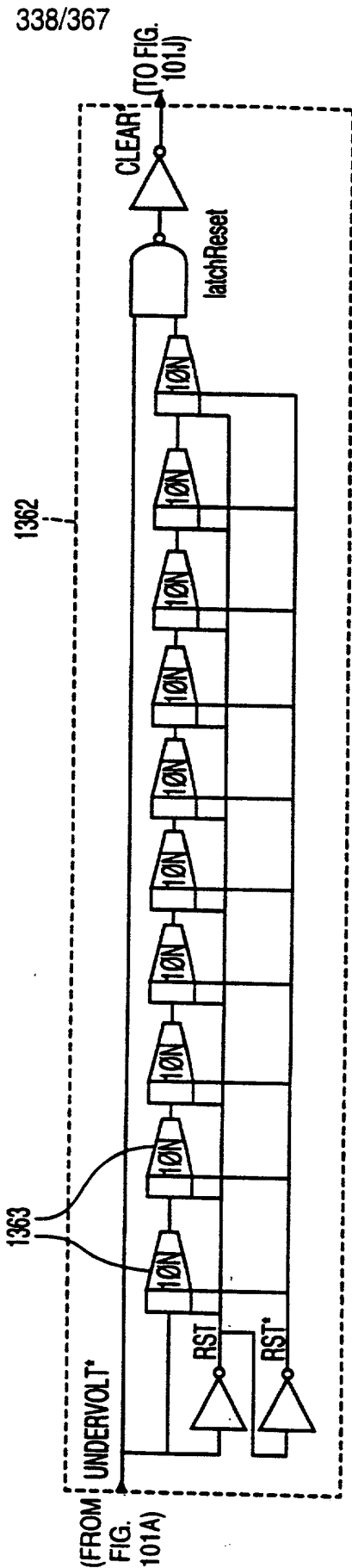
FIG. 100



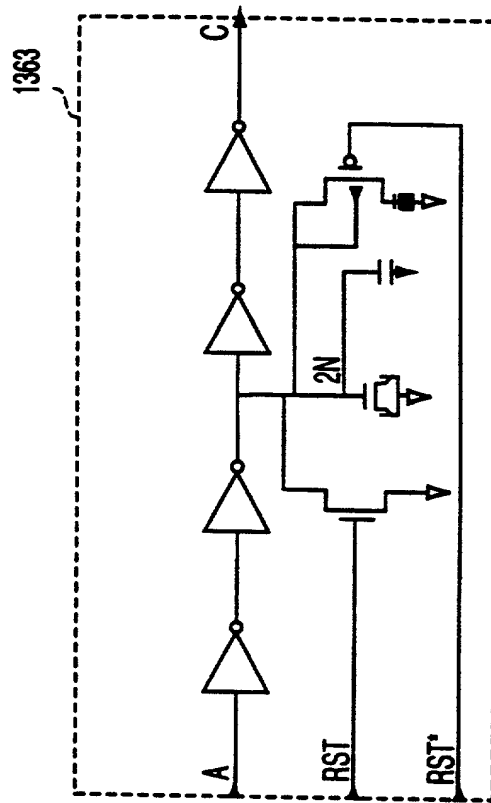
**FIG. 101B**



*FIG. 101C*



**FIG. 101D**

*FIG. 101E*

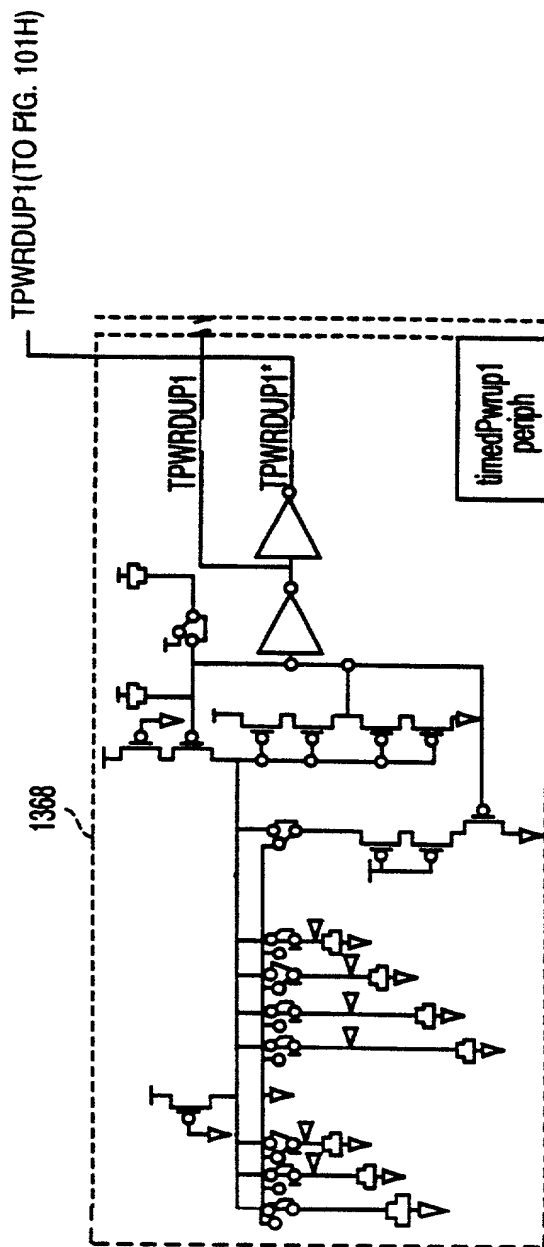


FIG. 101F

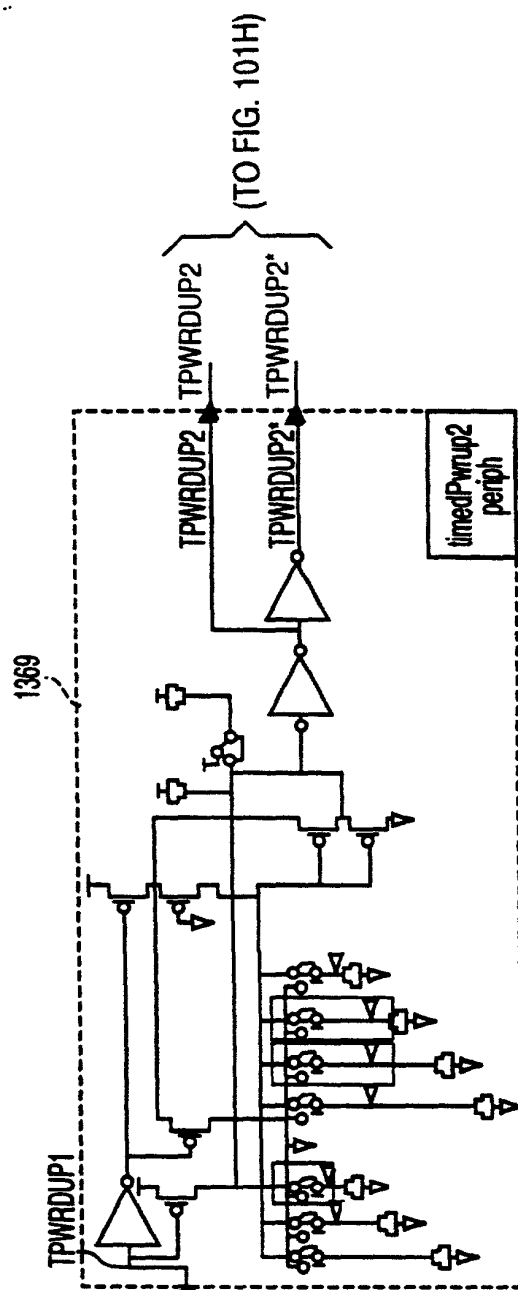


FIG. 101G

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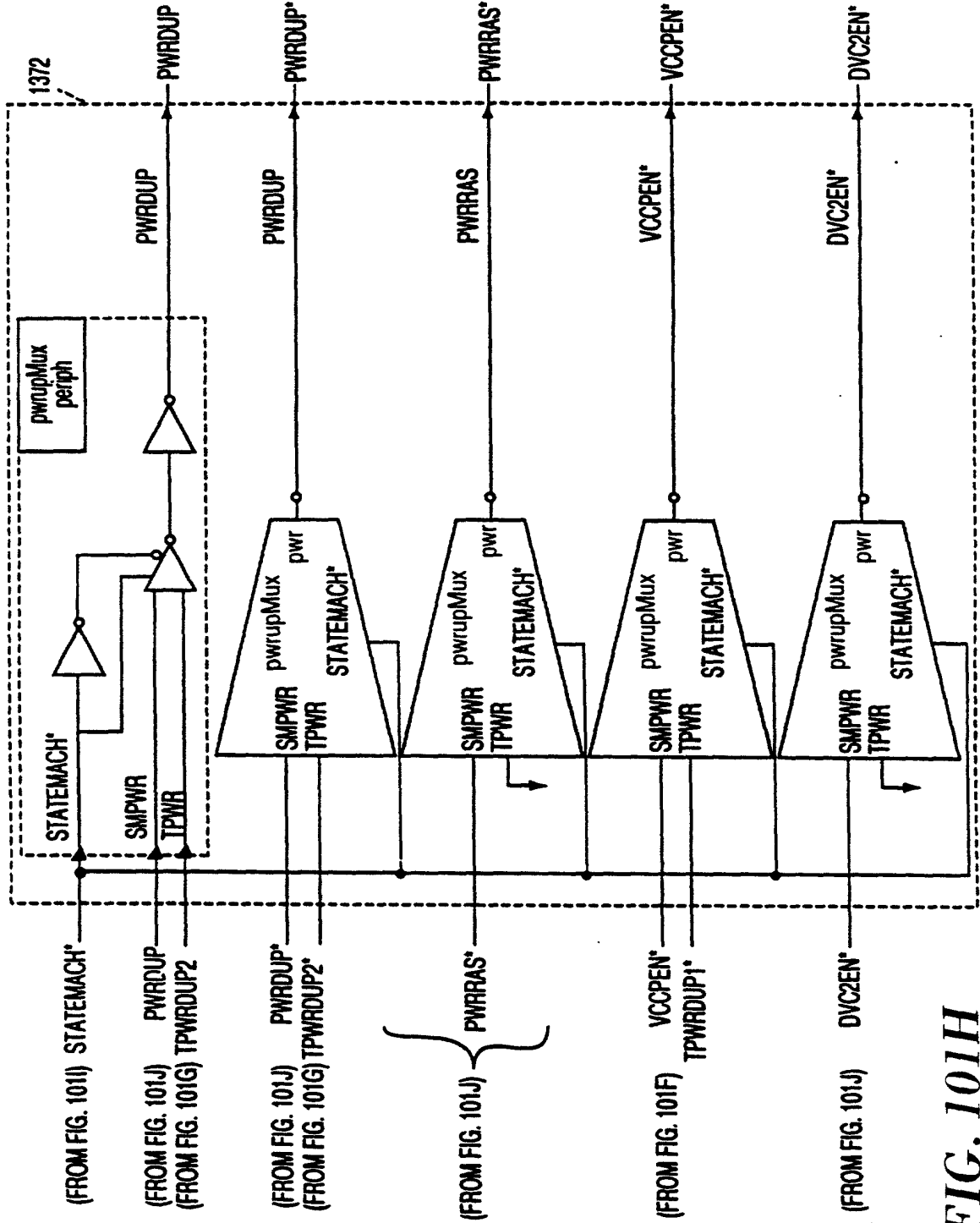


FIG. 101H

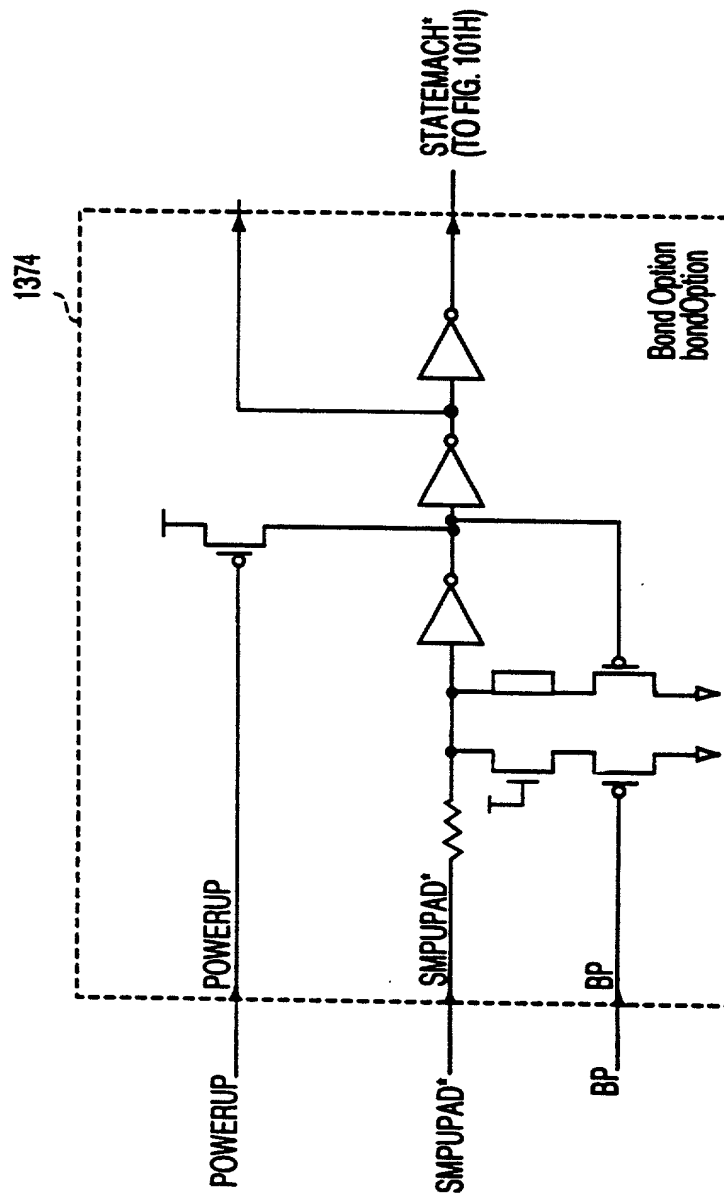
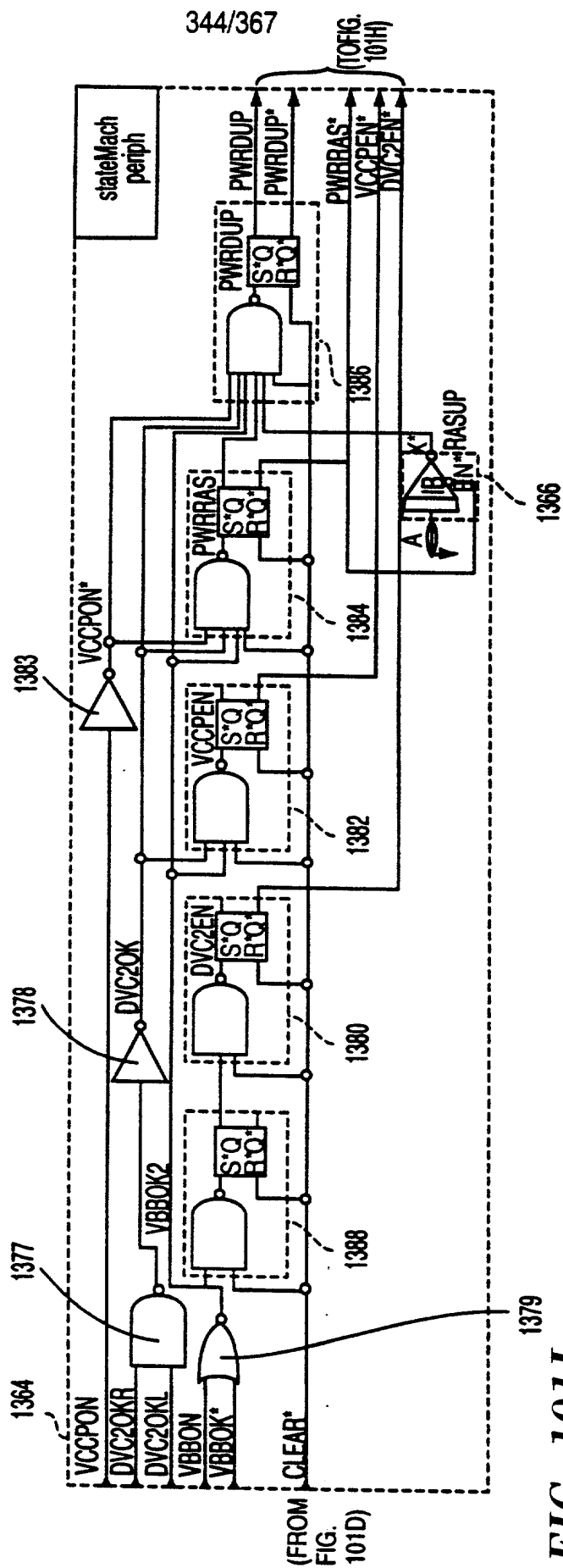
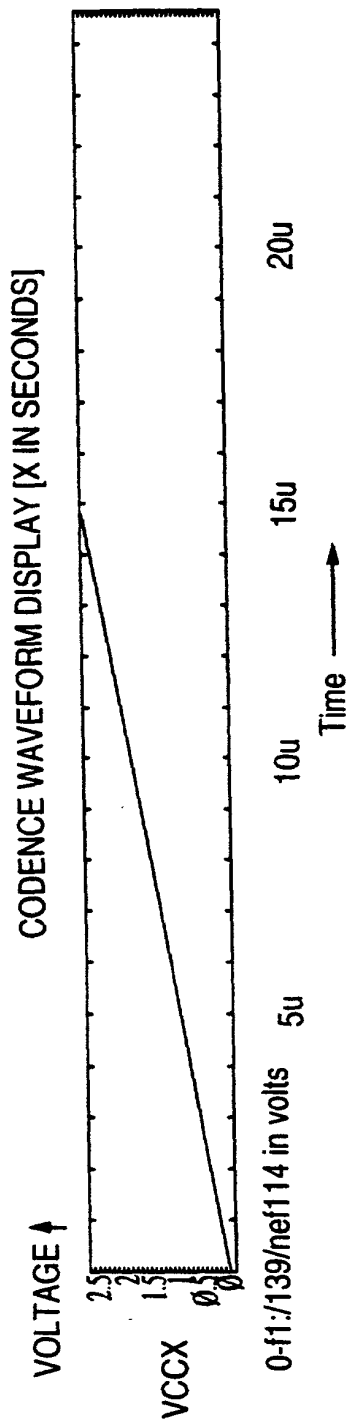


FIG. 101I



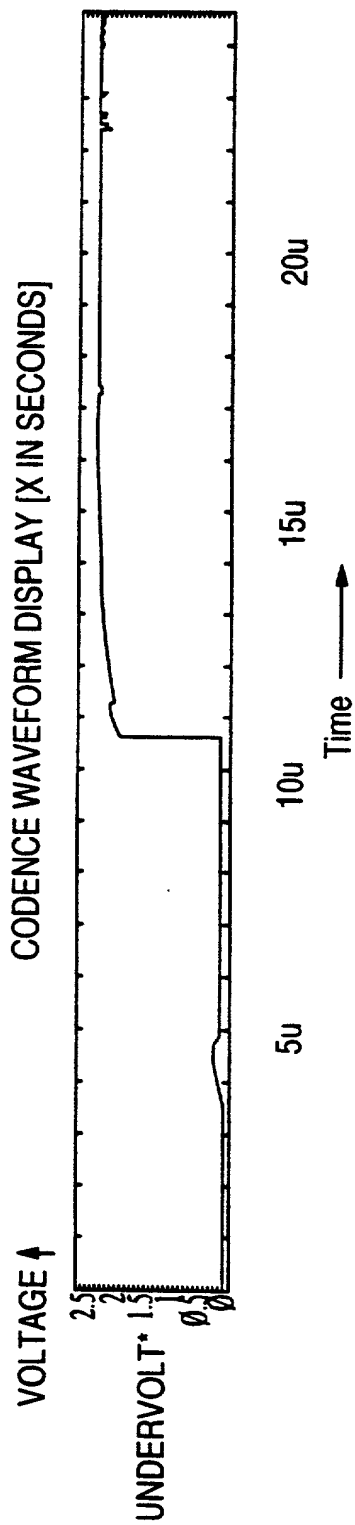
**FIG. 101J**





NOTE THAT PWRRAS\* WAITED FOR DVC20KR

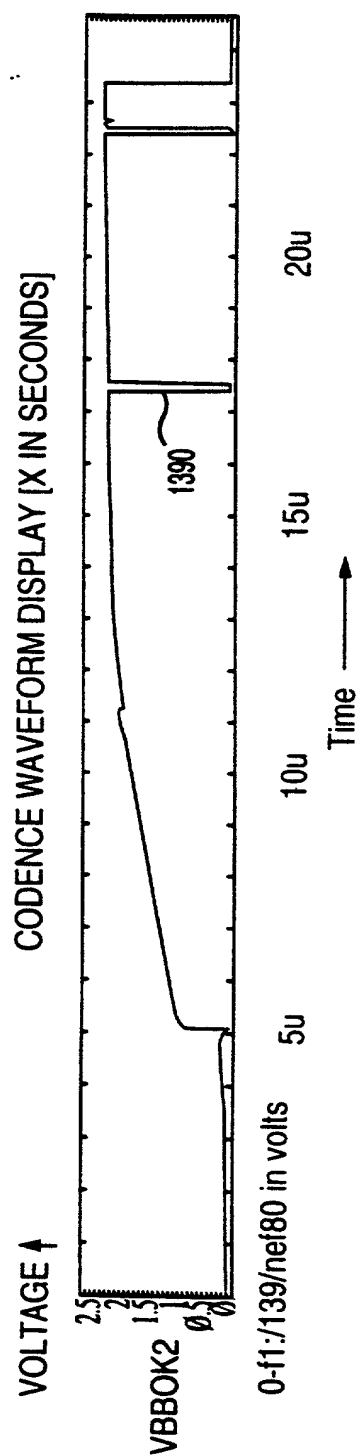
**FIG. 102A**



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102B**

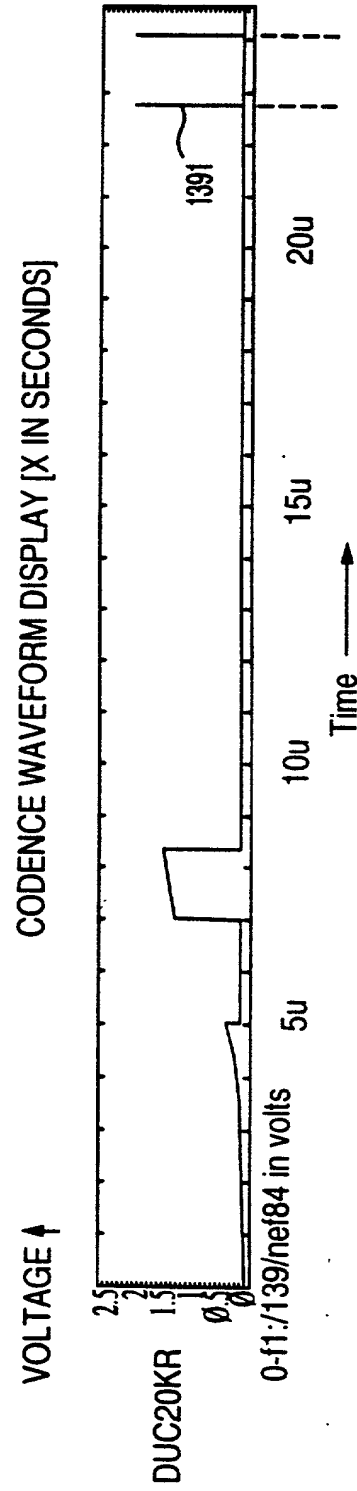




NOTE THAT PWRRAS\* WAITED FOR DVC20KR

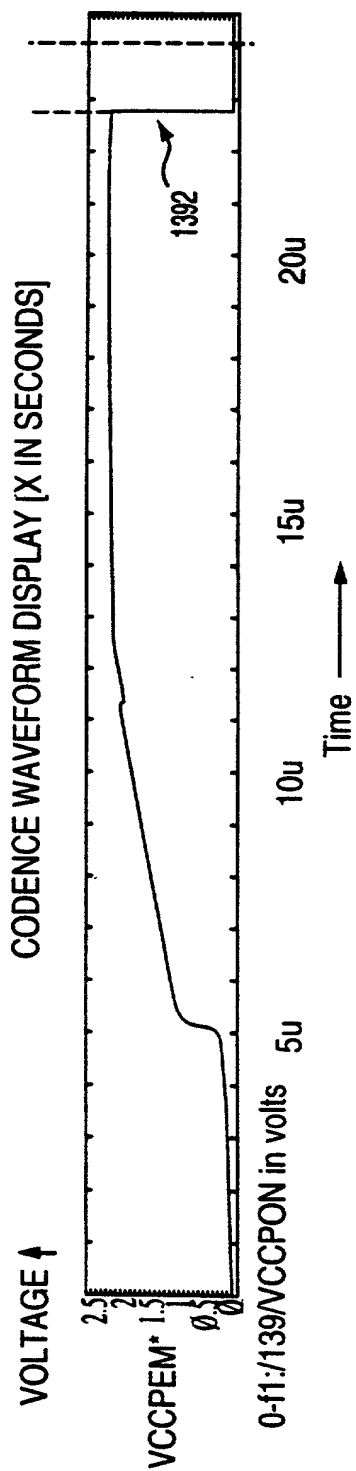
**FIG. 102D**





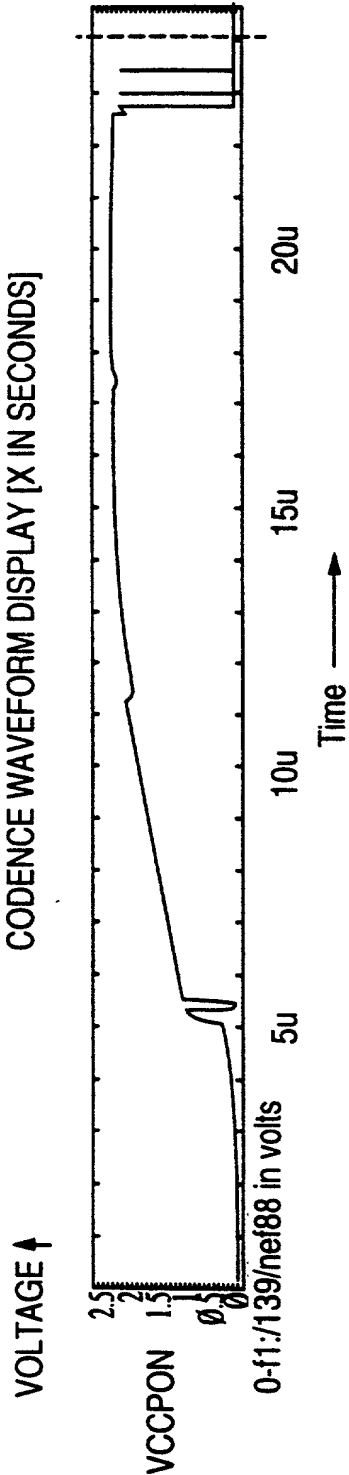
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

FIG. 102F



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

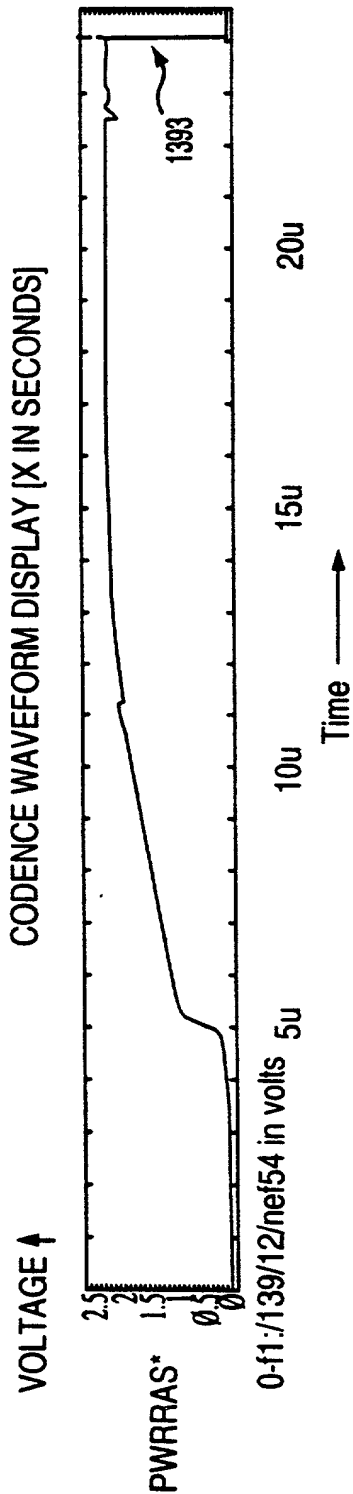
**FIG. 102G**



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

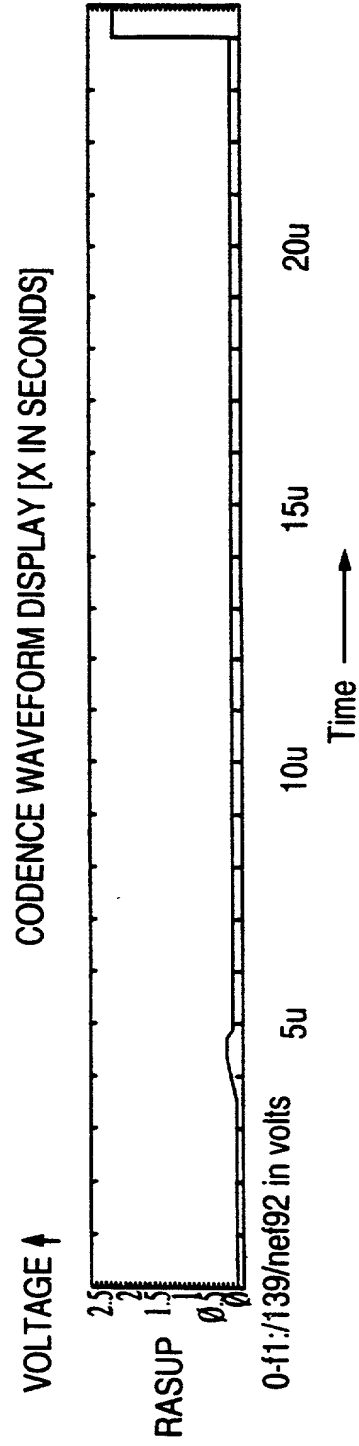
FIG. 102H





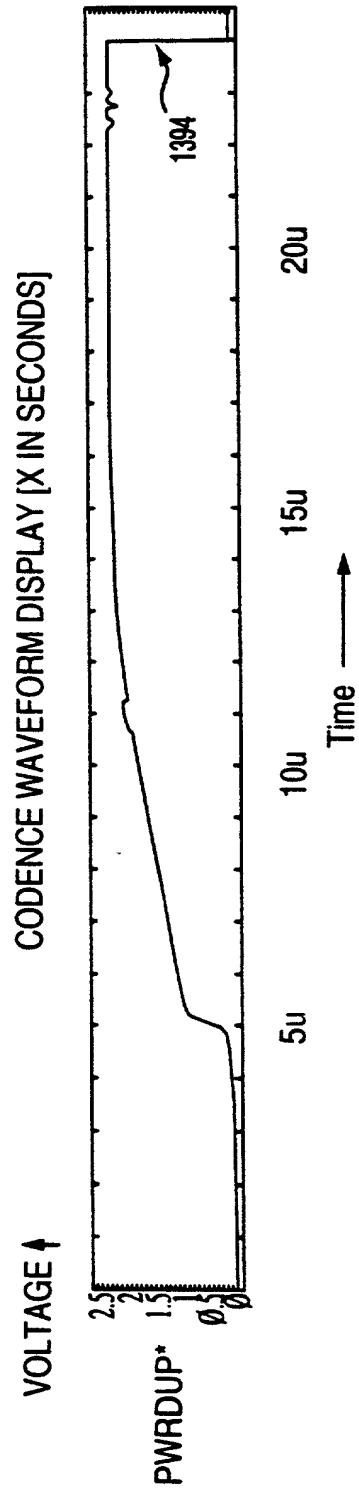
NOTE THAT PWRRAS\* WAITED FOR DVC20KR

FIG. 102I



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

**FIG. 102J**



NOTE THAT PWRRAS\* WAITED FOR DVC20KR

FIG. 102K

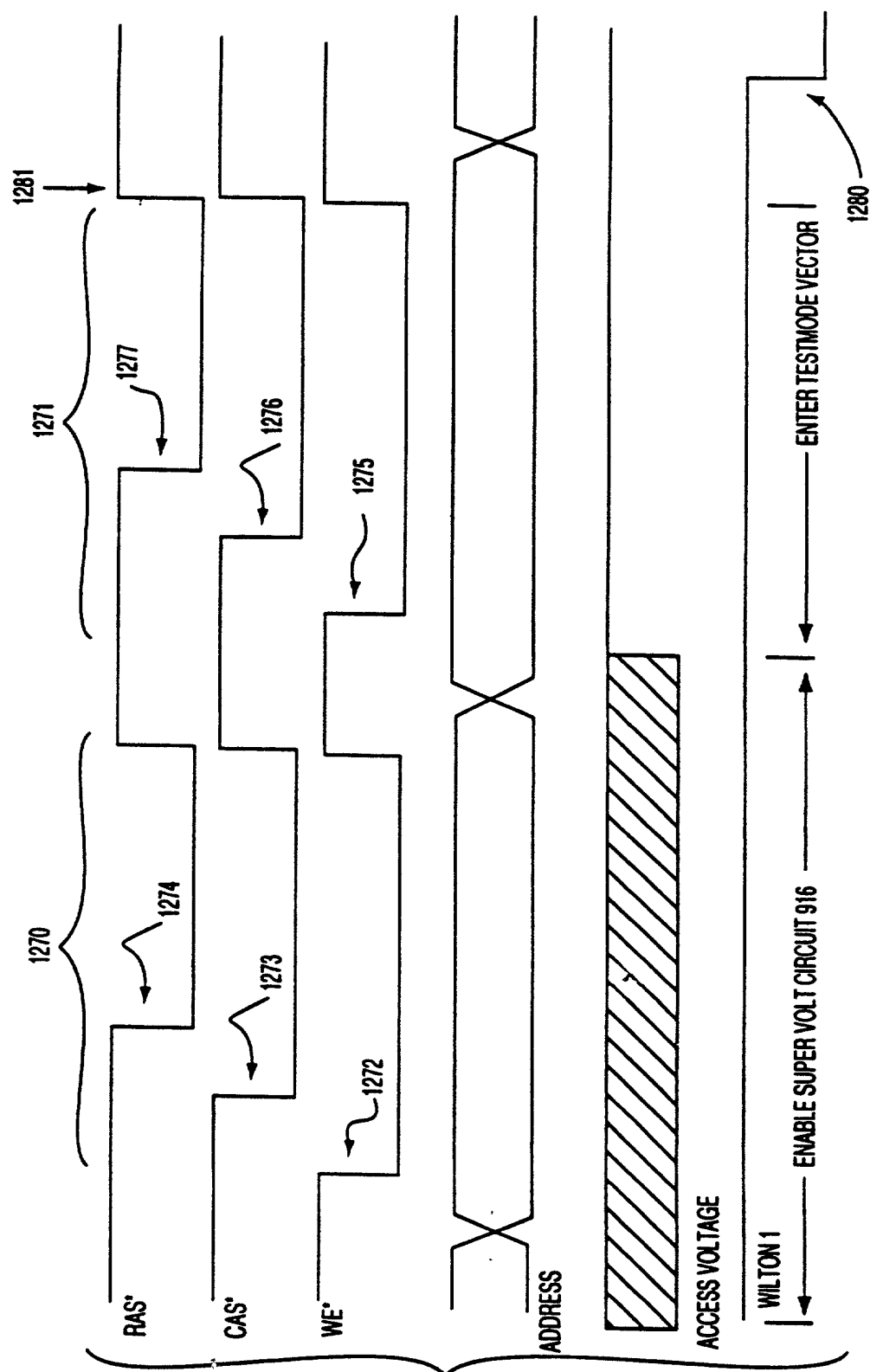
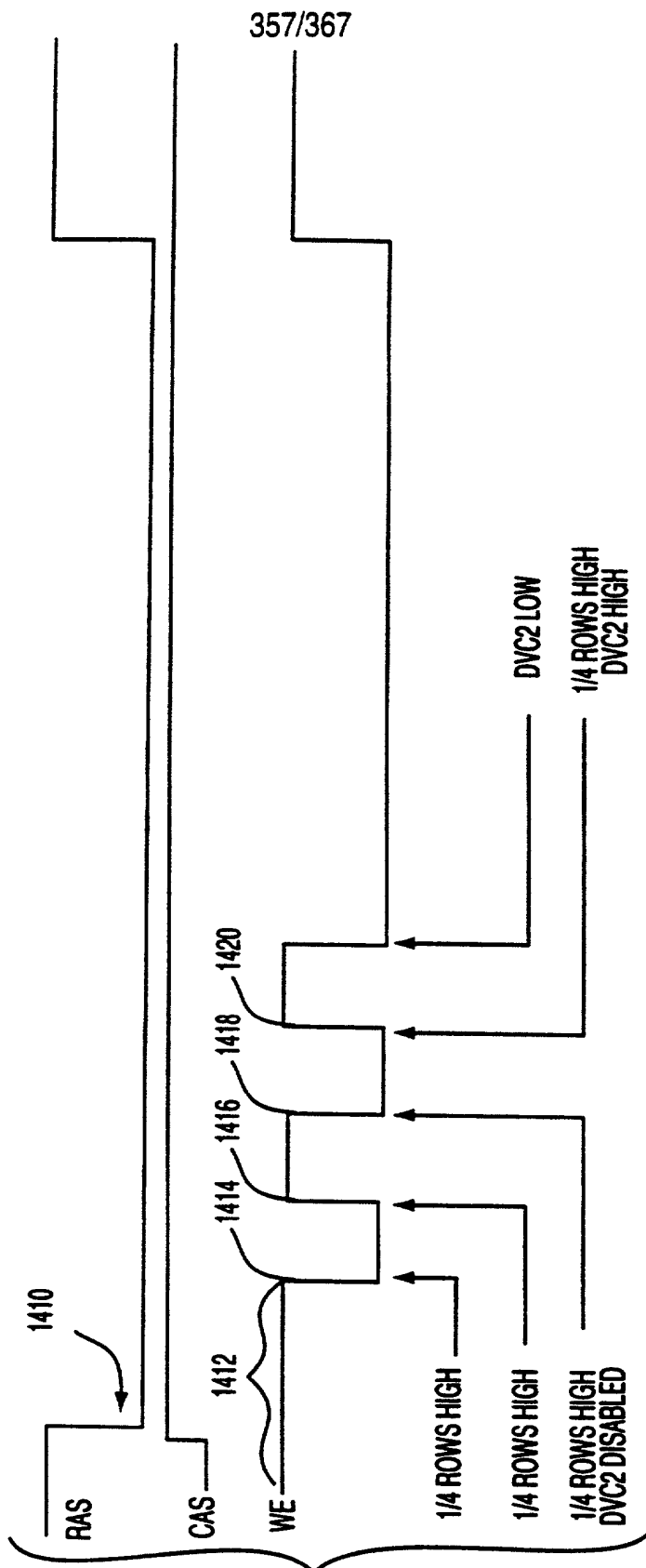
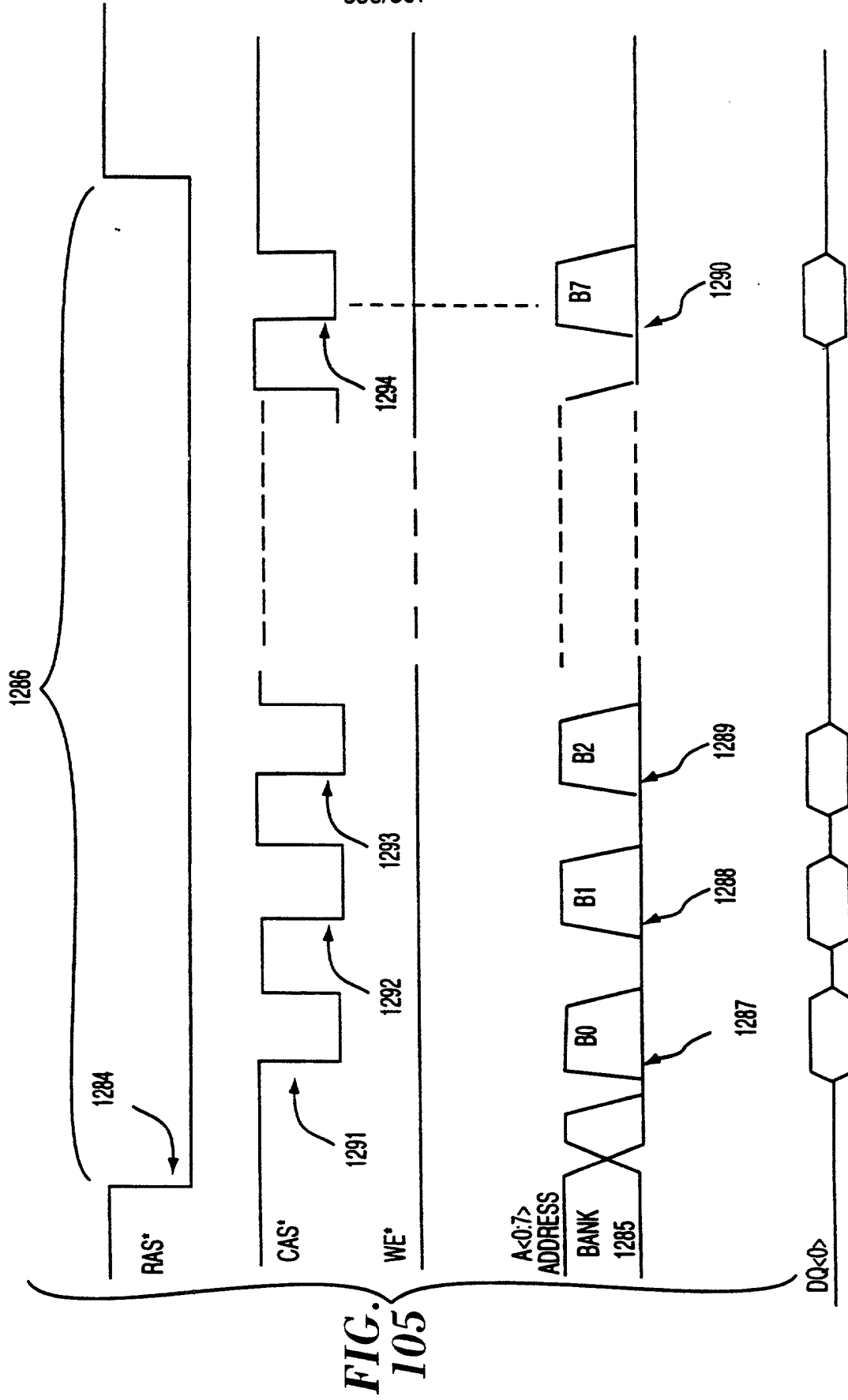


FIG. 103



**FIG.**  
**104**



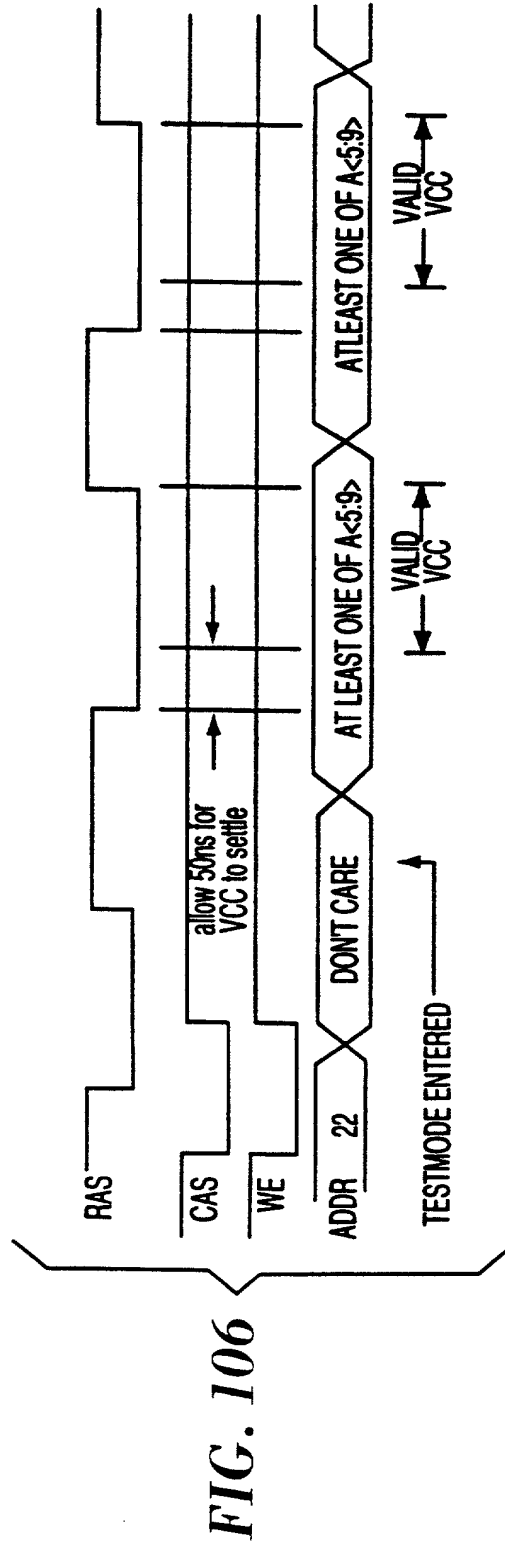
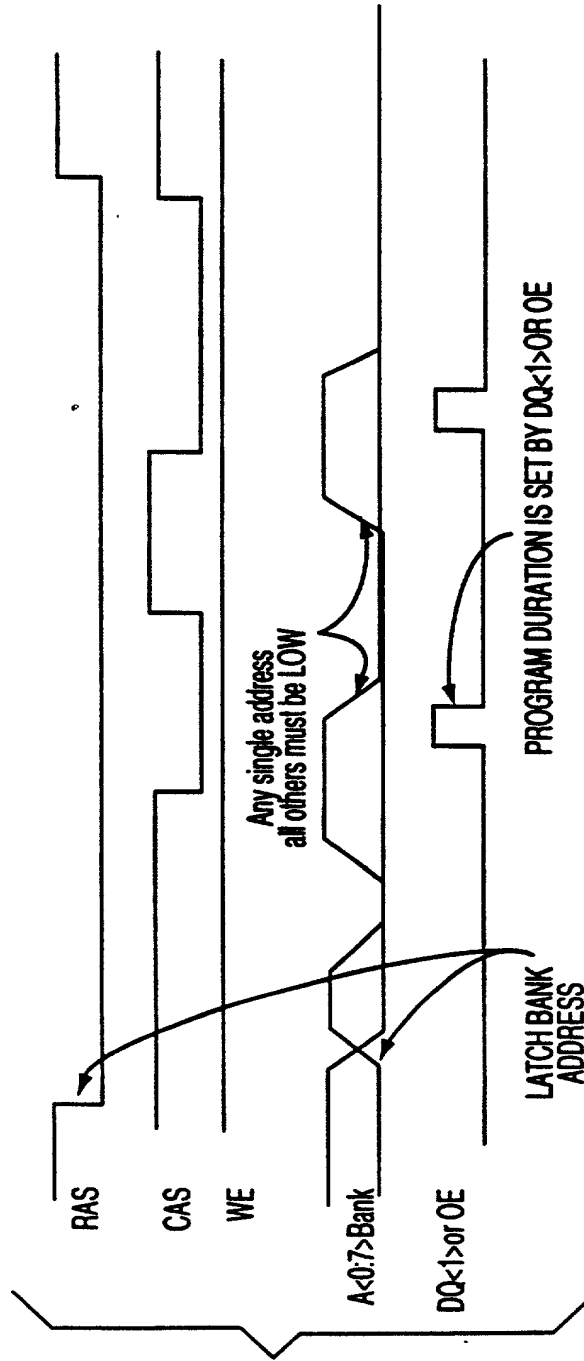
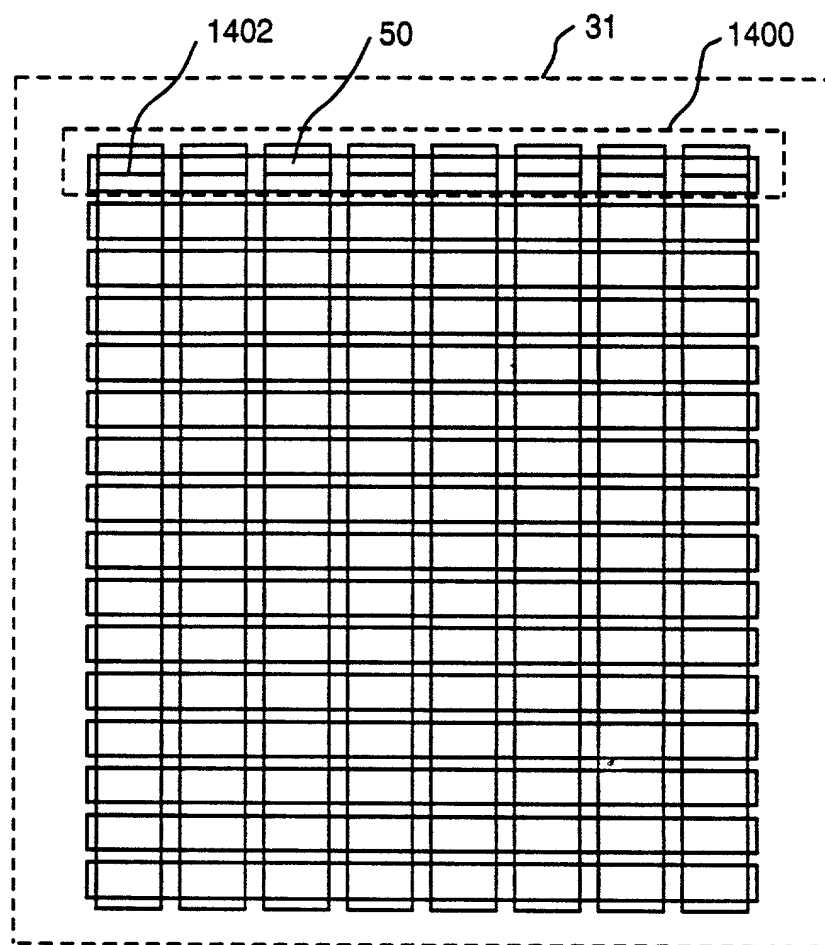


FIG. 107



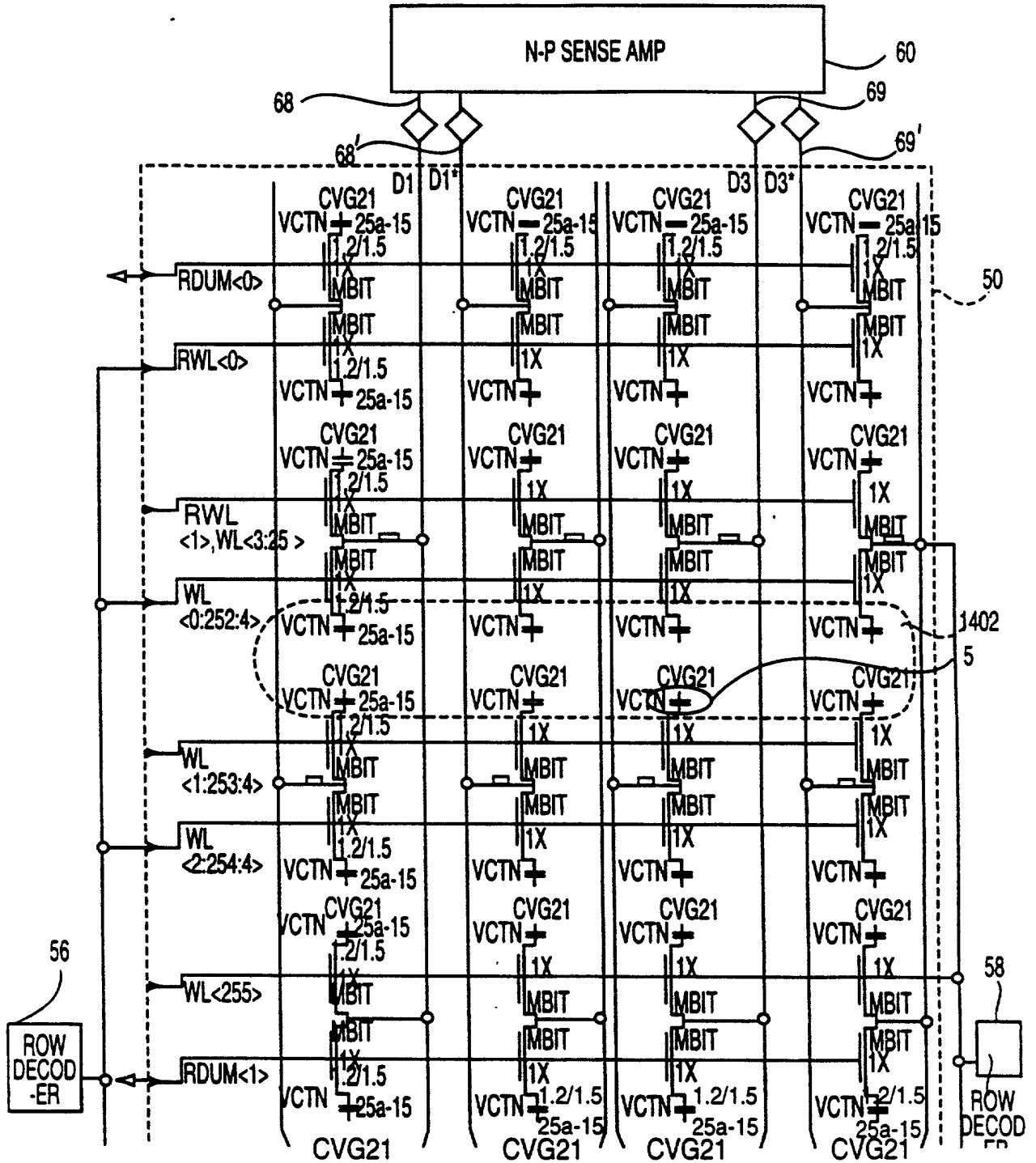


**FIG. 108**

**FIG. 109-1**

FIG. 109-1

FIG. 109-2



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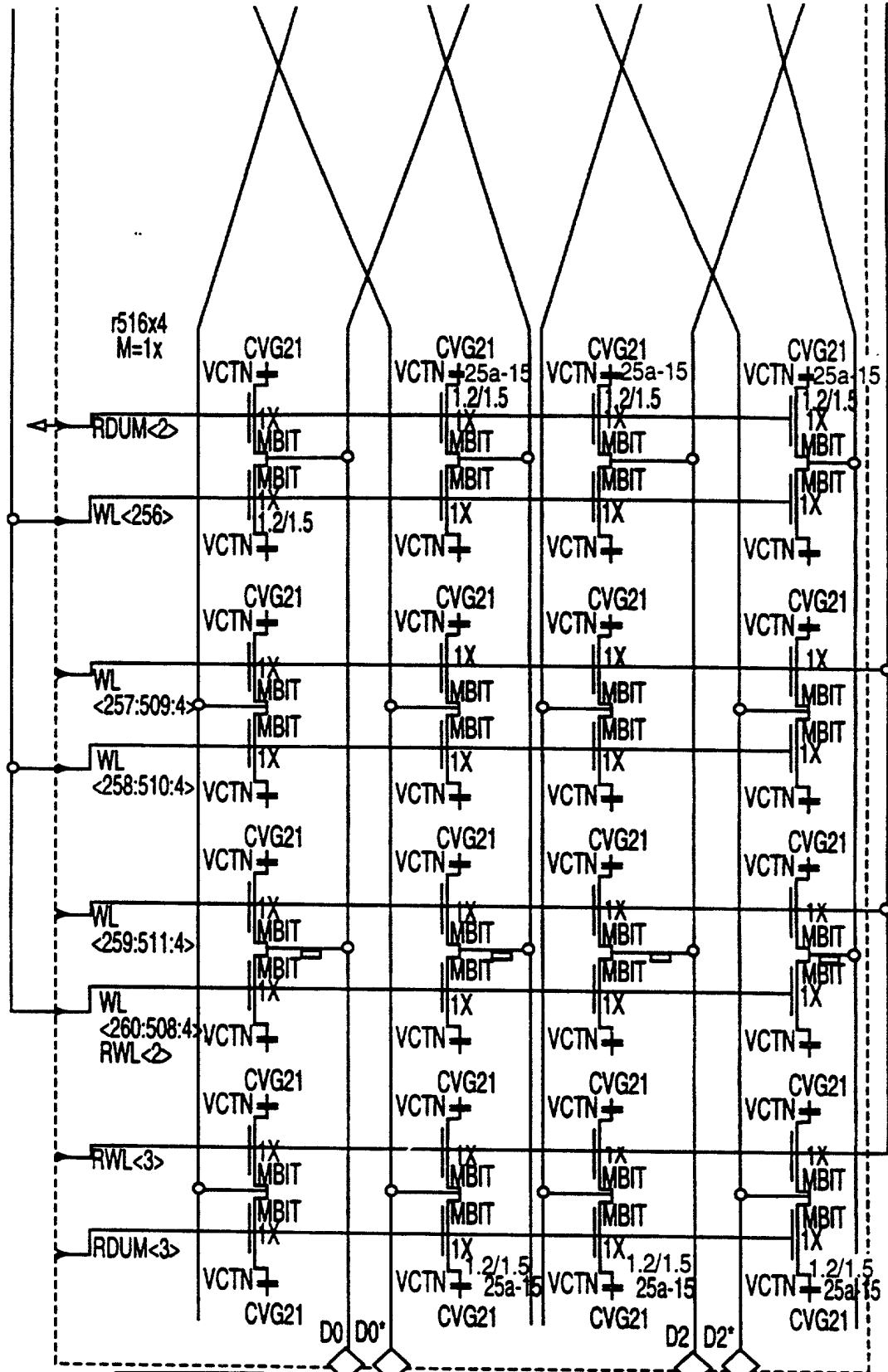


FIG. 109-1  
FIG. 109-2

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FIG. 109-2

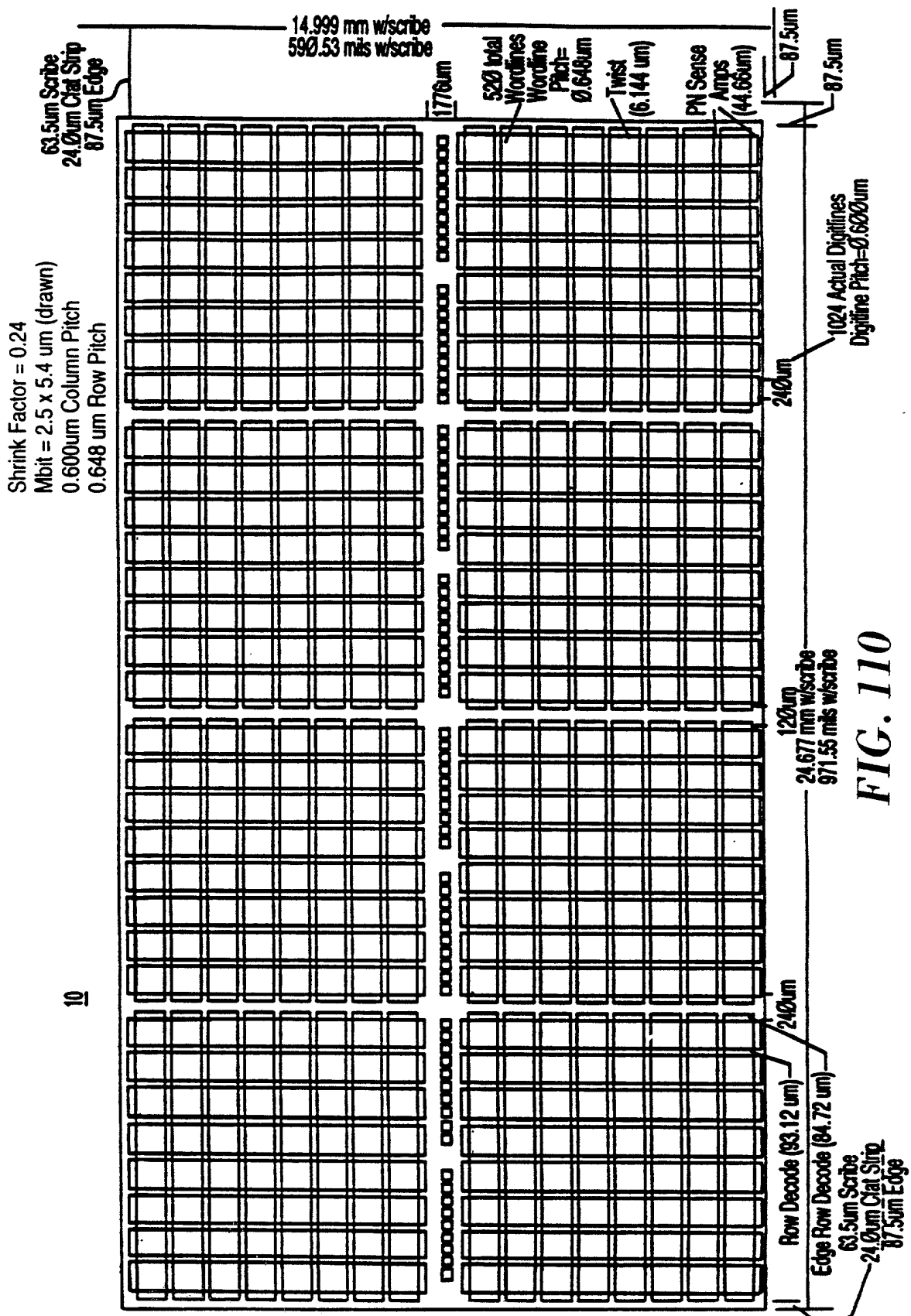
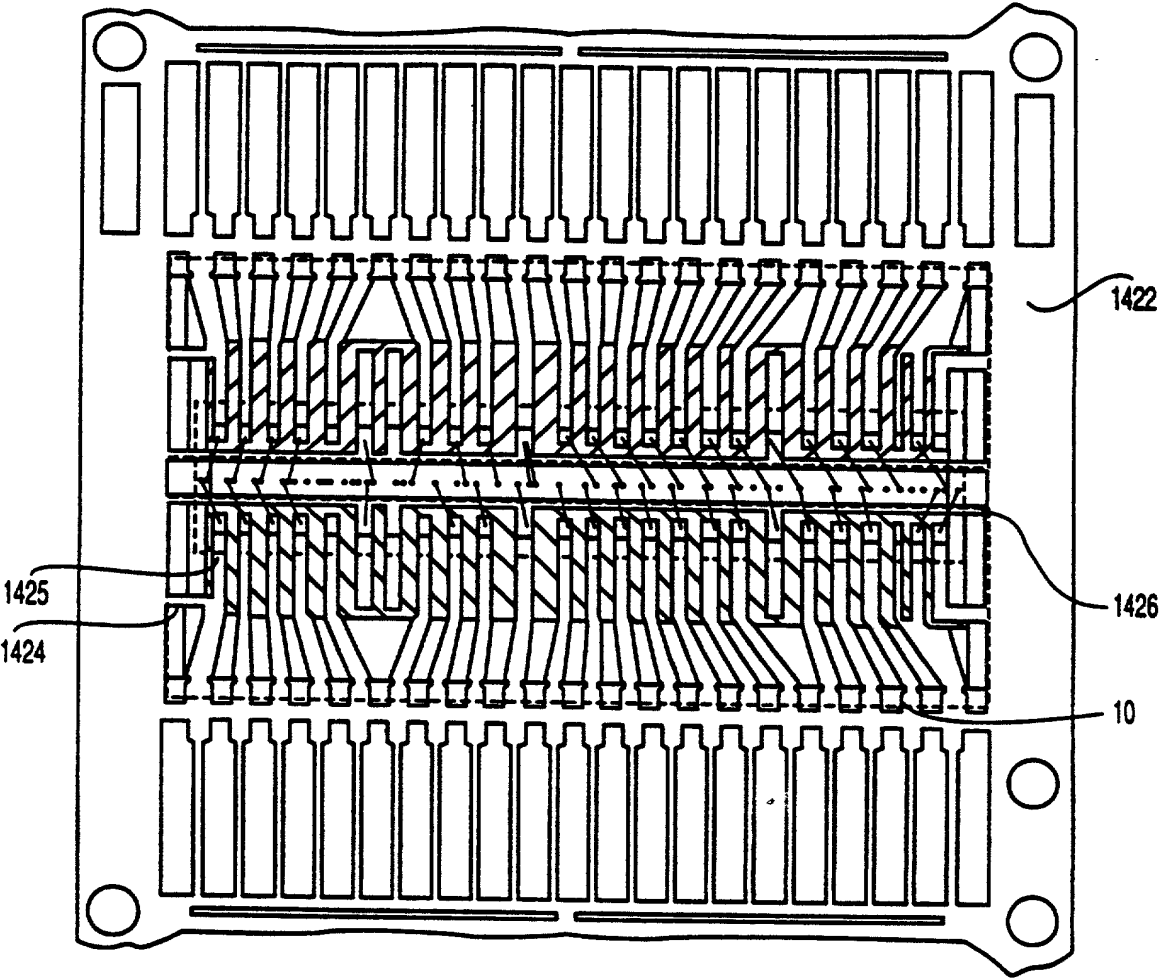
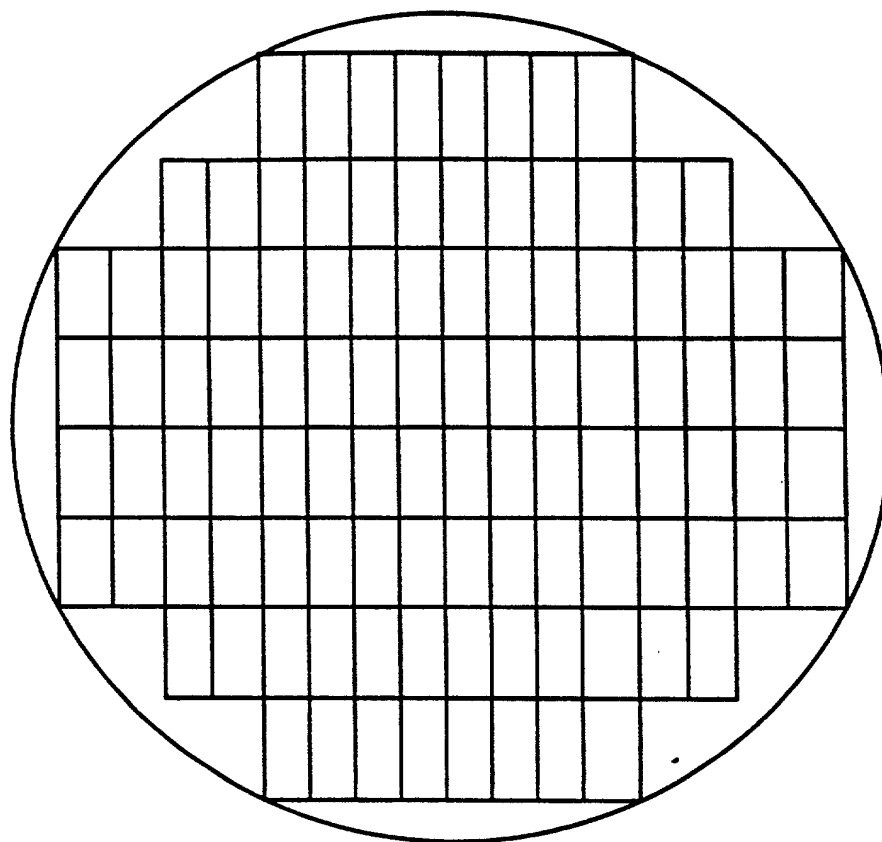
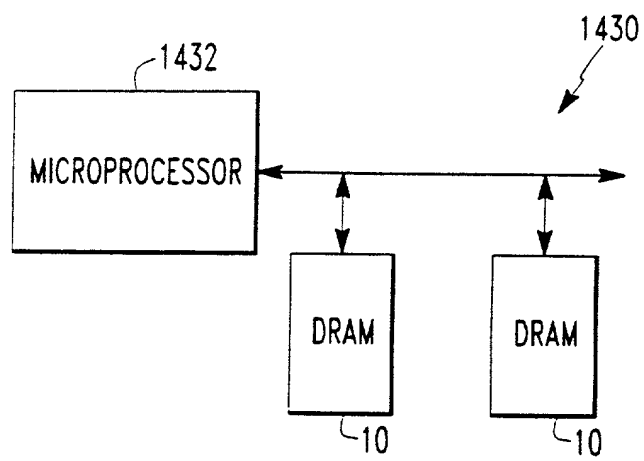


FIG. 110



**FIG. 111**

**FIG. 112**

*FIG. 113*